Improving Quantum Computer Scalability with Cryogenic Reversible Logic

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***Abstract*— Quantum computer scale-up is a world-wide priority, with the cryocooler power consumption being one of the limiting factors. For cryogenic qubits, the accepted direction is to compress the data in the cables that go in and out of the cryostat to reduce heat leakage, using cryogenic electronics to decompress and compress the data – yet this leads to the dissipation of the cryo-CMOS in the cryostat becoming a limiting factor. This talk considers reducing the dissipation of cryo-CMOS by around 100× by using a "reversible" circuit design. The talk discusses how the quantum computer environment is a "special case" allowing much lower dissipation than CMOS in smartphones (for example), provided that new circuits are used. The talk discusses the necessary circuits for control of error-corrected quantum computer and the results of simulation.**

***Keywords (Index Terms)* — Digital, quantum, reversible logic, reversible computing, quantum computing, cryogenic, electronics, adiabatic, quantum error correction.**

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