

Observations from Quantum Week and Opportunities for CSC

Erik P. DeBenedictis
Zettaflops, LLC
Albuquerque, NM, USA
erikdebenedictis@zettaflops.org

Abstract—CSC supported the IEEE Quantum Initiative’s Quantum Week. Some of the keynotes and workshops gave a positive assessment of the prospects for quantum computers and notably the potential contributions of CSC members. The quantum computing goal is to scale up to millions of error-corrected qubits. A million qubits would allow solution of real-world problems and error correction would allow computations that last hours or days instead of milliseconds. From the workshop at Quantum Week, there are plans for scaling to 1,000 qubits without error correction. To scale further will require some innovative technology directions—specifically directions that are well aligned with CSC’s topical space because they involve integrated classical and quantum components operating at cryogenic temperatures. CSC members as a group are uniquely equipped to support these technologies through superconducting qubits, classical Josephson junction electronics, familiarity with cryogenics, and scalable computer design.

Keywords—transmon, superconducting qubit, spin qubit, ion trap, scalability, quantum computer, cryo CMOS, SFQ, cryogenics, quantum error correction

I. CSC IDEALLY POSITIONED

Quantum computing and engineering are rapidly gaining traction, motivated by a quest for million qubits quantum computers. Such a computer may be a decade or more away, yet there is a growing view that “quantum advantage” will be demonstrated in the next few years. Quantum advantage implies quantum computers that customers would buy because they are more effective for their problems than classical supercomputers. This milestone could be the turning point from an industry supported by research funding to one supported by reinvested profits.

This short article shows how CSC’s topic mix that includes both classical and quantum technologies could give CSC a vital role in the development of this important new field.

A. A Quantum Moore’s law

Moore’s law has become a popular concept in computer technology. It is reasonable to ask if transmons, which are superconducting qubits, could be the “CMOS” for quantum computers.

Moore’s law led to Complementary Metal Oxide Semiconductor (CMOS) electronics improving in speed, power, and the number of devices per chip for decades,

powering a worldwide information revolution. The widely held belief is that Moore’s law was a smooth process, but this was not the case.

Moore’s law was originally formulated in the era of bipolar transistors but shifted to MOSFETs around 1980 due to MOSFETs being more manufacturable at scale. There was also a time when Gallium Arsenide was projected to take over from Silicon due to higher performance at the materials level. From the perspective of CSC members, the shift to Gallium Arsenide rolled out like the shift from cryogenic to room-temperature superconductors—they looked like good ideas, but nature did not agree.

Currently, superconducting transmons are the basis of the most effective quantum computer demonstration to date, the Google quantum supremacy demonstration involving the Sycamore chip and Oak Ridge National Laboratories’ Summit supercomputer [1]. However, the transmon has competitors. Ion traps seem ready to take the lead, but (prior to Quantum Week) spin qubits were most scalable due to the small size of single-atom qubits allowing up to 10^8 qubits per chip [2].

However, these qubits may not roll out as their advocates hope. Ion traps have a three-dimensional structure involving both optics and electronics that has never been demonstrated to be scalable.

While it may be possible to fit 10^8 spin qubits on a chip, several of the workshops at Quantum Week concluded that cryo CMOS control electronics would be far larger than the qubits and dissipate so much heat that scaling would be limited to 1,000 qubits [3].

Transmons are physically large compared to spin qubits, which could limit their scalability. However, the proponents of transmons have circuit refinements with new names like fluxonium [4]. Fluxonium is also based on superconductors, and hence assures continuity for CSC’s interest, yet the perception that quantum computers have a smooth scaling process will be hampered by the name of the underlying technology changing too often.

So, there is a quantum computer scale up race underway that is similar in some ways to the evolution of semiconductors. Superconducting qubits are a viable entry for sure, yet it remains to be seen whether superconducting qubits are destined to fill the role of bipolar transistors, CMOS, or Gallium Arsenide. However, CSC has a role refereeing the race.

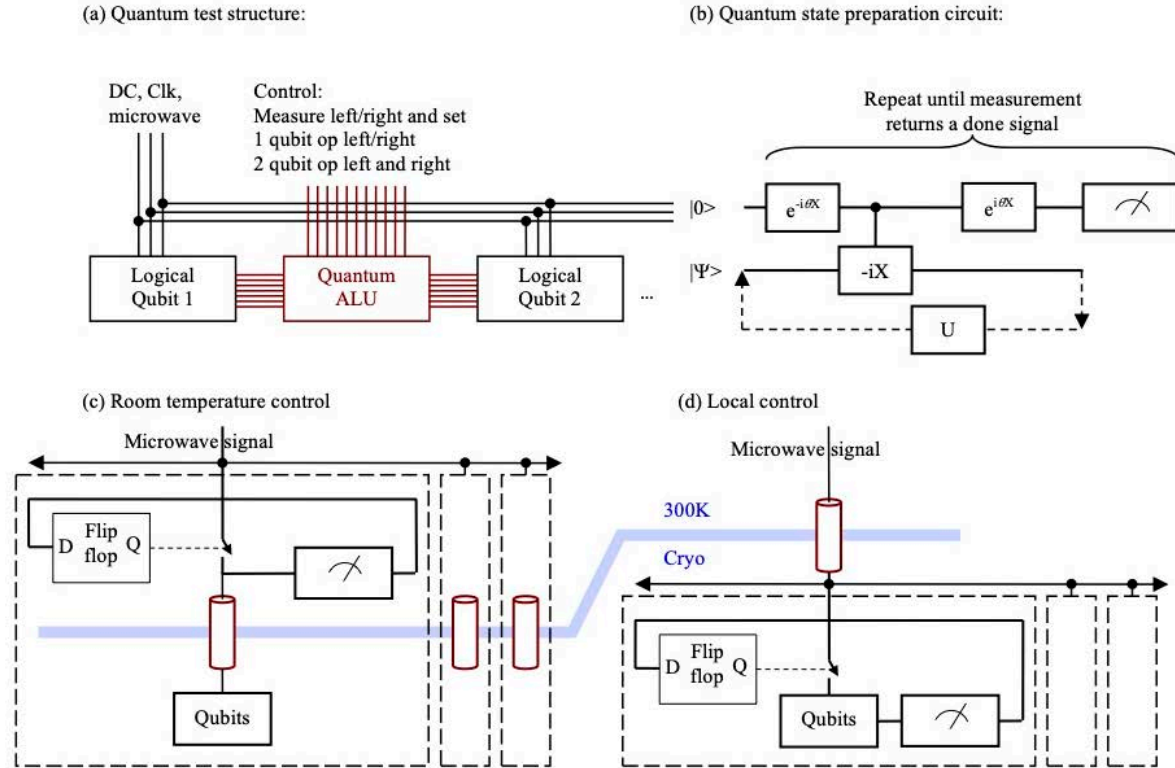


Fig. 1. (a) Representative integrated classical-quantum structure; logical qubits share control signals, but error correction behavior is local. Quantum logic that solves the user’s problem is in red. (b) Exemplary preparation for a small angular rotation. U is a correction. See ref. [5] for more information. (c) (d) Implementation as a mixed classical-quantum hybrid circuit with room temperature vs. local classical control. The key difference is whether one cable crosses the temperature gradient per qubit or whether some classical electronics is duplicated.

II. NEXT: CLASSICAL MEETS QUANTUM

The Google quantum supremacy demonstration [1] was purely quantum, meaning all its steps were rotations in a higher dimensional space (except I/O). However, useful quantum algorithms will require a mixture of classical and quantum operations. The best-known example is quantum error correction, where the presence of a qubit error inevitably leads the quantum computer to interrupt its quantum program briefly to fix the error. The interruption of the quantum computer’s control system is an inherently classical operation yet based on quantum information, creating a feedback loop within the system that has not been widely studied before. To scale up further will require knowing how to implement these coupled classical and quantum operations in a system that will inevitably become a new type of computer architecture.

Let me drill down into these new requirements, since they could become part of the mission of the CSC.

A. Quantum error correction

Quantum error correction is the next major quantum computing scale up challenge. In familiar language, qubits lose information over time like the bits in a common Dynamic Random-Access Memory (DRAM). To be useful in long-running calculations, both DRAM bits and qubits

need periodic “maintenance” to counter this loss. For qubits, this means implementing each logical qubit by a group of physical qubits that are protected by a quantum error correction code. The error correction code must be evaluated periodically to see if an error has occurred. Multiple errors cannot be corrected, so errors must be corrected promptly or there is a chance the whole calculation will fail.

A DRAM’s maintenance is called refresh and it is performed with special logic that refreshes entire rows of a DRAM array at once. The equivalent for a quantum computer is illustrated in Fig. 1a, where a common set of wires (shown in black) causes an error correction cycle on many qubits at once. The other wires (in red) would be gates that execute the user’s algorithm. Experimental demonstrations of quantum error correction are only now being attempted, and only on single logical qubits.

B. Post selection is simpler

Quantum error correction is too complex for this short article, so Fig. 1b shows a simpler structure that can serve as an example. Fig. 1b shows what is called a post-selected quantum computation, [5] which is essentially a loop in computer programming. The diagram shows two qubits, one containing data, $|\Psi\rangle$, and one called $|extra\rangle$ that is initialized to $|0\rangle$. A quantum gate operation is performed on the qubits and the extra qubit is then “measured,” or converted into a

classical 0 or 1. The extra bit controls the loop. If the bit is 1, the loop runs again. Otherwise, it exits. So, the circuit is like a computer program “do $f(|\Psi\rangle, |\text{extra}\rangle)$ while $(|\text{extra}| = 1)$.”

To demonstrate quantum error correction using the approach used in [1] would require a room temperature signal generator to send signals into the cryostat to make the qubits evaluate the error correction code. The quantum operations will lead to a measurement where a weak signal with the result moves from the qubit through a signal processing apparatus to room temperature. If the measurement returns a 1 the qubit is in error and the signal generator sends a signal pattern for correcting the qubit.

A simplified version of the feedback process described earlier is shown in Fig. 1c. The diagram shows the quantum measurement value being latched into a classical flip flop, which will open a switch to prevent the error correction waveform from reaching the qubit if there is no error.

Unfortunately, the diagram in Fig. 1c does not scale very well. Replicating the qubit structure in the dashed box would require duplicating the microwave cable from room temperature to the qubits. These cables cost thousands of dollars each and leak heat into the cold environment, increasing the load on the refrigerator. While nobody really knows how to build a large-scale quantum computer, there seems to be agreement that one wire crossing the temperature gradient per qubit will not work.

C. A more scalable approach

Fig. 1d accomplishes the same result more scalably by moving some of the electronics into the cold environment. In this case, a microwave signal is transmitted to the cold environment as a standard signal. The qubit measurement, flip flop, and switch are in the cold environment. Abstractly, the cost of the control electronics is multiplied by the scaling factor, or the number of qubits, instead of the cost of the cable. Demonstration of this point has become the next major milestone.

III. A MISSION FOR CSC

There is a concept in business called best of breed [6]. When applied to quantum computers, it says the best quantum computer will be a combination of the best qubit, the transmon, and the best classical electronics, CMOS. This design philosophy has been explored and shows a clear path to 10^3 qubits.

However, the goal is 10^6 error-corrected qubits.

In business, the alternate approach is called “integrated system,” which is recognized as being more appropriate for larger or more mature enterprises.

A. Integrating classical and quantum technologies

The open question is what classical and quantum functions are needed in the cryogenic environment and how to implement them. It is much more difficult to implement a function in the cold environment, so it would be desirable to

partition quantum error correction and other functions between room temperature and the cryogenic environment. Exactly what subfunctions need to be in the cold environment is an open question.

The best explored technology combination is transmons with cryo CMOS control. Yet the conclusion from Quantum Week and elsewhere is that this approach will only work to about 1,000 qubits, after which the heat dissipation of cryo CMOS becomes a scaling limit. The semiconductor industry has sunk untold billions of dollars into reducing CMOS energy dissipation with disappointing results.

B. What about Josephson junctions used classically?

CSC members have experience with analog JJ circuits and SFQ and adiabatic logic. This is a viable option that CSC, its members, and its supporting societies are ideally suited to address.

C. Best of breed to integrated system

The difficulty with an integrated system is that it requires an interdisciplinary workforce that not only understands the original “breeds,” but understands the interactions behind them so the disparate technologies can be combined in a way that exploits their synergies.

Every transmon is unique because of manufacturing variances. Taken at face value, the common microwave signal in Fig. 1d would only work if the transmons were tuned after manufacture to a common frequency, which is not done at present. Does this mean Fig. 1 is incorrect or does it mean that future qubit designs need to consider scalability and classical electronics?

Designing qubits to cater to the scalability requirements of classical electronics would require a tight interdisciplinary coupling between computer design and physics research, yet this is a coupling that CSC is in an ideal position to address.

One of the main goals of IEEE is to encourage communications between its members. CSC’s sponsoring societies and their members are very well aligned with the next steps in this aspect of quantum computing.

REFERENCES

- [1] Arute, Frank, et al., “Quantum supremacy using a programmable superconducting processor,” *Nature* 574.7779 (2019): 505-510.
- [2] Veldhorst, M., et al., “Silicon CMOS architecture for a spin-based quantum computer,” *Nature communications* 8.1 (2017): 1766.
- [3] Pauka, S. J., et al., “A cryogenic interface for controlling many qubits,” *arXiv preprint arXiv:1912.01299* (2019).
- [4] Kjaergaard, Morten, et al. “Superconducting qubits: Current state of play.” *Annual Review of Condensed Matter Physics* 11 (2020): 369-395. <https://doi.org/10.1146/annurev-conmatphys-031119-050605>.
- [5] Wiebe, Nathan, and Vadym Kliuchnikov, Floating point representations in quantum circuit synthesis, *New Journal of Physics* 15.9 (2013): 093041.
- [6] Best of Breed System <https://www.techopedia.com/definition/23200/best-of-breed-system>