Fully Functional Operation of Low-Power 64-kb Josephson-CMOS Hybrid Memories

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Abstract **- We have been developing a Josephson-CMOS hybrid memory with sub-nanosecond access time in order to overcome the memory bottleneck in single-flux-quantum (SFQ) digital systems. In this study, we aimed at reducing the power consumption of the 64-kb CMOS static RAMs to prevent the drawback of hybrid memory. We took three approaches, miniaturization of memory cells, improvement of data drivers and employment of a binary-tree decoder. By using these techniques, we decreased the power consumption of 64-kb CMOS static RAMs by 54% in Write operation and by 8% in Read operation. Moreover, we aimed at demonstrating fully functional operation of the 64-kb Josephson-CMOS hybrid memory composed of the low-power CMOS static RAM, Josephson interface circuits and Josephson current sensors by using the Rohm 0.18 μm CMOS process and the AIST standard process 2. We confirmed the correct memory operations for arbitrary address accesses. In circuit simulations, the total access time was evaluated to be 1718 ps. The power consumption was estimated to be 27.62 mW in Write operation and 21.25 mW in Read operation. Based on these estimations, we discuss the access time and power consumption of hybrid memories using future CMOS processes.**

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Keywords **– Single flux quantum electronics, SFQ electronics, CMOS, random access memory, RAM, hybrid memory, RAM power consumption, RAM access time**

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