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A Robust and Tree-Free Hybrid Clocking Technique for RSFQ Circuits – CSR Application

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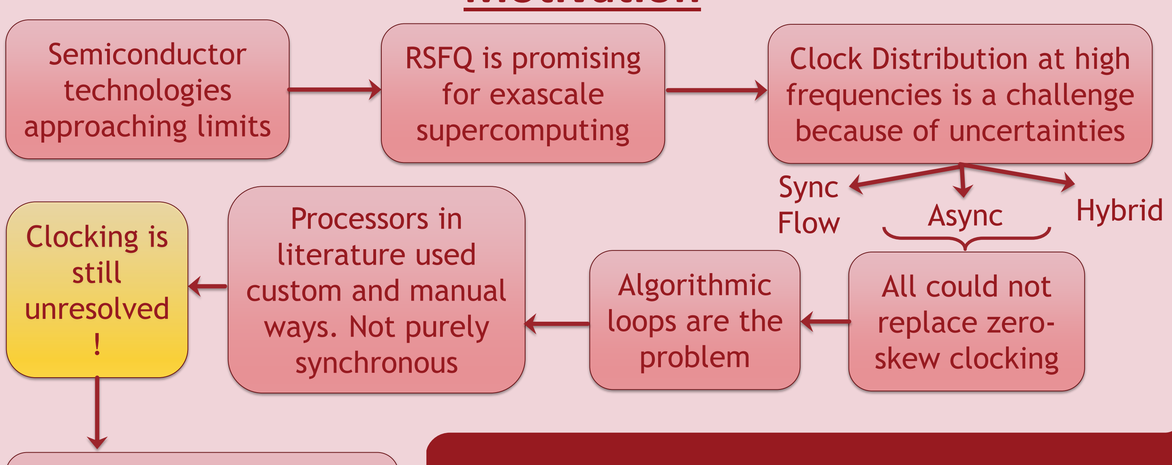
Abstract

One of the biggest challenges impeding RSFQ is the ultra-high-speed clocking of large scale circuits. The clocking complexity is aggravated by algorithmic loops and generic complex pipelines, whose presence is inevitable in large scale systems. This paper presents a new clocking technique, comprised of synchronized hybrid clock loops, whose frequency is intrinsically determined by the clock architecture. This tree-free scheme reduces the area, power, and complexities associated with traditional clock distribution networks. The timing constraints are locally defined within the hybrid clock loops of the architecture which improves robustness to variations. This paper demonstrates the clocking technique using a circular shift register (CSR) design, but argues its applicability to general RSFQ circuits. A SystemVerilog model of the architecture is built to quantify the benefits and prove the feasibility of the proposed scheme. As an example, for a 32-gates CSR, under a model of moderate local and global variations, our experimental results show up to 93% yield improvement at the same cycle time compared to zero-skew tree clocking.

Motivation



Clocking Loops

- Clocking a CSR has an additional constraint, the overall clock skew must be zero.
- Two available options: either zero-skew tree or mixed concurrent and counter flow.

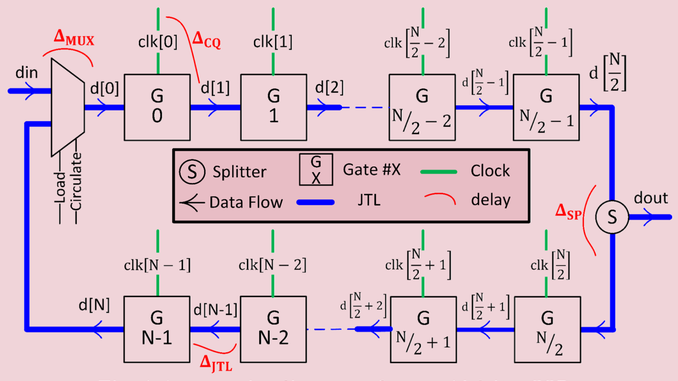


Fig.1 A generic diagram for an N-bits CSR.

I. Zero-skew tree

$$t_{clk[i]} - t_{clk[j]} = 0, \qquad \forall i, j$$

$$T \geq \Delta_{CQ} + \Delta_{JTL} + \Delta_{\mathrm{MUX}} + T_{setup}$$

$$\Delta_{CQ} + \Delta_{JTL} \geq T_{hold}$$

- Are generally problematic in large scale circuits.
- Large inductive clock network introduces uncertainties.
- Physical uncertainties are hard to account for.
- On-chip temperature fluctuations cause unexpected jitter and skew.
- Timing jitter from clock source.

II. Mixed

- Half is clocked concurrent-flow and half is counter-flow.

$$T \geq \Delta_{CQ} + \Delta_{JTL} + \Delta_{\mathrm{MUX}} + T_{setup}$$

$$\Delta_{CQ} + \Delta_{JTL} \geq T_{skew} + T_{hold}$$

- Global timing constraints define the clock frequency.
- Timing jitter from clock source.
- Need a single point of convergence and divergence.
- Need to superimpose the clock and the data flows.
- It is a scheme only applicable to a CSR.

The Proposed Clocking Scheme: HCLC

- Hybrid Clover-Leaves Clocking (HCLC).
- M pairs of hybrid clocked loops, or leaves, where each pair has one concurrent flow leaf and one counter-flow leaf.
- Tree-free. No clock source, only a GO signal.
- Frequency of operation is intrinsically determined.
- Higher robustness to the various uncertainties of the RSFQ technology.

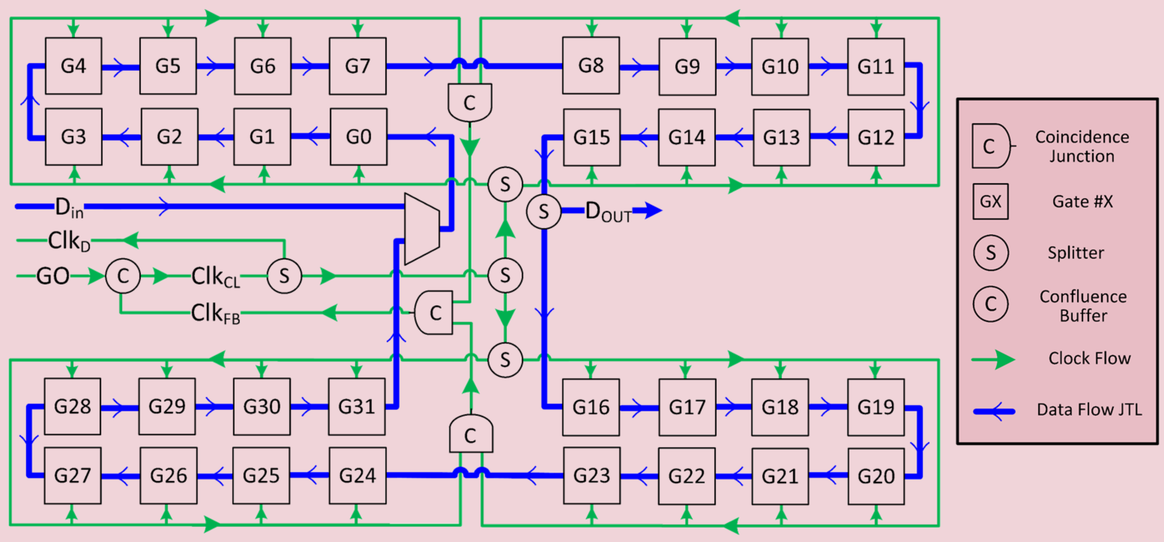


Fig.2 The proposed HCLC for a 32 gates CSR with M=2.

Simulations

- We built our own simulation platform for the CSRs.
- SystemVerilog used to model the RSFQ fluxons flow.

Timing Analysis

$$T = L_{leaf_{max}} \cdot T_{skew} + \Delta_{CF} + \Delta_{SP} + \log_2(2M) \cdot (\Delta_{SP} + \Delta_{CC})$$

$$T \geq \Delta_{CQ} + \Delta_{JTL} + \Delta_{\mathrm{MUX}} + T_{setup}$$

$$\Delta_{CQ} + \Delta_{JTL} \geq T_{skew} + T_{hold}$$

- We used DFFs as gates and JTLs as CSR data path. Data is loaded then circulated.
- Test the functionality and the timing violations using SystemVerilog directives.
- Modeled gate delays as independent Gaussian random variables.
- Ran Monte Carlo with $3\sigma_{global} = 20\%, 3\sigma_{local} = 10\%$, in addition to σ for non-idealities and other uncertainties. Clock sources with clock jitter of $\sigma = 5.8\%$.
- The results show that HCLC provides a more robust solution than the zero skew.
- The mixed-CSR gives similar robustness (but it is CSR-specific).
- HCLC achieves the same yield but with faster operation than the mixed-CSR.

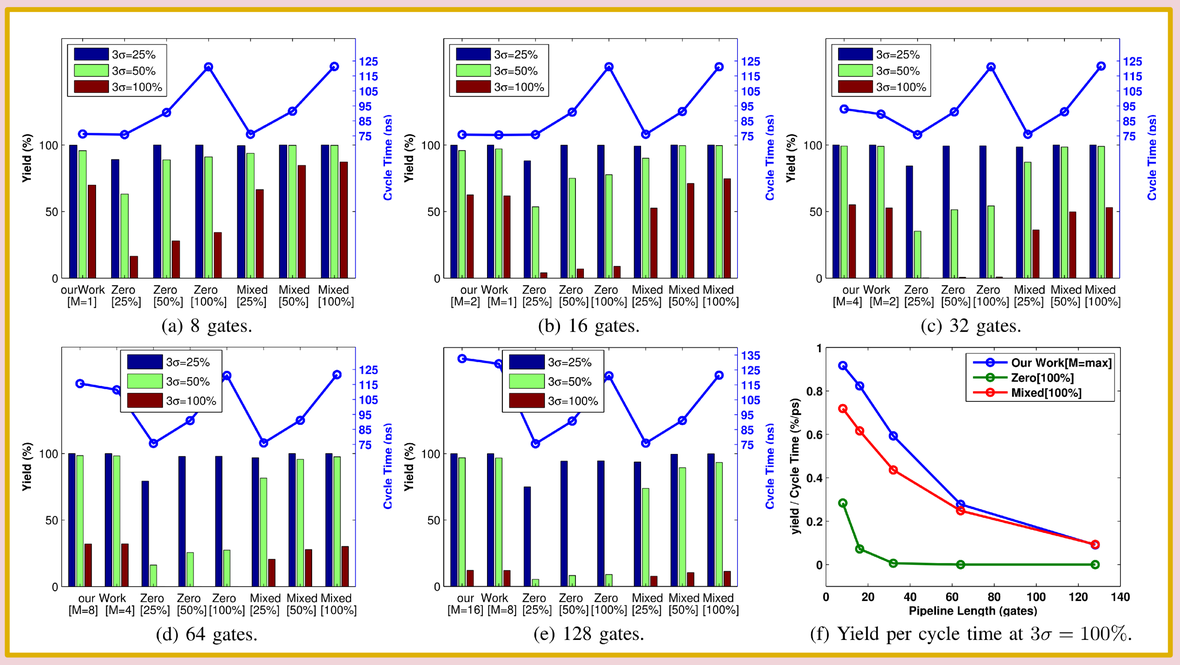


Fig.3 (a-e) The bars are the yield (left y-axis) at different non-idealities standard deviation, while the line is the average cycle time (right y-axis). The figures are for different pipeline lengths, and the percentage below the design name is the clock cycle added margin w.r.t. the setup constraint. (f) The yield with non-idealities $3\sigma = 100\%$ divided by the cycle time versus different pipeline lengths.

Extensions and Future Work

- Creating a hierarchy of clovers within clovers, building groups recursively.
- Conditional conjunction between clocks from interleaving clovers to accommodate complex pipelines.
- The data flow and clock flow can be arranged separately.
- Hybrid approach where the clover element is a zero-skew cluster.

➢ Bypassing the clovers hierarchically and eliminating the insertion delay from the cycle time.
➢ An O(1) cycle time clocking architecture whose robustness is based on spatial correlation.
➢ The benefits of the clocking strategy depends on a process of ordering and grouping the gates.

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