Experimental Investigation of ERSFQ Circuit for Parallel Multibit Data Transmission

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***Abstract*—We present test results for parallel data communication ERSFQ circuits with clock recovery. We experimentally study on-chip and chip-to-chip parallel data communication circuits with 4-, 8- and 16-bit word lengths. The largest circuit is a 16-bit chip-to-chip communication test circuit embedded into a testbed with clock distributed over a combination of active and passive transmission lines with transmitter/receiver pairs, and is comprised of 3464 Josephson junctions in total. All ERSFQ circuits are fabricated using MIT-LL 10-kA/cm^2 SFQ5ee process. For the chip-to-chip communication experiment, a multi-chip module (MCM) is assembled using Hypres' MCM flip-chip bonding process which connected the MIT-LL-made flip-chip to the Hypres-made MCM carrier using 220 signal bumps with 50 um pitch. We experimentally confirmed correct functionality of 4-, 8- and 16-bit circuits and measured their current bias margins. For the 16-bit chip-to-chip communication circuit mounted to a MCM, we measured ±12% dc bias margins similar to the margins measured for the on-chip version of the same circuit. The MCM circuit is also evaluated at high clock speed generated by an external source, while the data words are changed at low speed. The correct functionality is observed without significant reduction in the bias margins using average-voltage test approach.**

Keywords—energy-efficient computation, SFQ, data link, clock recovery, asynchronous, superconducting

I. Introduction

Energy efficiency became the limiting factor defining the semiconductor processor performance. The estimated power required by the next generation semiconductor-based exascale supercomputer might reach ~100 megawatts [1, 2]. A significant improvement in energy efficiency can be achieved with superconducting single flux quantum (SFQ) digital technology which can offer both low power dissipation and high clock speed [3, 4].

One of the critical items in design of high-speed data processing circuits is a communication of parallel multi-bit data words over distances on-chip and between chips, often connecting different clock domains. This requires an accurate timing control of the received data to recover clock, avoid data skews and prevent additional latencies. In superconducting high data rate circuits, the clock period can ultimately be less than the transmission time over the communication data links. In this case, several subsequent data words can be traveling on the link at the same time. For RSFQ-type circuits, clocking is local; transmitters and receivers belong to different clock domains. This makes clock recovery, skew-free data links highly critical.

In this paper, we present the results of experimental investigation of our ERSFQ [5] parallel data communication circuits with clock recovery and skew protection. We implemented and tested the communication circuits for the on-chip and chip-to-chip data links integrated in the multi-chip module (MCM).

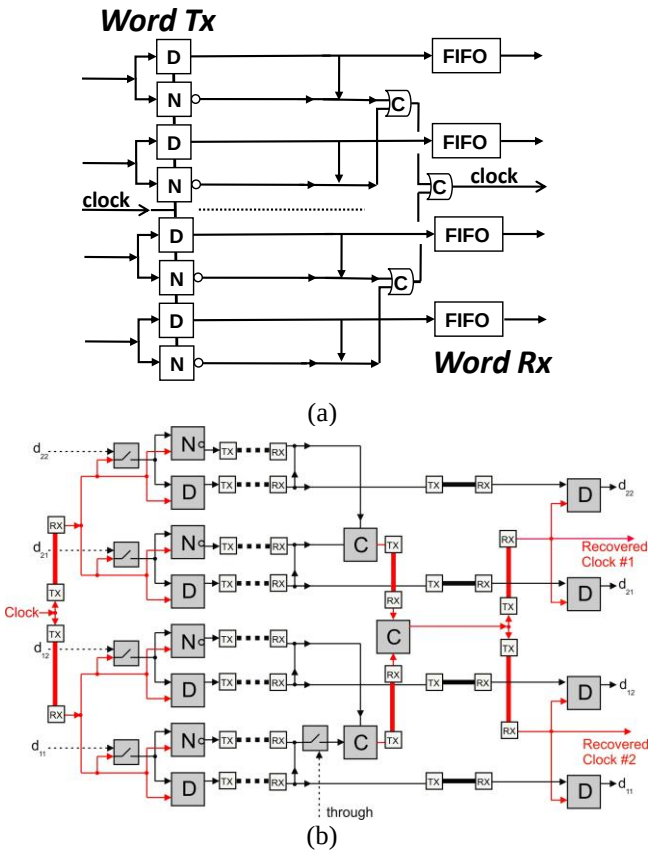

Fig. 1. (a) General block-diagram for parallel multibit data transmission with clock recovery. (b) The block-diagram of MCM experiment: external dc controls are shown with dashed lines, PTLs are in bold and carrier/flip-chip/carrier transmission is shown in dotted bold.

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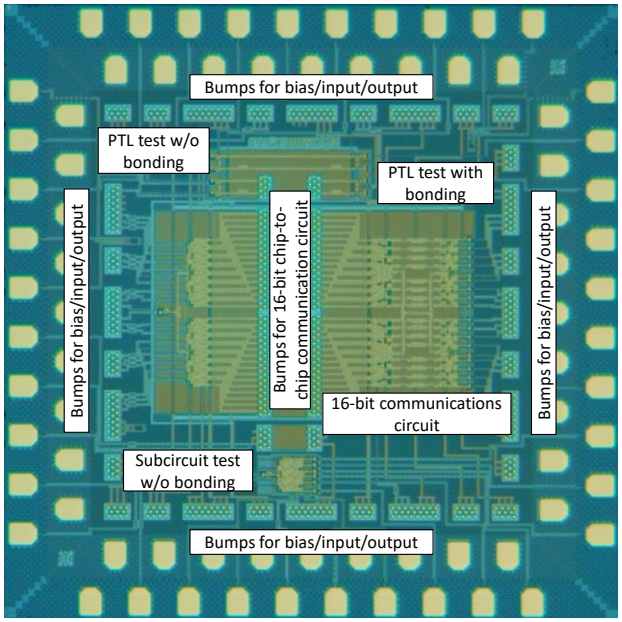

Fig. 2. Flip-chip with 16-bit communication circuit and test structures.

II. Design Approach and Layout

Fig. 1a presents a general block diagram of our approach to transmit parallel multi-bit data. The main idea is to have every data bit in true and complementary forms. Thus, an SFQ pulse will always be transmitted regardless of the bit value. A synchronous generation of complementary data is done using D-cells (D flip-flop (DFF)) and N-cells (NOT gates). At the receiver side, the true bit lines go to the buffer (e.g., FIFO buffer) awaiting the recovered clock signal.

The signal of arrival of a bit is generated by the merging of corresponding true and complementary lines to assure the arrival of SFQ pulse regardless of bit value. All channels are combined through the binary tree of C-elements [6] to recover clock. The clock to FIFO is released only when all bits have successfully reached the final C-element, with earlier data bits waiting in the FIFO of a sufficient depth for all data words to arrive. This approach eliminates problem with data skew and word-to-word interference.

In order to verify our design approach, three on-chip versions of the ERSFQ [5, 7] circuits with the increasing complexity (4-bit, 8-bit and 16-bit) are realized. In our particular experiment (with truncated 4-bit block diagram shown in Fig. 1b), data pulses are generated by applying clock pulses to dc-switches. As for the FIFO, a DFF is used in each bit line. Clock pulse going through such a switch generates data SFQ, if control dc current is applied. The C-element is the key of the whole clock recovery. It should produce single output if and only if both inputs arrive. The main drawback of asynchronous C-element is that it remains in the wrong state if only one input has arrived. Self-resetting is realized by adding small resistors to C-element storage loops. To experimentally verify the correct operation of the communication circuit, another dc-switch is added to allow introduction of an error and check self-resetting properties of the C-element. For the 16-bit circuit version, the data and clock distribution by means of only Josephson transmission lines (JTLs) becomes impractical and too energy consuming. The passive transmission lines (PTLs) with corresponding transmitter (Tx) and receiver (Rx) pairs are used (shown in bold in Fig. 1b).

Fig. 2 shows the layout of the 5x5 mm^2 MCM flip-chip of the most complex 16-bit experiment. The circuit is comprised of 3464 Josephson junctions and designed to be flip-chip bump bonded on 1-cm^2 MCM carrier. The main 16-bit communication circuit is laid out in the center of the chip

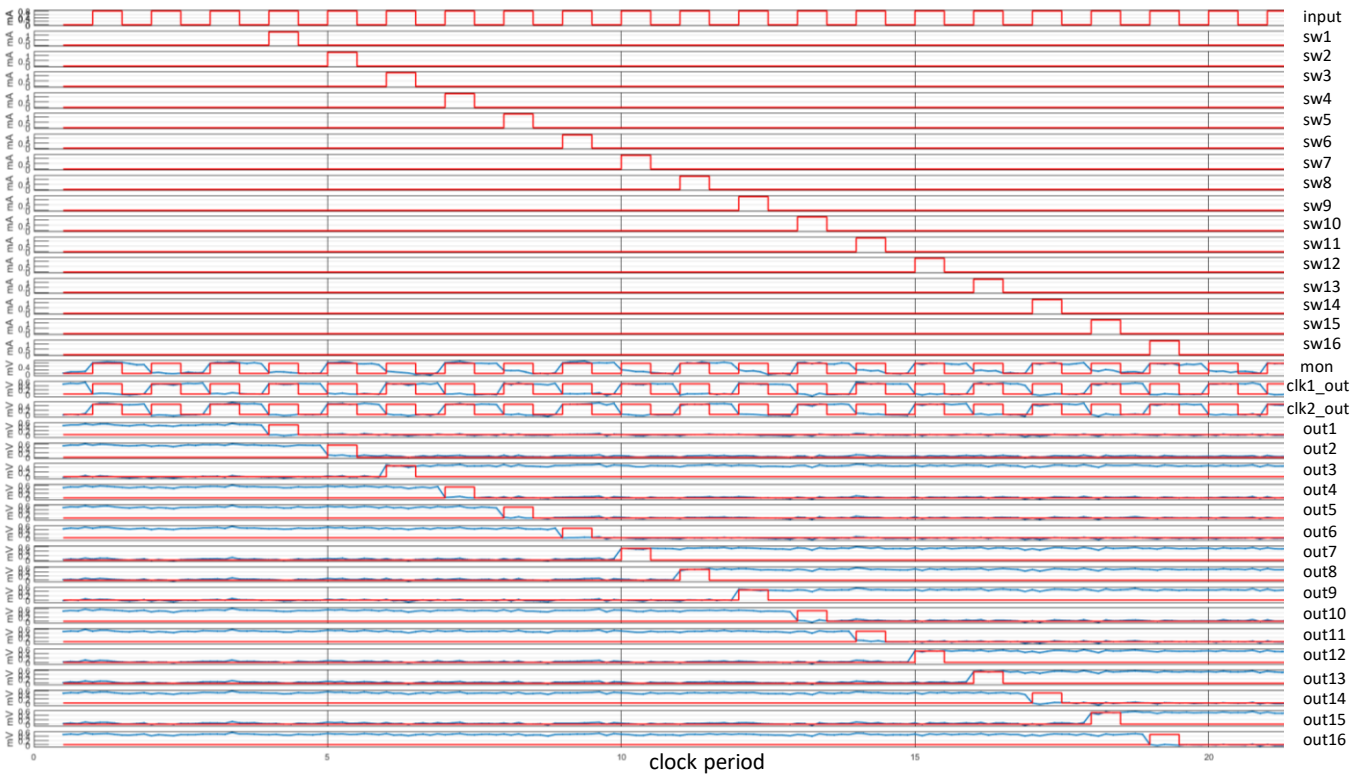

Fig. 3. Functionality test of the MCM with ERSFQ 16-bit communication circuit. The correct operation is verified with dc bias current operational margins measured. The red traces show input signals applied and expected outputs. The blue traces are the data and clock outputs measured via standard RSFQ toggle flip-flop SFQ/dc converters.

shown in Fig. 2 and can be tested only via MCM with input/output signal sent/measured through the bumps on its perimeter. To model chip-to-chip transmission, single flux quantum (SFQ) signals are sent off from the flip-chip to the MCM carrier, traverse the carrier, and then return to the flip chip. To facilitate this process, two columns of bumps are fabricated (visible in the center of the circuit layout in Fig. 2).

The flip-chip also includes multiple test structures to characterize: (a) fidelity of our MCM assembly process and current carrying ability of the bumps and (b) 4-bit communication circuit and PTLs to screen chips for design/fabrication yield. The operational bias margins of the latter structures are measured directly on the flip-chip without MCM.

III. Experiment

A. On-Chip Communication Circuits

Three versions of the on-chip experiment with ERSFQ 4-bit, 8-bit and 16-bit circuits on 5x5 mm^2 chips are designed for MIT-LL 10-kA/cm^2 SFQ5ee process [8]. The fabricated chips are mounted in immersion cryoprobe and evaluated at 4.2 K temperature with multilayer mu-metal providing necessary magnetic shielding. Functionality test and bias margin measurements are performed with the help of Octopux [9] multifunctional test system with control patterns applied and circuit outputs evaluated. The full and most energy-efficient (ERSFQ) bias margins are measured. By measuring the current-voltage characteristics (IVC) of ERSFQ bias limiting junctions, we are able to distinguish the most energy-efficient (EE) operation of the circuits (zero-voltage regime) when bias limiting JJs are not switching from the less energy-efficient when non-zero voltage is observed [10]. Table 1 lists typical full and EE bias margins for tested on-chip communication circuits.

TABLE I. Typical Bias Margins for On-chip Communication Circuits

	4-bit	8-bit	16-bit
I_c (mA)	33.55	119.7	350
Bias low (mA)	26	110.5	299
Bias high (mA)	42.5	140	414
Full margins (+/- %)	24.1	11.8	16.1
EE margins (+/- %)	12.7	4	7.9

B. MCM Assembly

To accommodate 5x5 mm^2 flip chips with the 16-bit chip-to-chip communication circuit (Fig. 2), we designed 1-cm^2 passive MCM carrier with matching bump structures. The bumps are designed with diameter of 15 μm and a pitch of 50 μm. The discontinuities presented by bump interconnects to passive transmission lines are modeled using lumped elements to have a characteristic impedance of 5 Ω. The inductance is calculated using 3D extraction software InductEx [11] and the required capacitance to the ground formed by the transmission line is tuned. The MCM 1-cm^2 carrier is fabricated at Hypres [12]. The MCMs are assembled at Hypres using our epoxy assisted Cu bumps technology [13] with the refined epoxy deposition and conditioning methods allowing precise measurement of epoxy amount and removal of air bubbles from the deposited epoxy.

Tests of all 220 MCM signal bumps, with each signal bump surrounded by four ground ones, show 100% connectivity. These are non-superconductive bumps with resistance ~0.15 Ω. The bumps are able to carry ~150 mA of the current without making the adjacent Nb film resistive. IVCs of Josephson junction arrays measured via MCM carrier

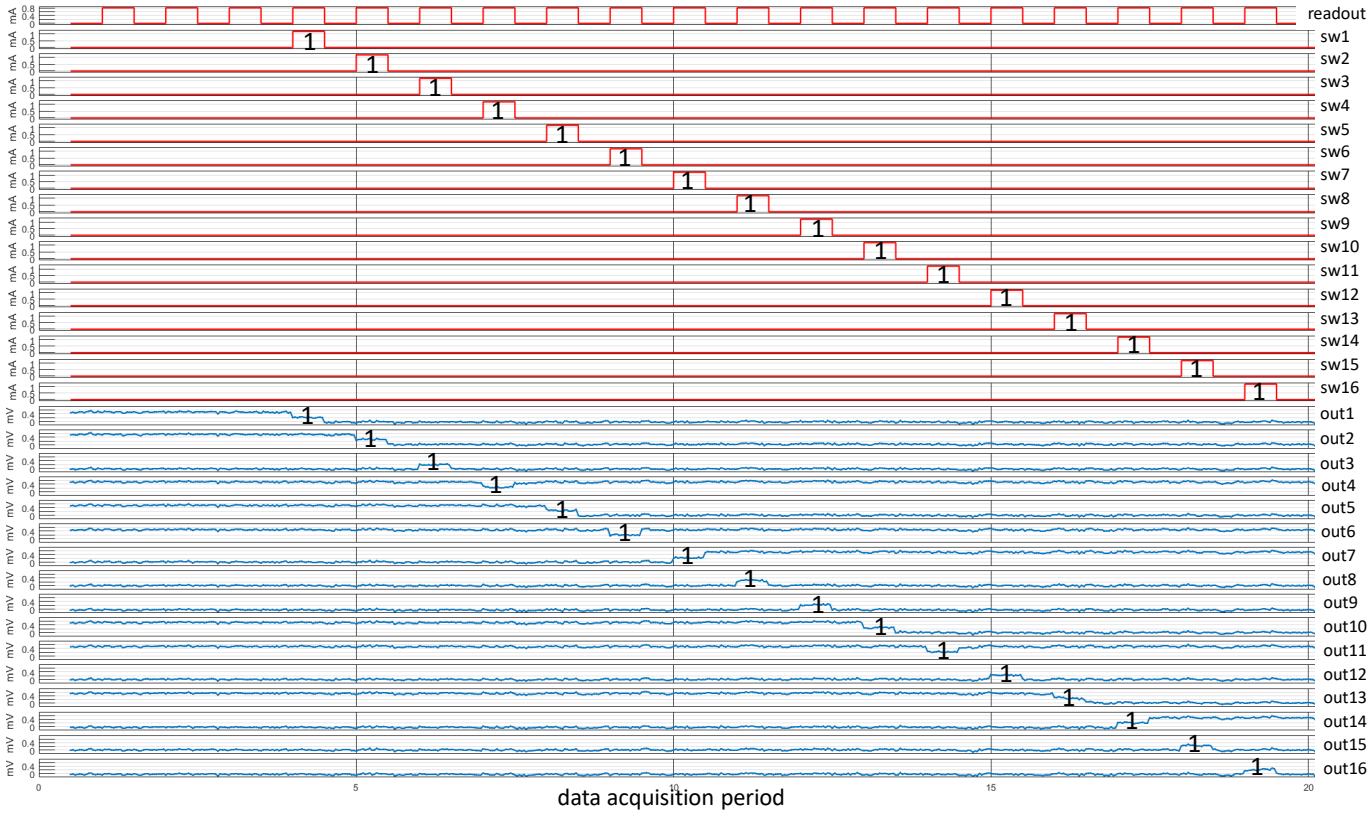

Fig. 4. Correct functional operation of MCM with the ERSFQ 16-bit chip-to-chip communication circuit at 49 GHz clock frequency.

are identical to ones measured directly on the flip-chip. Tx and Rx bias margins for PTLs measured via MCM are comparable to margins for identical PTLs measured on flip-chip showing that our bumps do not affect the integrity of SFQ pulses.

C. MCM with 16-bit Chip-to-Chip Communication Circuit: Functional Low and High Frequency Test

We successfully tested the MCM with the 16-bit communication circuit. Fig. 3 shows the correct functionality of the assembled MCM measured using Octopux. The test pattern includes: (a) a train of pulses to provide SFQ clock; (b) staircase dc current controls (*sw1, sw2, … sw16)* applied to generate sixteen data patterns; (c) three clock outputs: one to monitor integrity of the clock input, and *clk1_out* and *clk2_out*, which are two recovered clocks at the data output side of the chip; (d) sixteen data outputs from the MCM circuit. All outputs are measured via standard toggle flip-flop SFQ/dc converters. The measured output pattern verifies the correct operation for the irregular data pattern sent and is observed on all outputs from *out1* to *out16*. The correct operation is confirmed for this pattern with bias margins ±12%.

In order to perform high-speed test at GHz clock frequencies, we employ a technique similar to one demonstrated in our earlier tests of 8-bit ALU [14] and a 4-to-16 decoder [15]. In this technique, we apply a high-speed clock signal from the high-frequency generator, while the control signals to the data bits are applied at fairly low speed (~2 MHz) from the Octopux. The output data stream is also monitored with the Octopux on the output toggle-type SFQ/dc converters. When the output is "0" with no pulses coming to the SFQ/dc converter, the output will be a static voltage level at either 0 or V_{max} ~ 400 μV. Alternatively, if a high-speed stream of SFQ pulses is coming to the converter, it oscillates at the clock frequency between the two voltage states, resulting in average voltage level of $V_{max}/2$ ~ 200 μV. Therefore, if measured with the Octopux, the "0" will be represented with a line both at 0 or V_{max}, and "1" as a line at $V_{max}/2$. All possible transitions from "0" to "1" and from "1" to "0" (up-up, up-down, down-up and down-down) can be observed depending on the initial state of the output TFF and the number of clock pulses during input switch ON state.

This method is used to test an MCM with the 16-bit chip-to-chip communication circuit at multi-GHz clock frequency. As an example, Fig. 4 shows the correct output patterns for the circuit at clock frequency of 49 GHz. The first trace in Fig. 4 shows the internal Octopux clock at ~2 MHz required for the test patterns to be generated and sent while outputs are being acquired from the chip. Similar to Fig. 3, the next thirty-two traces represent dc current controls applied to generate sixteen data patterns and sixteen data outputs acquired from the MCM. Here the control signals to the switches are applied to the inputs in the staircase pattern, while clock is provided by the room temperature high frequency generator. The measured outputs followed the input pattern with "0" represented either by voltage at 0 or V_{max} and "1" represented by voltage level of $V_{max}/2$ at the outputs. In Fig. 4 voltage scale for all outputs is from 0 to 400 μV. The correct output pattern is observed with bias margins of +/- 8% with average-voltage test. The output DFFs (see Fig. 1b) had a buffer junction preventing forceful push-through data without a clock. In order to provide additional means to separate correct and incorrect behavior, which might look the same in this average-voltage test, an additional switch (marked "through" in Fig. 1b) is introduced in the C-element tree. Deactivation of this switch makes all outputs disappear, proving intended clock recovery function. It is worth noting that the performed test does not provide a bit-error rate (BER) and serves as an estimate of the correct high-speed functionality indicating no permanent error within margins of operation [15, 16]. A more elaborate input data generation, together with testing of the complementary data outputs, would allow BER estimates to be obtained in a similar manner as in [14].

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