Design and Implementation of a 16-Word by 1-Bit Register File Using Adiabatic Quantum Flux Parametron Logic

N. Tsuji[1], C. L. Ayala[2], N. Takeuchi[2], T. Ortlepp[3], Y. Yamanashi[1], and N. Yoshikawa[1]

[1]Department of Electrical and Computer Engineering, Yokohama National University, Yokohama 240-8501, Japan
[2]Institute of Advanced Sciences, Yokohama National University, Yokohama 240-8501, Japan
[3]CiS Research Institute for Microsensor Systems GmbH, 99099 Erfurt, Germany

E-mail: tsuji-naoki-yz@ynu.jp

***Abstract*—We have been developing extremely energy-efficient microprocessors using the adiabatic quantum flux parametron (AQFP) logic. In this study, we designed and fabricated an AQFP register file, which is one of the key building blocks in the microprocessor. The 16-word by 1-bit register file with dual output ports and a single input port was designed by using an AQFP cell library with a minimalist design. The circuit is composed of three decoders and feedback delay latches (D-latches), which are clocked by four-phase excitation currents. The circuits were fabricated using the AIST 10 kA/cm^2 Nb process. The total junction number and circuit area are 2544 and 3.1 mm × 5.4 mm, respectively. The estimated energy consumption is 18 aJ per clock cycle for 5 GHz operation. The latency is 1600 ps for 5 GHz operation. In the low-speed test, we confirmed the correct operations across 15 addresses.**

***Keywords (Index Terms)*— Superconducting circuits, QFP, adiabatic logic, latch, register file.**

IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), January 2017.
Received September 18, 2016; Selected October 7, 2016. Reference ST553; Category 4.
Preprint of ASC 2016 manuscript 1EOr2B-03 submitted to *IEEE Trans. Appl. Supercond.* for possible publication.
DOI: 10.1109/TASC.2017.2656128.