Design and High-speed Demonstration of an SFQ Complex Event Detector Circuit for Complex Event Processing

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***Abstract*— Recently, many investigations are conducted for processing the big data. One is known as complex event processing (CEP), which is real time processing to extract meaningful information from an input data stream. High-speed real-time processing is essential in the CEP system. One potential application of the CEP system is for a network intrusion detection system (NIDS). The NIDS monitors packet data streams in the network, and detects packets that contain viruses by performing pattern matching between input data and virus patterns.**

A complex event detector (CED) circuit is a key component in the CEP system, which performs pattern matching between an input data stream and compared n-bit data patterns called "symbol". The symbol is usually represented by 8-bit data in NIDS. In this study, we develop a CED circuit using single-flux-quantum (SFQ) circuits, which operate at very high speed with extremely low power consumption.

In our design, input data is compared with a symbol stored in 1-symbol matching circuit. CED circuits for detecting multiple symbols are designed by connecting the 1-symbol matching circuits in series. This architecture enables the scalability of the CED circuit when extending the symbol length. We designed and implemented an 8-bit 4-symbol SFQ CED circuit using the AIST ADP2 Nb process. The correct operation was confirmed at 52.1 GHz by on-chip high-speed measurements.

Acknowledgment

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2).

***Keywords (Index Terms)*— Big data processing, complex event processing, CEP, real-time processing, data stream, network intrusion detector system, NIDS, pattern matching.**

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