Energy-Efficient and Compact ERSFQ Decoder for Cryogenic RAM

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***Abstract*—We report on the development of energy-efficient decoders for cryogenic random access memory and register file. To reduce the pitch, area, and energy, our decoder employs a scalable binary tree architecture. We implemented these decoders using ERSFQ logic controlled by magnetically coupled address lines. These lines are driven by energy-efficient drivers based on the current-stirring technique. A 4-to-16 version of the decoder was laid out and fabricated in HYPRES 6-layer 10 kA/cm^2 and MIT LL 8-layer 10 kA/cm^2 processes with 15 μm and 28 μm decoder row pitch, respectively. The decoders were designed to have ~ 30 ps latency and dissipate ~ 40 aJ per clock. We experimentally confirmed the functionality of the circuits with ±8% dc bias margins and verified its operation up to 13 GHz clock.**

***Keywords (Index Terms)*— Energy-efficient logic, decoder, random access memory, cryogenic magnetic memory, ERSFQ, RSFQ, SFQ.**

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