

64-kb Hybrid Josephson-CMOS 4 Kelvin RAM with 400 ps Access Time and 12 mW Read Power

Theodore Van Duzer, Life Fellow, IEEE, Lizhen Zheng, Member, IEEE, Stephen R. Whiteley, Member, IEEE, Hoki Kim, Jaewoo Kim, Xiaofan Meng, and Thomas Ortlepp

Abstract - We have designed, simulated, fabricated and tested a 64-kb hybrid Josephson-CMOS memory using a 5 mm x 5 mm Josephson interface chip and a 2.0 mm x 1.5 mm CMOS chip. The Josephson chip uses the Hypres 4.5 kA/cm² niobium technology and the CMOS chip is made using the TSMC 65 nm technology. The chips are connected using short wire bonds in a piggy-back package. The chip sizes and pad layouts have been constrained to allow testing in our wideband American Cryoprobe Model BCP-2 test probe in order to measure ultra-short delays. The test signals of 5 mV amplitude are chosen to represent the signals that would be supplied to the memory in a digital computing or signal processing system. Each input signal is first amplified in a four-junction logic (4JL) gate driving a Suzuki stack, which, in turn, drives a highly sensitive CMOS comparator that raises the signal to volt level. Such amplifiers are provided for the address, data, read and write inputs to the CMOS memory. Output currents from the memory cells are detected by ultra-fast 4JL gates providing 5 mV output signals; an equivalent arrangement was used for the delay tests. The overall read delay is the access time, which we find to be about 400 ps. We extrapolate from the measured and calculated power dissipation in this partially accessed 64-kb memory to a fully accessed 64-kb memory and find the expected overall read power dissipation to be about 12 mW for operation at 1 GHz.

Keywords - Hybrid memory, access time, high-speed interface, 4 K CMOS

IEEE/CSC & ESAS European Superconductivity News Forum (ESNF) No. 22 October/November 2012. ESNF Reference No.ST320 Category 4.

The published version of this preprint appeared in *IEEE Transactions on Applied Superconductivity* 23, 1700504 (June 2013).