Design, Implementation, and On-Chip High-Speed Test of an SFQ Half-Precision Floating-Point Adder

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Abstract—We are developing a large-scale reconfigurable data-path (LSRDP) based on single-flux-quantum (SFQ) circuits to establish a fundamental technology for future high-performance computing systems. In the LSRDP, an SFQ floating-point adder (FPA) is one of the main circuit blocks as well as one of the most complicated circuit blocks. In the present paper, we designed and implemented an SFQ half-precision FPA and carried out on-chip high-speed tests. The data format of the half-decision FPA obeys the IEEE standard, in which two input data streams, an 11-bit significand and a 6-bit sign/exponent, are processed bit-serially. Floating-point addition is performed in three steps: (1) alignment and rounding of significands, (2) addition/subtraction of the significands, and (3) normalization of the result. We implemented an SFQ half-precision FPA using the SRL 2.5 kA/cm^2 niobium standard process. The size, power consumption, and total junction number are 5.86 mm × 5.72 mm, 3.5 mW, and 10,224, respectively. The simulated DC bias margin is ±20% at 20 GHz, which corresponds to the performance of 1.67 GFLOPS. We successfully confirmed the correct operation of the FPA, except for a read-out circuit for the significand, at 24 GHz by on-chip high-speed tests.

Index Terms—SFQ circuits, superconducting integrated circuits, LSRDP, floating-point adder, shifter, normalizer

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