Adiabatic Quantum-Flux-Parametron Logic with Extremely Low Power Consumption

Nobuyuki Yoshikawa

Department of Electrical and Computer Engineering, Yokohama National University
Hodogaya, Yokohama 240-8501, Japan

March 20, 2013(HP55). This highlight was solicited by ESNF, because of the high importance of energy-efficient computing.

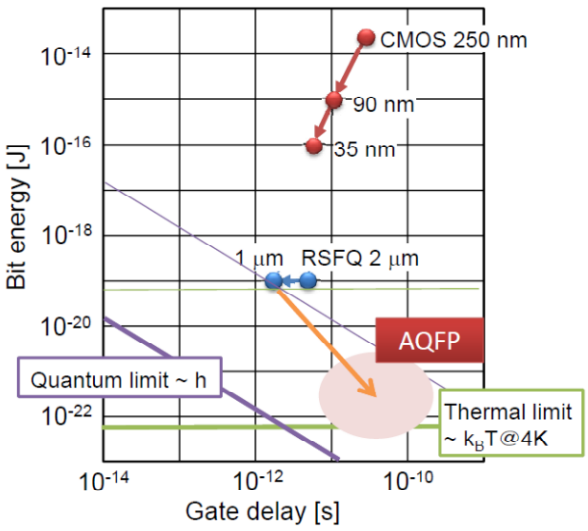

Fig.1. Bit energy and gate delay of AQFP, RSFQ and CMOS gates.

Energy efficiency of logic circuits is the most important metric nowadays, because the power consumption limits the performance of recent digital systems, such as computers, servers and routers. Some estimations show that the power consumption of an exascale computer based on CMOS devices will exceed 100 MW and there is no effective solution to reduce it even assuming future CMOS devices. Superconducting logic is a promising technology, and a lot of energy efficient logic circuits are proposed and developed actively at the moment. Our group in Yokohama National University recently reported several papers concerning ultra-low-power logic using adiabatic quantum flux parametron (AQFP), which enables us to approach the lowest energy limit in computation [1]-[6].

Our intention is to reduce the dynamic energy consumption of nonhysteretic quantum flux parametrons (QFPs) by operating them slowly or adiabatically. Figure 1 is a comparison of bit energies and gate delays between AQFP, RSFQ and CMOS logic gates, which shows AQFP logic gates have more than five orders of magnitude of advantage in terms of the bit energy comparing to conventional CMOS logic gates.

In our first paper [1], we have investigated the circuit parameter condition of QFPs in the adiabatic operation mode. We evaluated the dynamic energy dissipation of AQFPs in circuit simulation and found that it can be reduced to a level much lower than that of RSFQ circuits.

In our second paper [2], we measured energy dissipation of an AQFP gate using a superconducting

resonator-based method, by which the bit energy of the AQFP gate was estimated to be 10 zJ for 5 GHz operation. This value is about five orders of magnitude smaller than that of state-of-the-art CMOS logic gates.

In our third paper [3], we investigated the relationship among circuit parameters of AQFP gates, the bit energy and the robustness through circuit simulation. We also calculated the bit-error-rate of AQFP gates at finite temperatures and showed that the AQFP gates operate correctly even for the bit energy approaching $k_B T$.

In our fourth paper [4], we designed and implemented a 1-bit AQFP full adder and examined its operation through simulations and experiments. Figure 2 show a micrograph of the 1-bit AQFP full adder. The measurement results indicated that the 1-bit AQFP full adder has a wide current bias margin of as large as about plus/minus 28%.

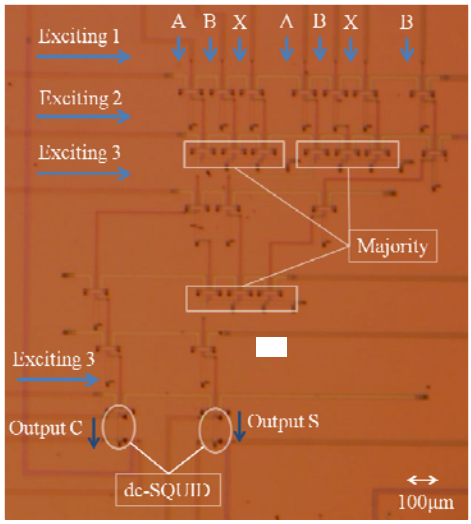

Fig. 2. Micrograph of an 1-bit AQFP full adder fabricated by using the ISTEC standard process.

In our fifth paper [5], we proposed an energy-recoverable on-chip AC power source to drive AQFP gates. We designed and fabricated the on-chip AC power source and demonstrated its correct operation at an oscillation frequency of 4.4 GHz. Recently we successfully confirmed the operation of AQFQ gate driven by the on-chip AC power source. The results will be published soon [6].

Through our recent results, we believe that we could stimulate a new paradigm of superconducting digital electronics, which makes it possible to realize digital systems with extremely high-energy efficiency.

[1] N. Takeuchi, D. Ozawa, Y. Yamanashi and N. Yoshikawa, "Adiabatic quantum flux parametron as an ultra-low-power logic device," *Supercond. Sci. Tech.*, **26**, 035010 (2013).

[2] N. Takeuchi, Y. Yamanashi and N. Yoshikawa, "Measurement of 10 zJ energy dissipation of adiabatic quantum-flux-parametron logic using a superconducting resonator," *Appl. Phys. Lett.*, **102**, 052602 (2013).

[3] N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi and N. Yoshikawa, "Margin and Energy Dissipation of Adiabatic Quantum-Flux-Parametron Logic at Finite Temperature," *IEEE Trans. Appl. Supercond.*, **23**, 1700304 (2013).

[4] K. Inoue, N. Takeuchi, K. Ehara, Y. Yamanashi, and N. Yoshikawa, "Simulation and Experimental Demonstration of Logic Circuits Using an Ultra-low-power Adiabatic Quantum-flux-parametron," *IEEE Trans. Appl. Supercond.*, **23** 1301105 (2013).

[5] T. Mukaiyama, N. Takeuchi, Y. Yamanashi and N. Yoshikawa, “Design and Demonstration of an On-chip AC Power Source for Adiabatic Quantum-Flux-Parametron Logic,” *Supercond. Sci. Tech.*, **26**, 035018 (2013).

[6] T. Mukaiyama, N. Takeuchi, Y. Yamanashi and N. Yoshikawa, “Operation of an Adiabatic Quantum-Flux-Parametron Gate Using an On-chip AC Power Source,” *IEEE Trans. Appl. Supercond.*, **23** (2013), *in press*.