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Plenary presentation 2-KN given at ISEC, 28 July-1 August 2019, Riverside, USA.

YNU Initiative for Global Arts & Sciences
YOKOHAMA National University

ISEC 2019
July 28 – August 1, 2018, Riverside, CA

Superconducting computing: present status and perspectives

Nobuyuki Yoshikawa

1) Graduate School of Engineering

2) Institute of Advance Science

Yokohama National University, Japan

Extended Abstracts of

1987 INTERNATIONAL SUPERCONDUCTIVITY ELECTRONICS CONFERENCE (ISEC '87)

AUGUST 28–29, 1987
KENCHIKU-KAIKAN HALL
5-26-20 Shiba, Minato-ku
TOKYO, JAPAN

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SESSION-IX: Digital and Analog Circuits-II

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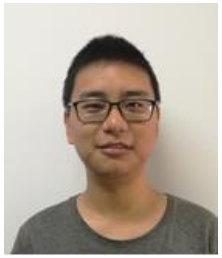
Members in the research unit on “Extremely Energy-Efficient Processors”









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Outlines of This Talk

- Background and motivation
- Past and present status of superconducting digital electronics
- Operation principles of AQFP circuits
- AQFP as a logic circuit
- Recent research activities on AQFP circuits
- Future directions
  - Josephson/CMOS hybrid memories
  - Reversible logic circuits
- Summary

Background

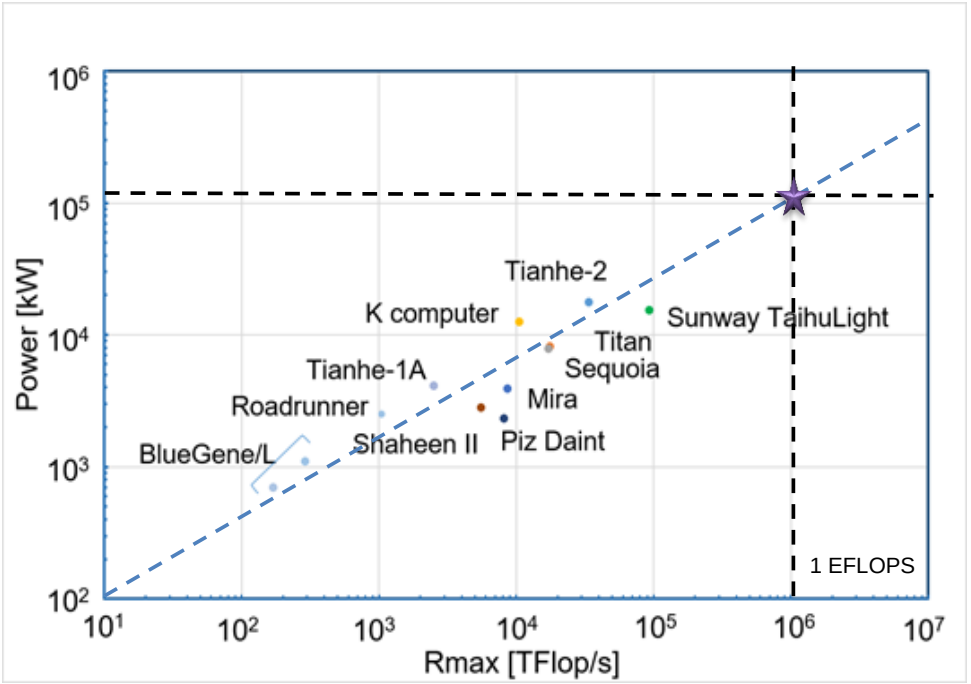
Estimated power consumption to realize an exa-scale computer

> 100 MW
~ $million/100 MW per year

K computer (Japan)

Peak performance: 10.5 PFLOPS
Power consumption: 12.6 MW

1st-ranked computers in recent TOP500



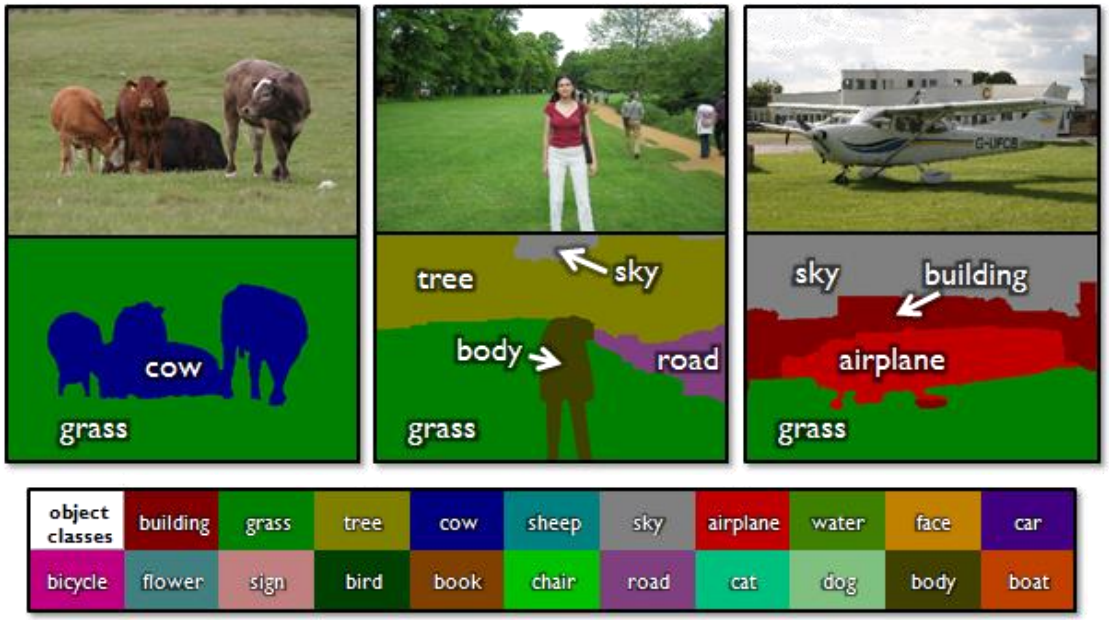
http://www.top500.org/

Low-Power Logic Devices is highly demanded.

AI is Power Hungry

https://www.nvidia.com/en-us/titan/titan-xp/

Example of Semantic Segmentation



http://jamie.shotton.org/work/research.html

input size: 513 x 513
Flops: 346 GFLOPS

https://github.com/albanie/convnet-burden

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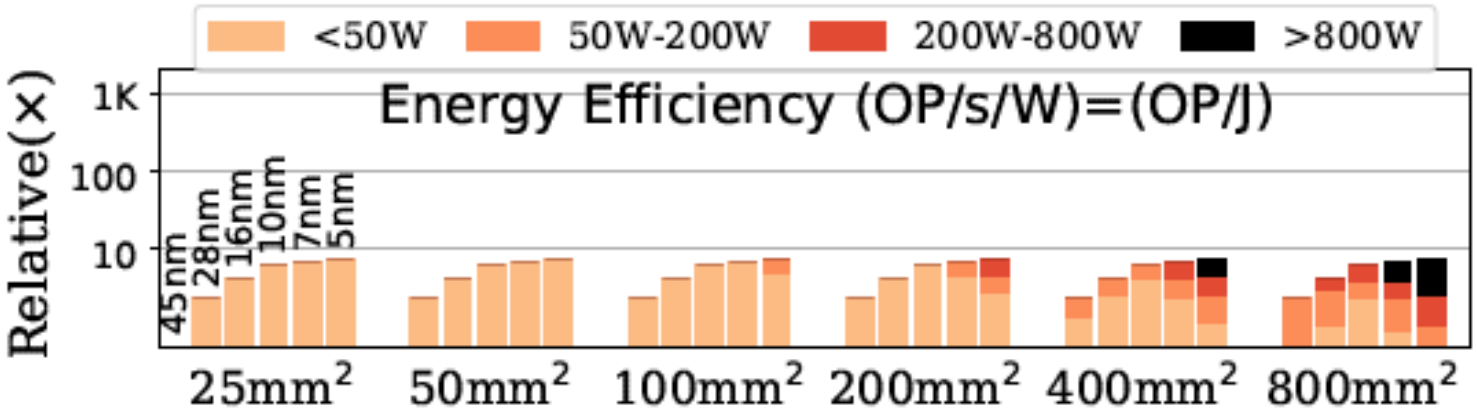
Energy Efficiency of CMOS Chips

Energy efficiency of CMOS chips for different CMOS nodes and die sizes

f_{chip} = 1 GHz



Normalized to 25 mm^2 chip fabricated with 45 nm CMOS

A. Fuchs and D. Wentzlaff, "The Accelerator Wall: Limits of Chip-Specialization," *the 25th IEEE International Symposium on High-Performance Computer Architecture (HPCA '19)*, 2019.

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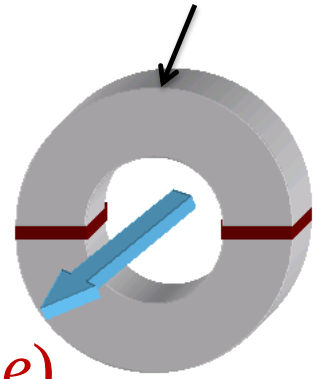
Single-Flux-Quantum (SFQ) Circuits

SFQ circuits

Superconducting loop
with Josephson junctions

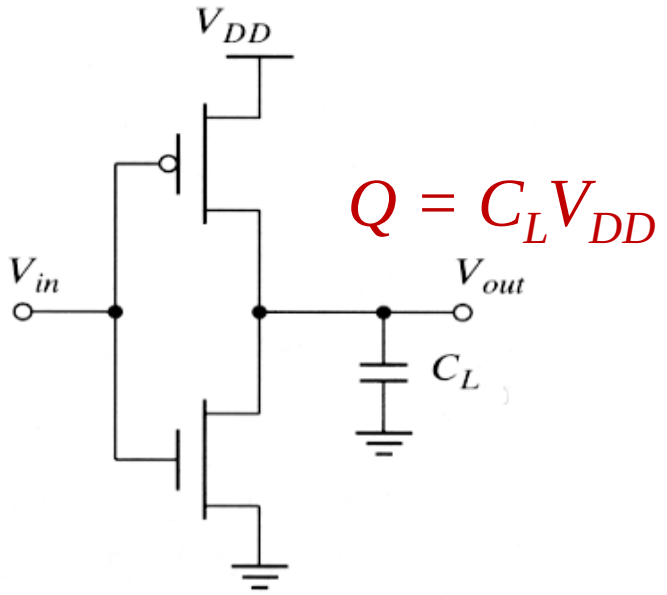


$\Phi_0 = h/(2e)$

Switching energy

$E = \Phi_0 I_c \sim 10^{-19}$ J

CMOS circuits

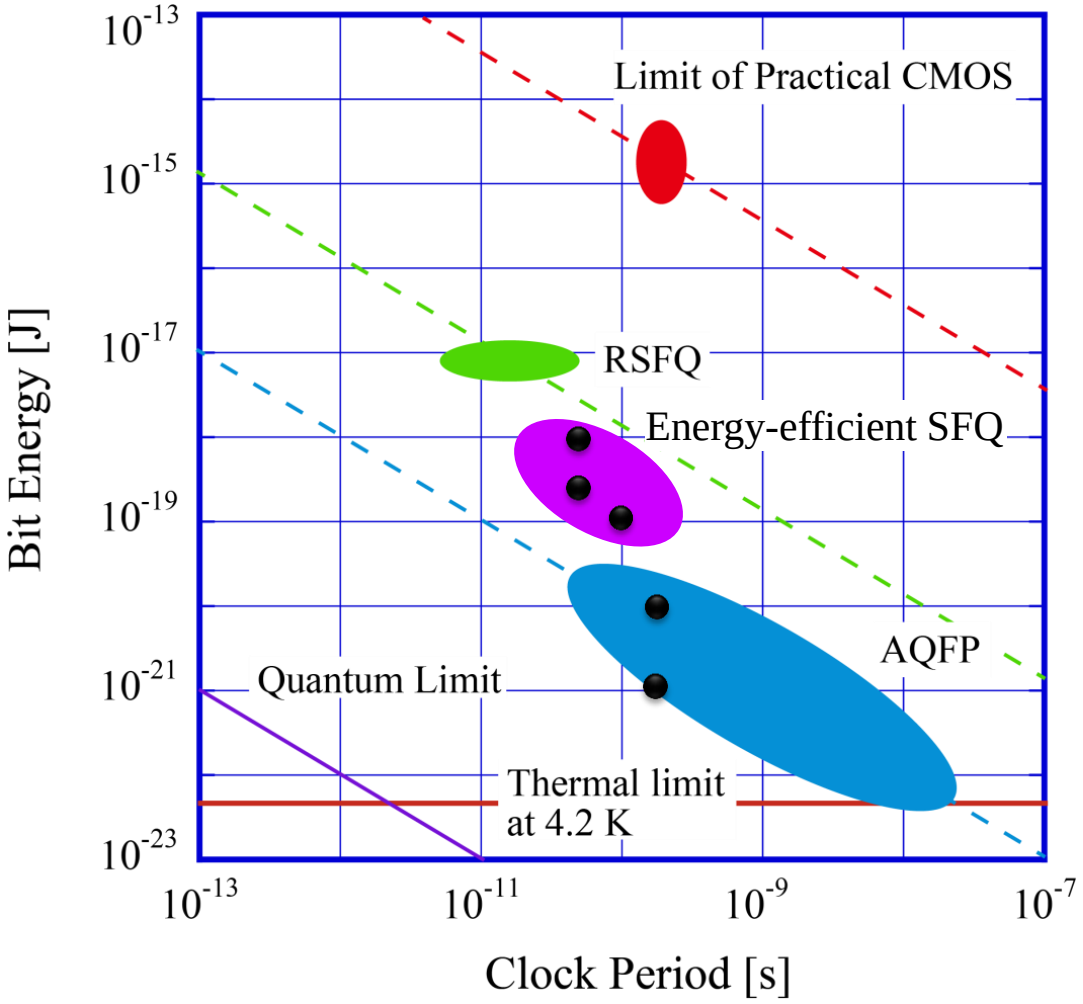


$Q = C_L V_{DD}$

Switching energy

$E = QV_{DD} \sim 10^{-16}$ J

Comparison of Energy-Delay Product



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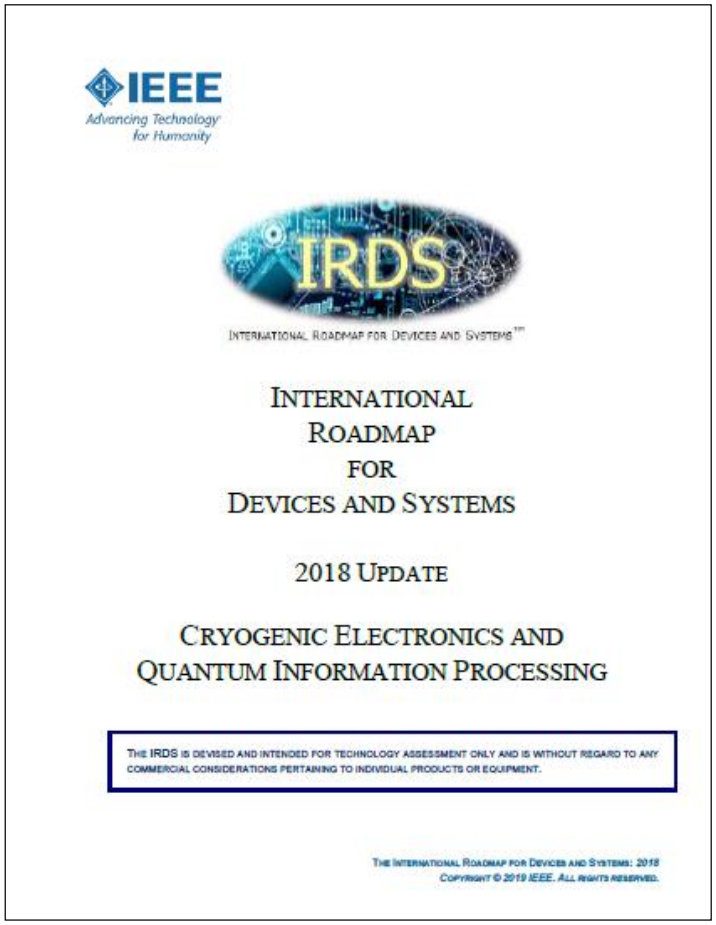
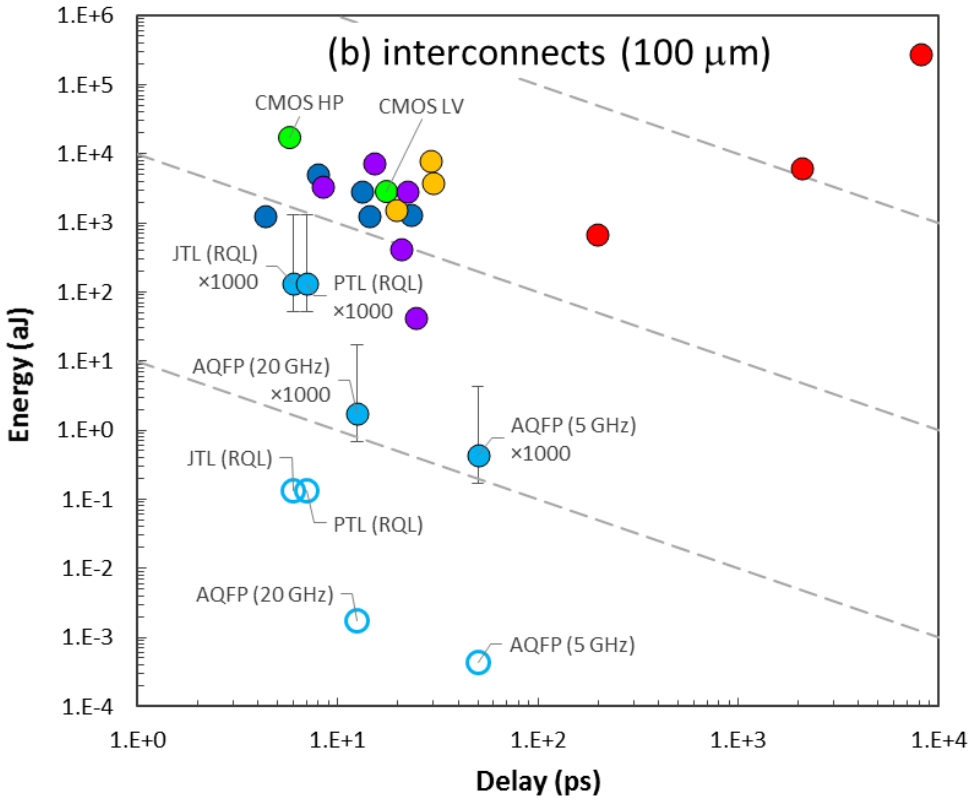
IRDS
(International Roadmap for Device and Systems)





Energy and delay of gates with 100 μm interconnection length

Available at https://irds.ieee.org/editions/2018

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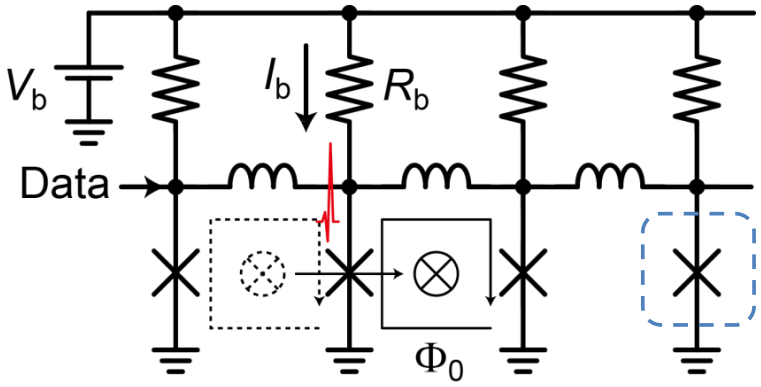
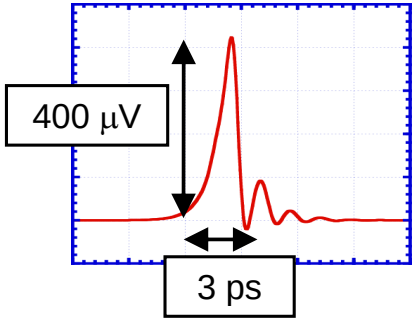
Rapid Single-Flux-Quantum (RSFQ) Circuits

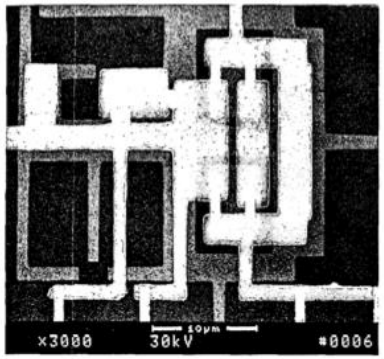


Josephson junction



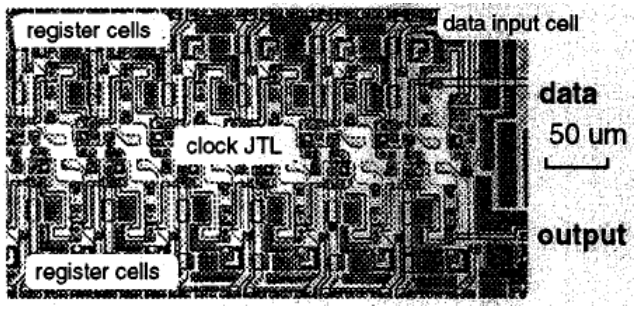
- Pulse height ~ 400 μV
- Pulse width ~ 3 ps
- Power ~ nW/gate

K. K. Likharev, V. K. Semenov, *IEEE Trans. Appl. Supercond.* 1, 3–28 (1991).



T Flip-flop operating at up to 770 GHz.

W. Chen *et al.*, *IEEE Trans. Appl. Supercond.* 9, 3212–3215 (1999).



256-b shift register operating at 12 GHz

O. Mukhanov *et al.*, *IEEE Trans. Appl. Supercond 3*, 2578-2581 (1993).

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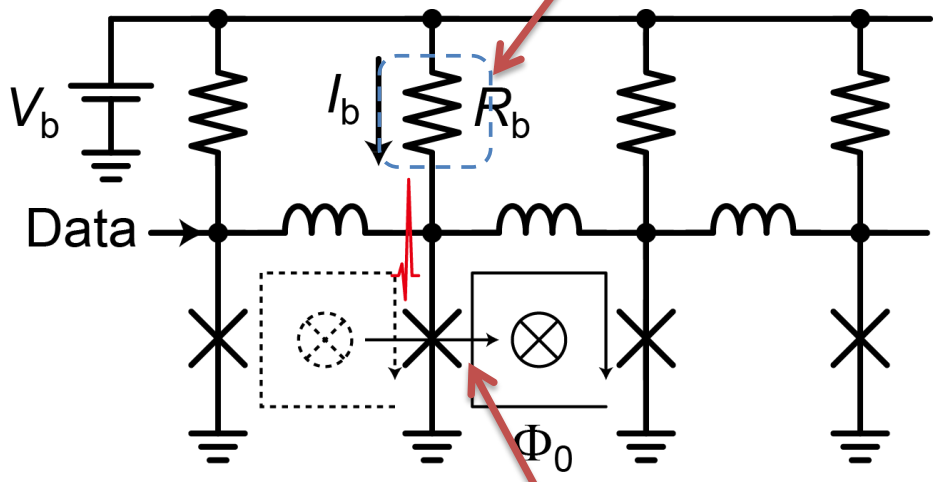
Power Consumption in RSFQ Logic

Static power dissipation:

$$P_S = R_b I_c^2$$



$$P_D \sim P_S/20$$

Dynamic power dissipation:

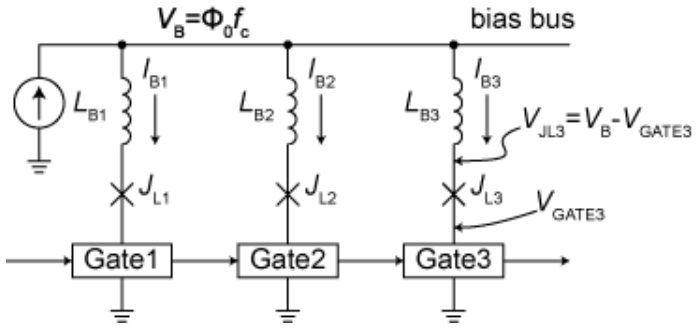
$$P_D = \Phi_0 I_c f$$

Reduction of static power is required.

Energy-Efficient SFQ Circuits

DC Powered

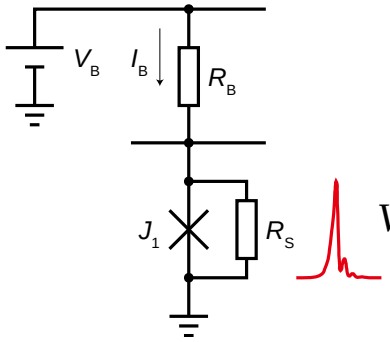
ERSFQ (Hypres)



$P_S \sim P_D \sim I_c\Phi_0 f$

O. A. Mukhanov, *IEEE Trans. Appl. Supercond.* **21**, 760 (2011).

LV-SFQ (Nagoya Univ.)



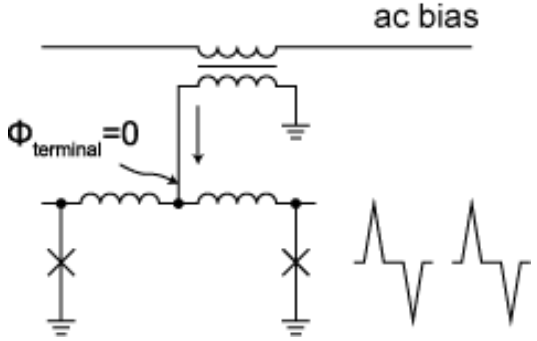
$P_S \sim 5P_D, \; P_D \sim I_c\Phi_0 f$

$$V=\frac{\Phi_0}{2\pi}\frac{d\varphi}{dt}$$

M. Tanaka *et al*. *JJAP* **5** 1053102 (2012)

AC Powered

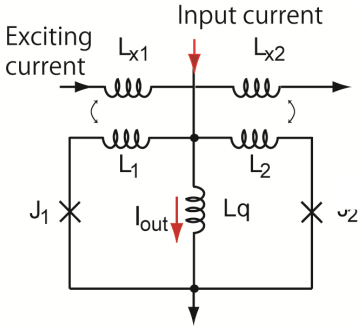
RQL (Northrop Grumman)



$P_S \sim 0, \; P_D \sim I_c\Phi_0 f$

Q. P. Herr *et al.*, *J. Appl. Phys.* **109**, 103903 (2011).

AQFP (Yokohama National Univ.)



$P_S \sim 0, \; P_D < I_c\Phi_0 f$

N. Takeuchi, *et. al*., *SUST*, 26, 035010 (2013).

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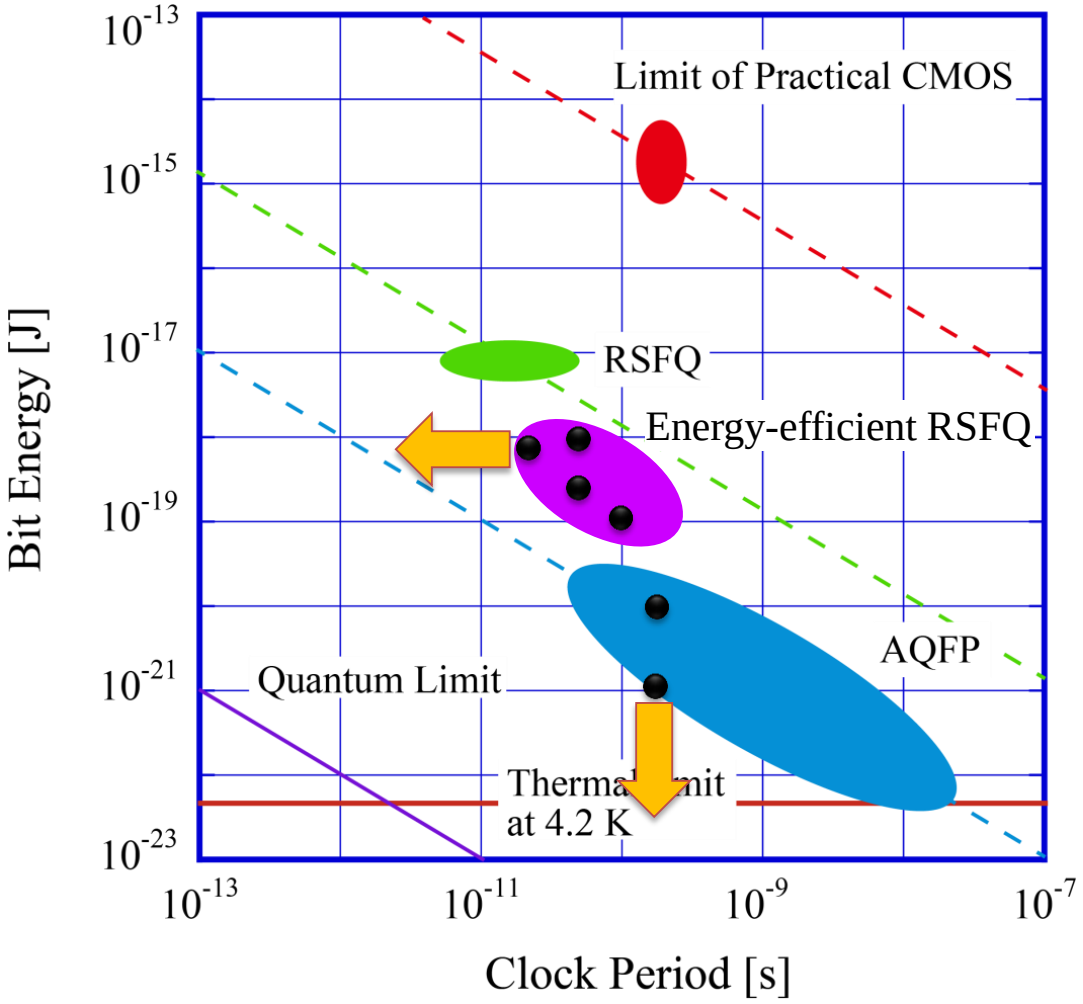
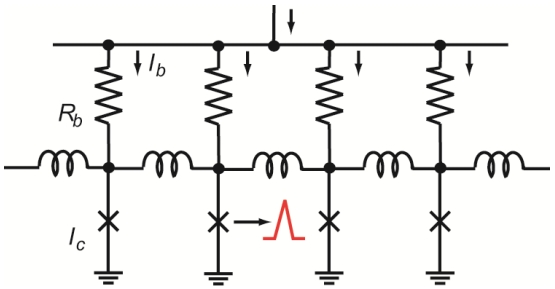
Comparison of Energy-Delay Product



Two Options in SC Digital Electronics

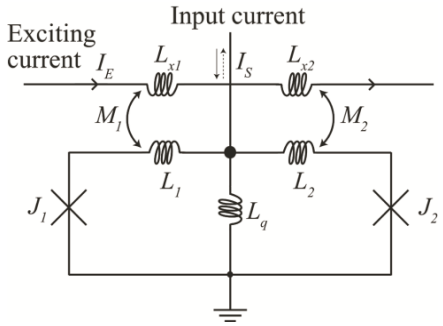
SFQ Logic

- Extremely high throughput
  - 50 GHz ~ 100 GHz frequency
  - RSFQ, ERSFQ, LVSFQ, RQL



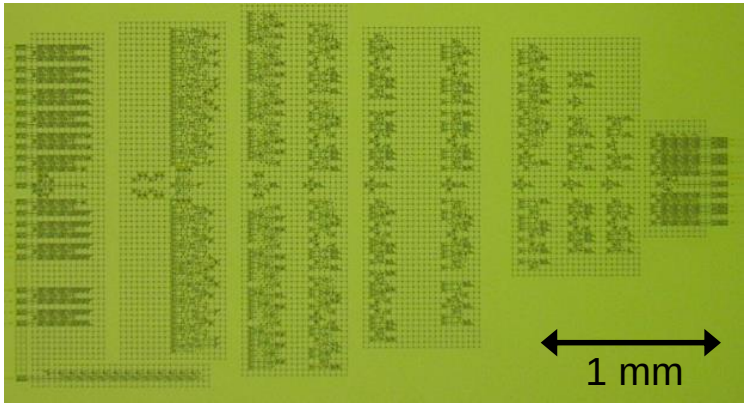
Adiabatic QFP Logic

- Extremely high energy efficiency
  - 1~10 zJ/operation

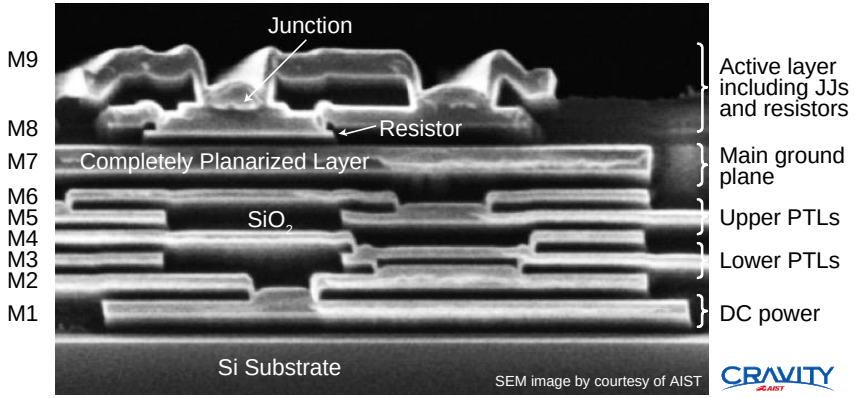


Combination of these two logic circuits brings about high-performance digital systems.

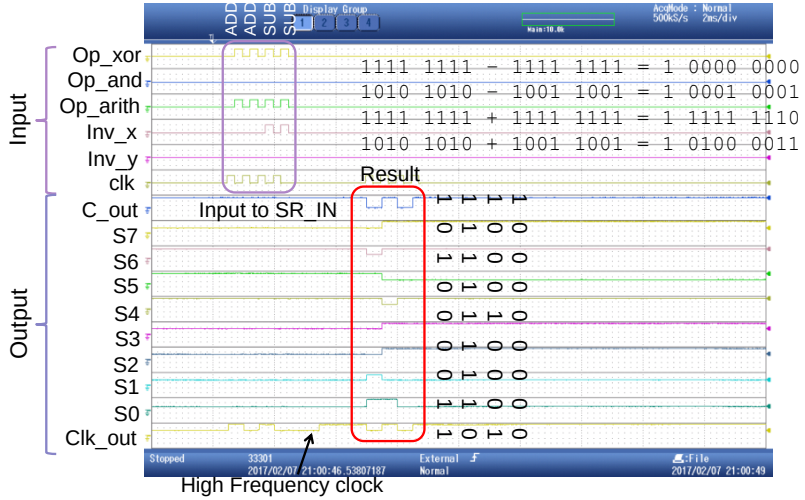
56-GHz Demonstration of Gate-Level-Pipelined, Bit-Parallel ALU

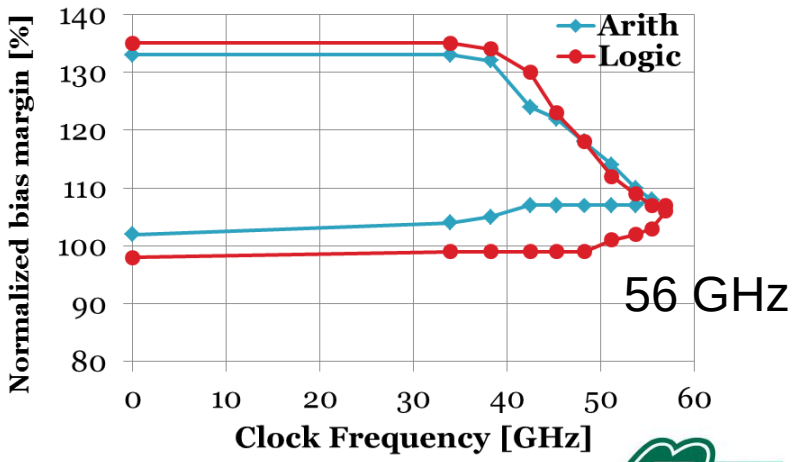


7348 junctions, 3.93 × 2.07 mm²



S. Nagasawa et al. *IEICE Trans. Electron.* **E97-C** (2014) 132–140.





M. Tanaka et al. ISLPED 2017 Design Contest Honorable Mention Award, Taipei

NAGOYA UNIVERSITY

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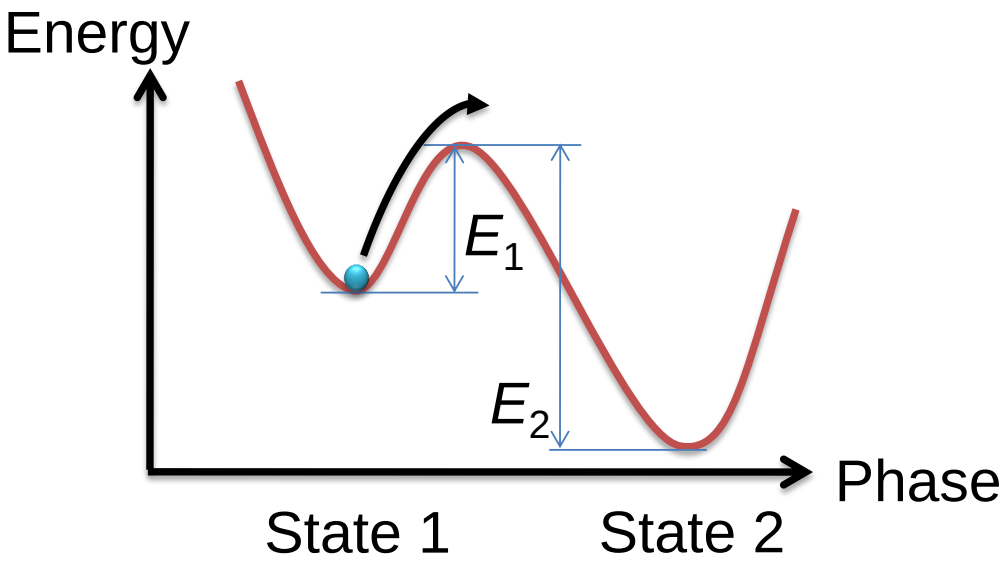
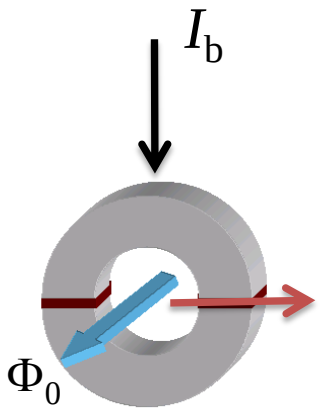
- AQFP as a logic circuit
- Recent research activities on AQFP circuits
- Future directions
  - Josephson/CMOS hybrid memories
  - Reversible logic circuits
- Summary

Energy Potential of RSFQ Circuits





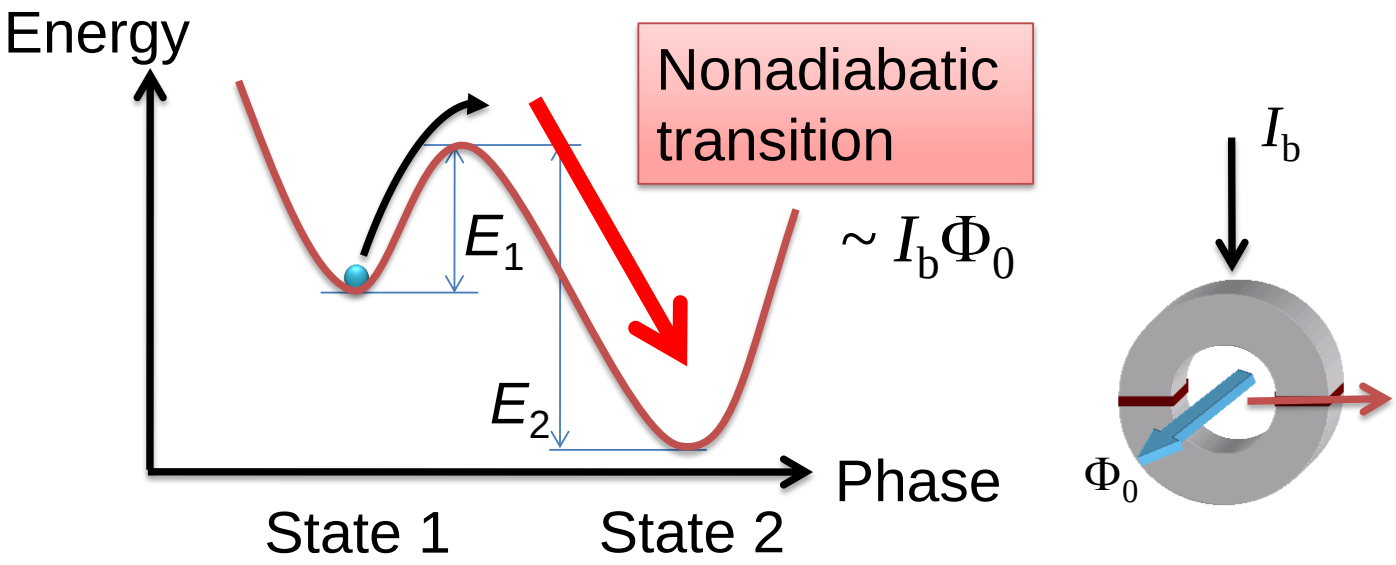
Input energy: E_1
Output energy: E_2

Energy dissipation: E_2

Requirement for the reduction of switching errors

$E_1 > 100\ k_B T$

Energy Potential of RSFQ Circuits



Adiabatic operation of the system is required for energy-efficient computing.

Quantum Flux Parametron (QFP)

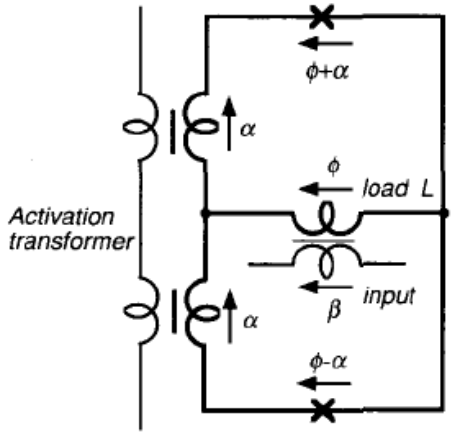


Fig. 1. The basic model of a simple QFP. It consists of two *rf*-SQUID's which share the same inductive load L.

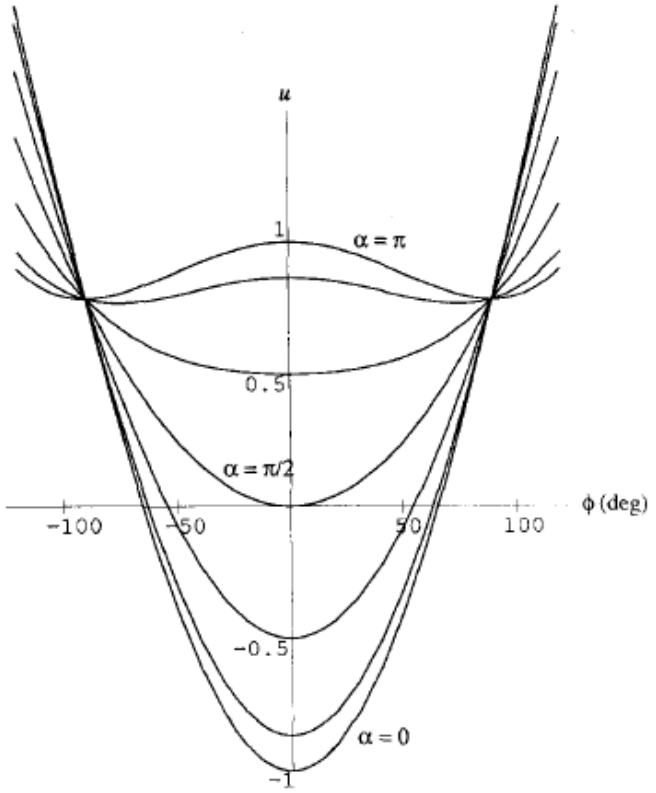


Fig. 2. The normalized Hamiltonian of the basic model shown in Fig. 1. With increasing the activation, bistable states appear. It is possible to choose either stable state by applying a small input.

E. Goto, Proc. 1st RIKEN Symp. Josephson Electronics, pp. 48-51 (1984).

M. Hosoya et al., *IEEE Trans. Appl. Supercond*. 1, 77–89 (1991).

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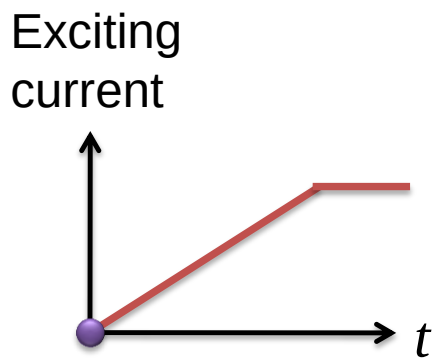
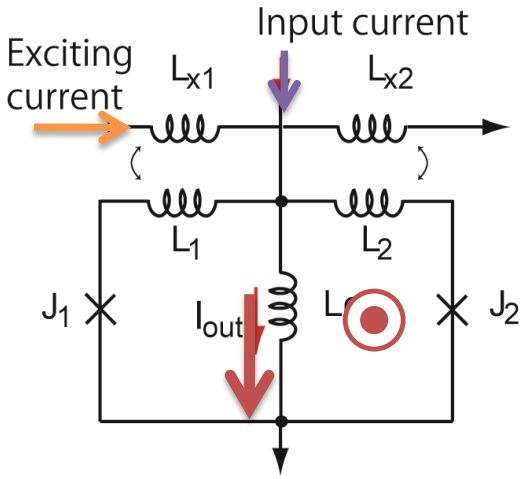
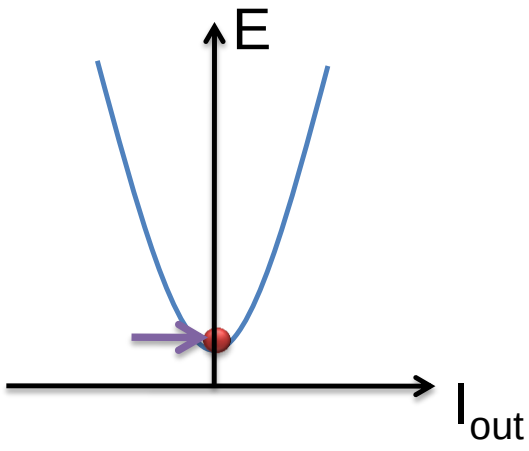
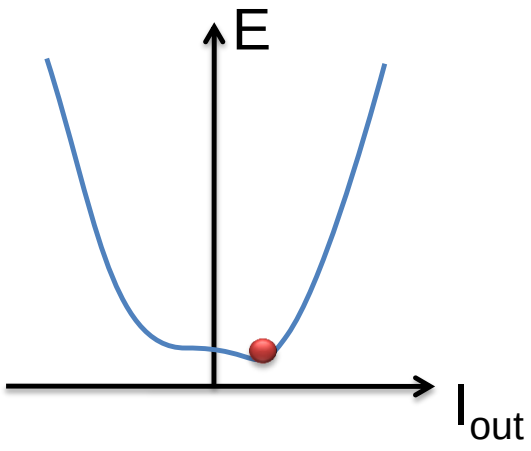
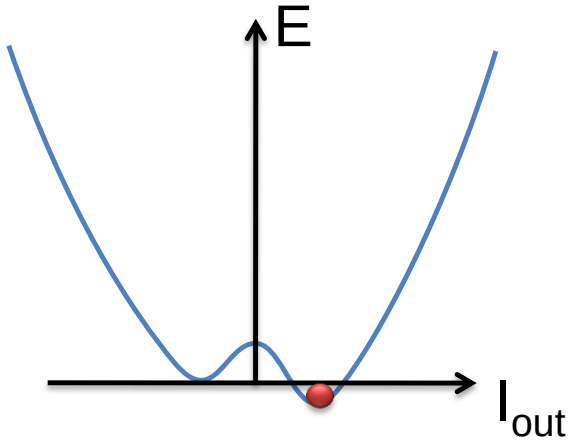
Operation Principle of Quantum Flux Parametron (QFP)





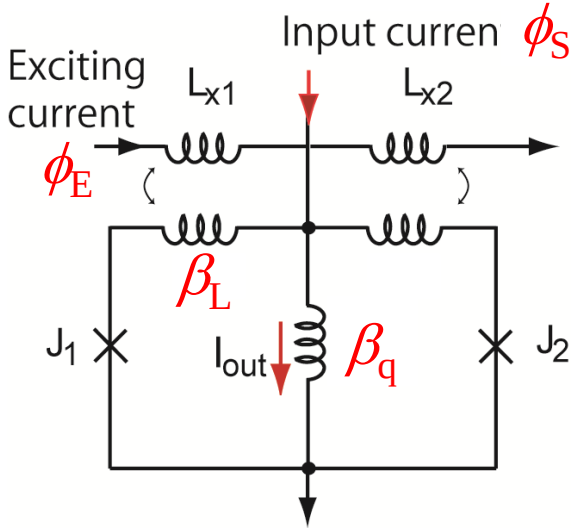






E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984*.

Potential Energy of QFP



$$U_{qfp} = E_j \left[\frac{(\phi_E - \phi_-)^2}{\beta_L} + \frac{(\phi_S - \phi_+)^2}{\beta_L + 2\beta_q} - 2\cos\phi_- \cos\phi_+ \right]$$

Normalized exciting current $\phi_E = 2\pi \frac{M_1 I_E}{\Phi_0}$,

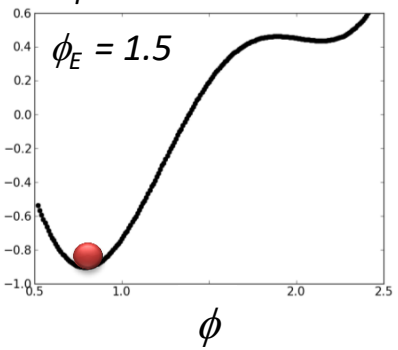
Normalized input current $\phi_S = 2\pi \frac{L_q I_S}{\Phi_0}$

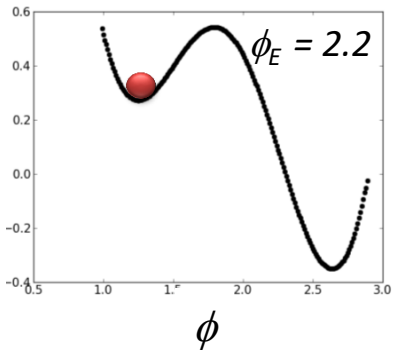
Normalized loop inductance $\beta_L = 2\pi \frac{L_1 I_0}{\Phi_0}$,

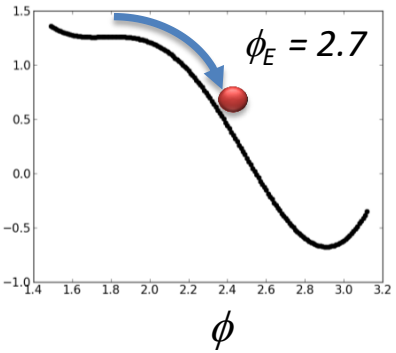
Normalized output inductance $\beta_q = 2\pi \frac{L_q I_0}{\Phi_0}$

$$E_j = \frac{E_J}{2\pi} = \frac{I_0 \Phi_0}{2\pi}, \quad \phi_+ = \frac{\phi_1 + \phi_2}{2}, \quad \phi_- = \frac{\phi_1 - \phi_2}{2}$$

◆ $(\beta_L , \beta_q) = (1.0, 3.0)$



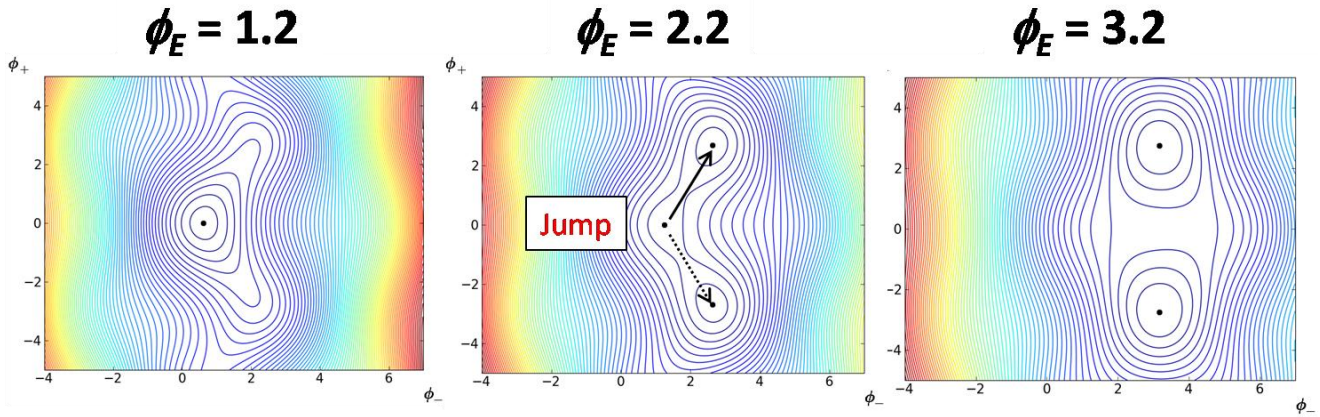




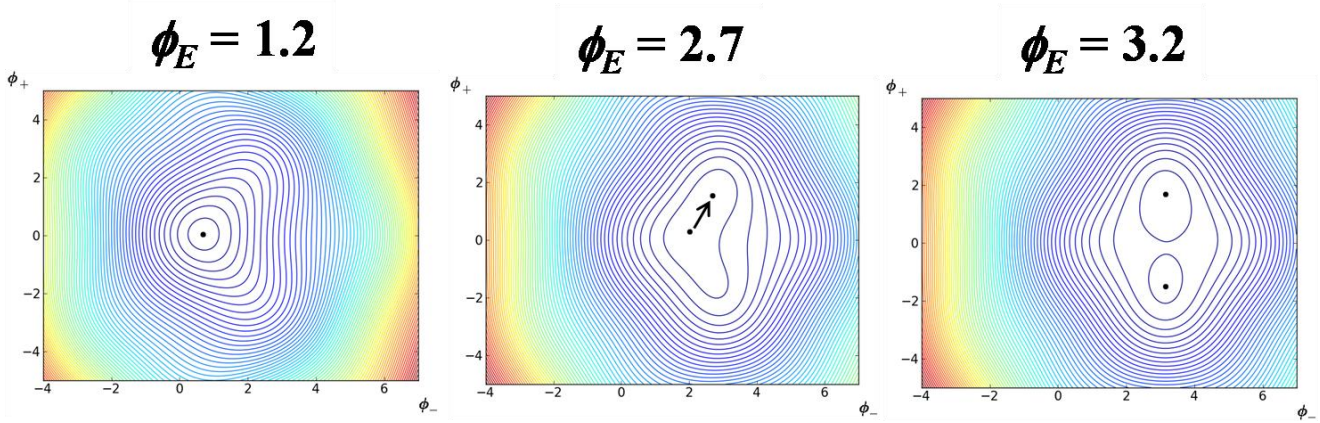
M. Hosoya et al, *IEEE Trans. Appl. Supercond.* vol. 1, 1991, pp. 77 – 89.

QFP in Nonadiabatic and Adiabatic Modes

Non-adiabatic-mode QFP ◆ $(\beta_L , \beta_q) = (1.0, 3.0)$



Adiabatic-mode QFP ◆ $(\beta_L , \beta_q) = (0.8, 0.4)$



N. Takeuchi, *et. a*l., *SUST*, 26, 035010 (2013).

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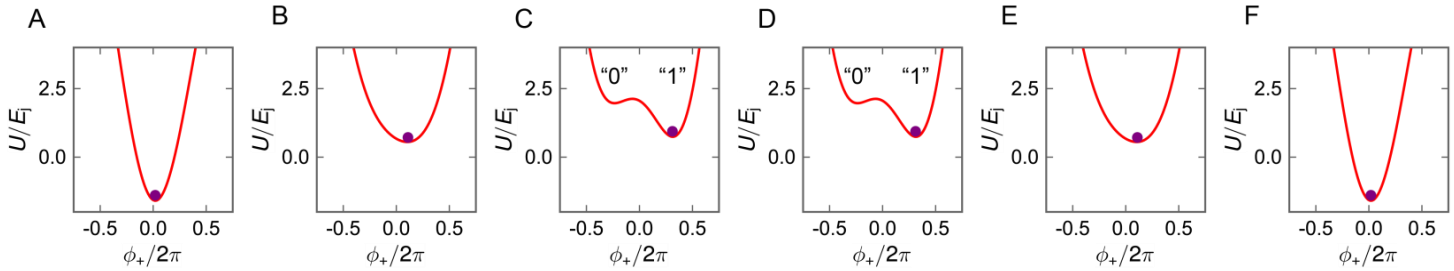
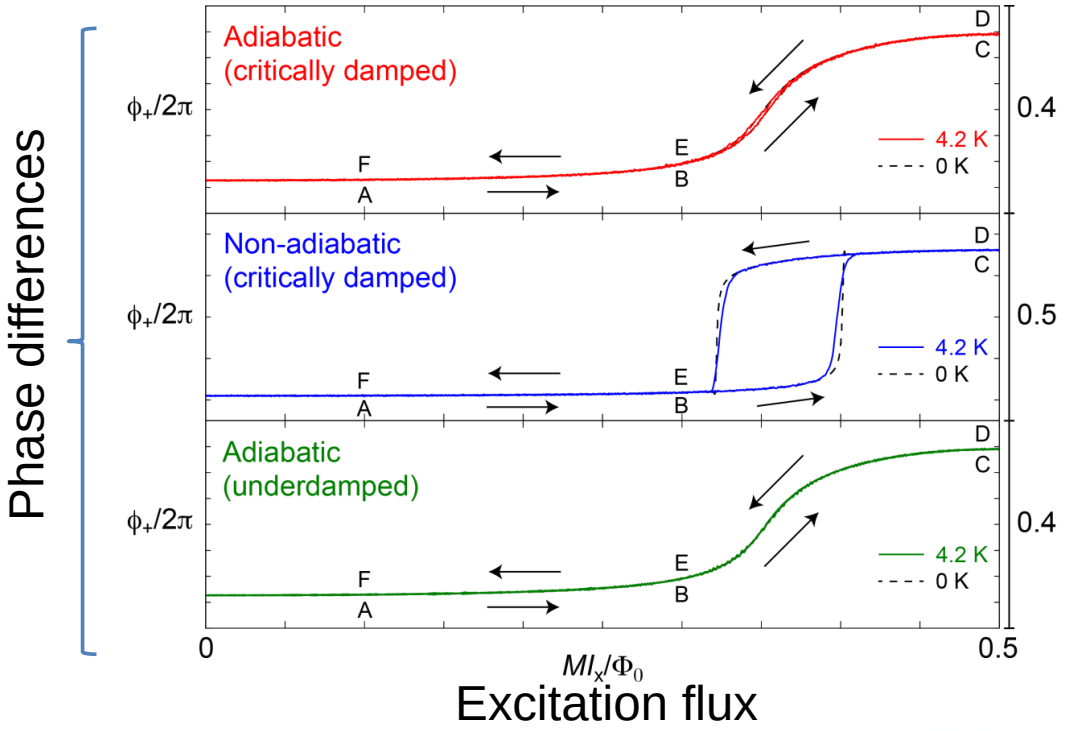
Evolution of Junction Phase





The phase of junctions in AQFP change adiabatically.

Takeuchi *et al.*, Phys. Rev. Appl. 4, 034007 (2015).

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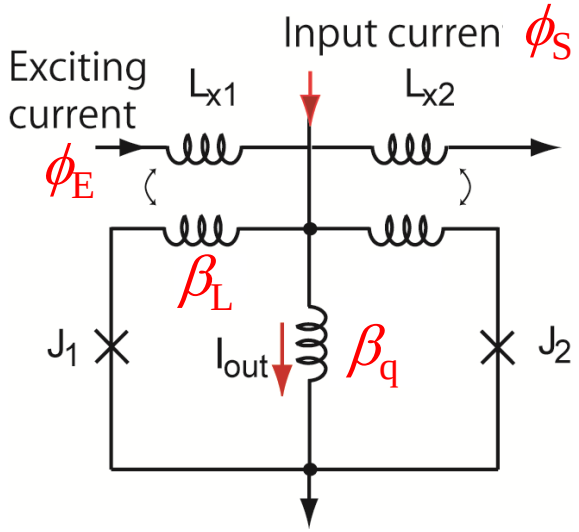
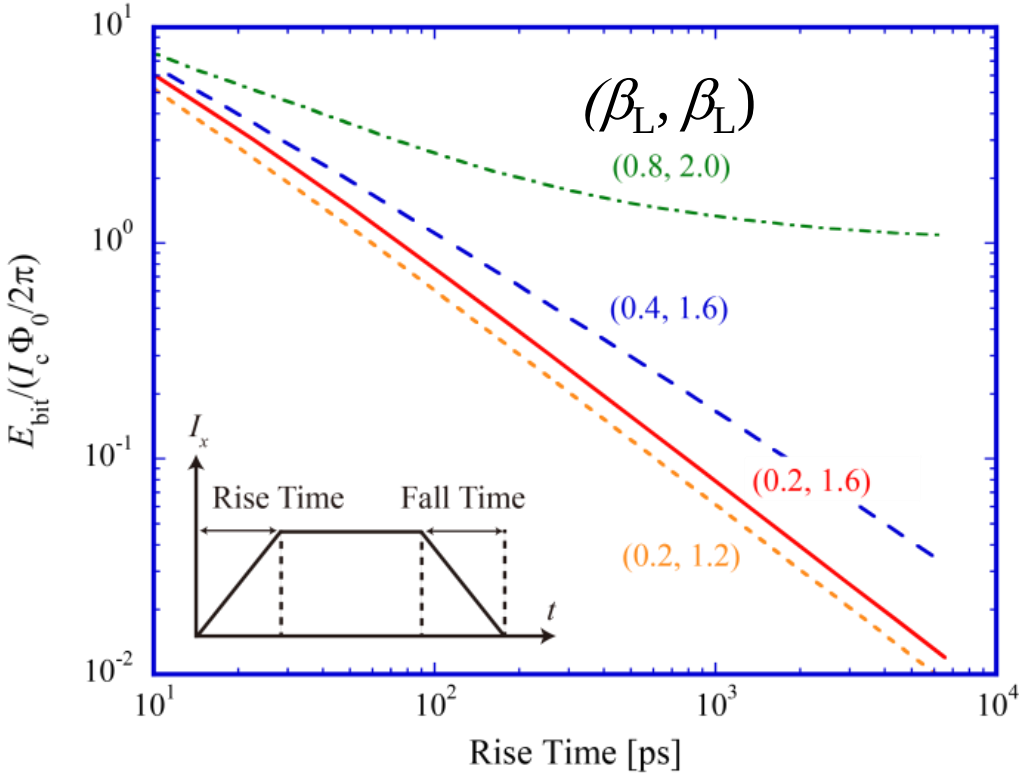
Bit Energy vs. Clock Period of AQFP



Energy dissipation $\propto f$



When rise time is 1000 ps, $E_{bit} = 0.023\, I_c\Phi_0$ (~ $20k_BT$).

→ 1/1000 of RSFQ

N. Takeuchi, *et. al.*, *SUST*, 26, 035010 (2013).

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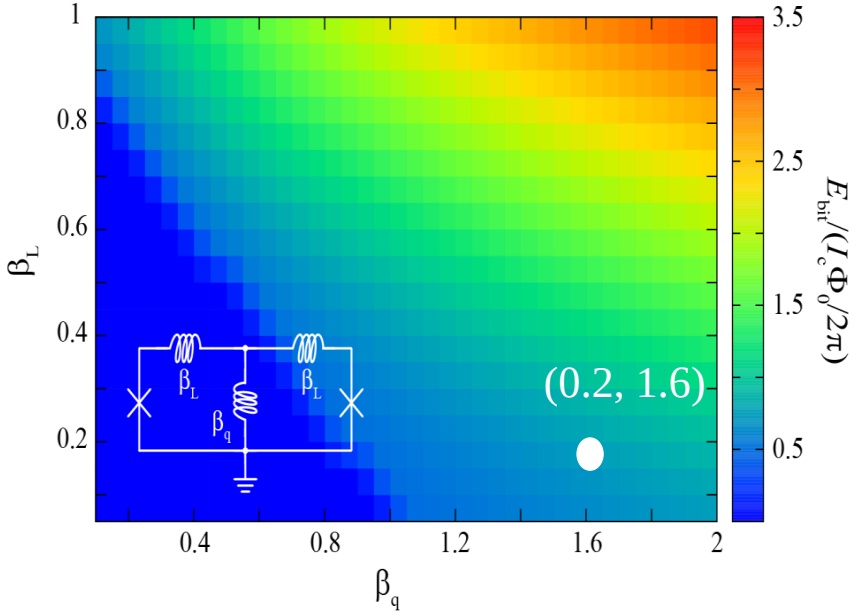
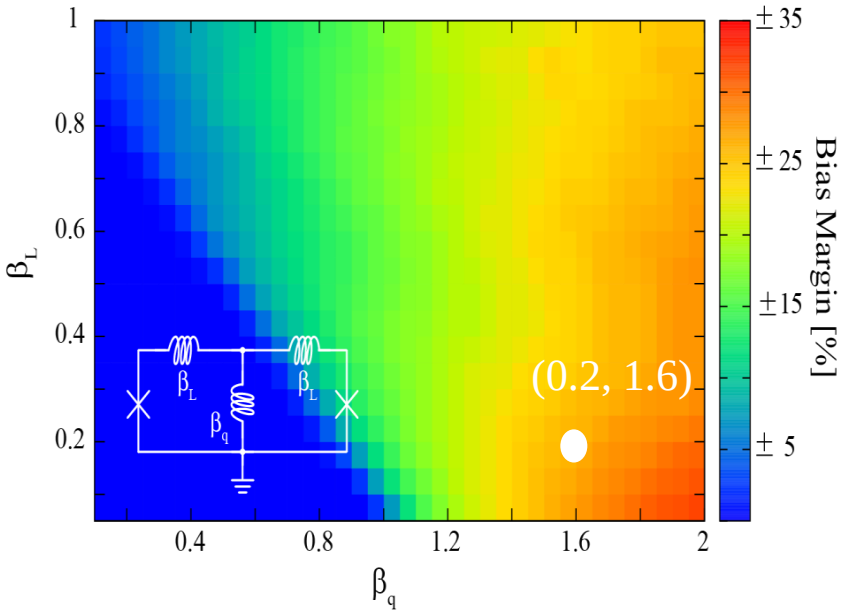
Robust AQFP Design

Bit Energy



$L_{in,n} = L_{q,n}$, $k_q = 0.3$, $I_{in1} = 0.1I_c$ and the rise time is 100 ps.

Bias Margin



$L_{in,n} = L_{q,n}$, $k_q = 0.3$, $I_{in1} = 0.1I_c$ and the rise time is 100 ps.

N. Takeuchi, *et. al.*, *IEEE TAS.*, 23 (2013) 1700304

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Energy Consumption of AQFP

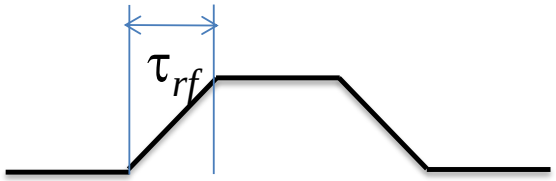
Bit Energy

$$E_{bit} = 2I_c\Phi_0 \frac{\tau_{sw}}{\tau_{rf}}$$

Intrinsic switching time

$$\tau_{sw} \approx \frac{\Phi_0}{I_c R} = \sqrt{\frac{2\pi\Phi_0 C}{\beta_c I_c}}$$

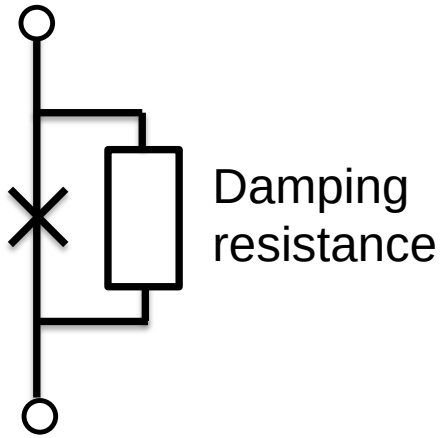
- τ_{rf}: Rising/falling time of clock



- β_c: McCumber parameter

  $\beta_c \sim 1$: critical damping

  $\beta_c > 1$: under damping



N. Takeuchi, *et. al.*, APL., 103, 052602 (2013).

Energy Consumption of AQFP

Bit Energy

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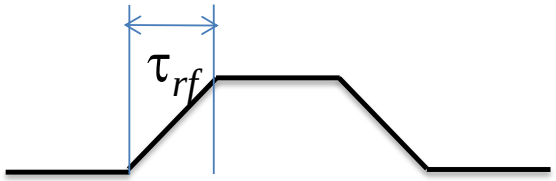
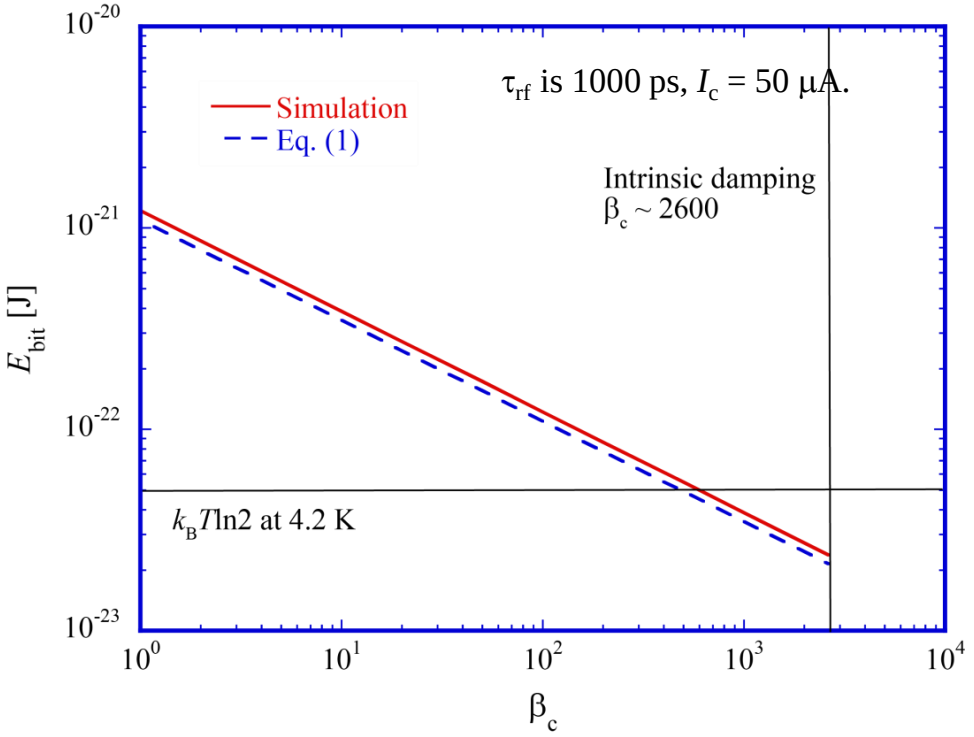
- τ_{rf}: Rising/falling time of clock



β_c Dependence of Bit-Energy of AQFP



N. Takeuchi, *et. al.*, APL., 103, 052602 (2013).

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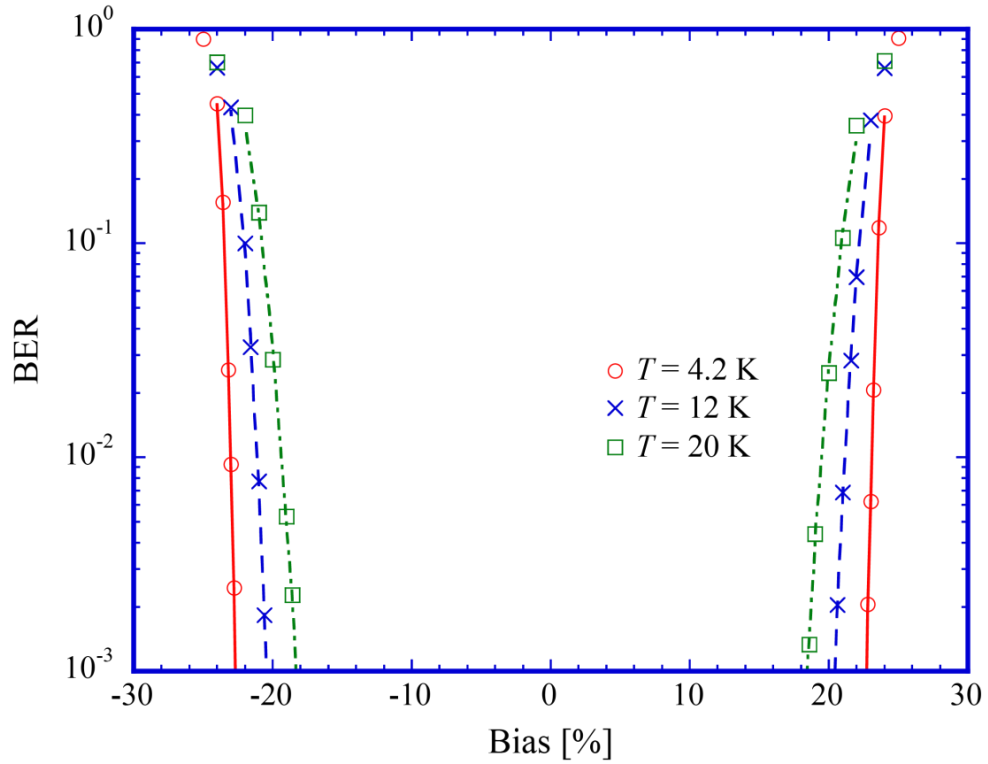
Bit-Error-Rate (BER) of the AQFP at Finite Temperatures



- Iteration number is 10^4.

$(\beta_L, \beta_q) = (0.2, 1.6)$, $I_c = 50$ μA, $L_{in,n} = L_{q,n}$, $k_q = 0.3$, $I_{in1} = 0.1I_c$ and rise time is 200 ps.

T [K]	$I_c\Phi_0/K_BT$	Bias Margin for BER < 10^{-23}
4.2	110	±19.4 %
12	38.6	±13.8 %
20	23.2	±8.8 %

N. Takeuchi, *et. al.*, *IEEE TAS.*, 23, 1700304 (2013).

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Outlines of This Talk

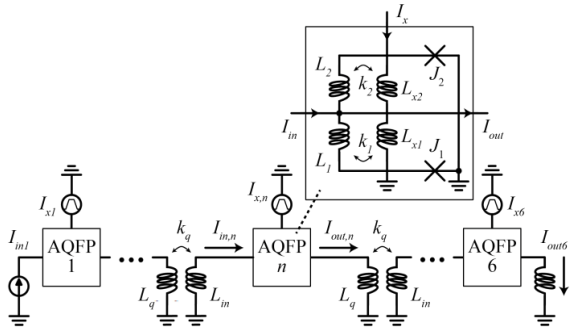
- Background and motivation
- Past and present status of superconducting digital electronics
- Operation principles of AQFP circuits
- AQFP as a logic circuit
- Recent research activities on AQFP circuits
- Future directions
  - Josephson/CMOS hybrid memories
  - Reversible logic circuits
- Summary

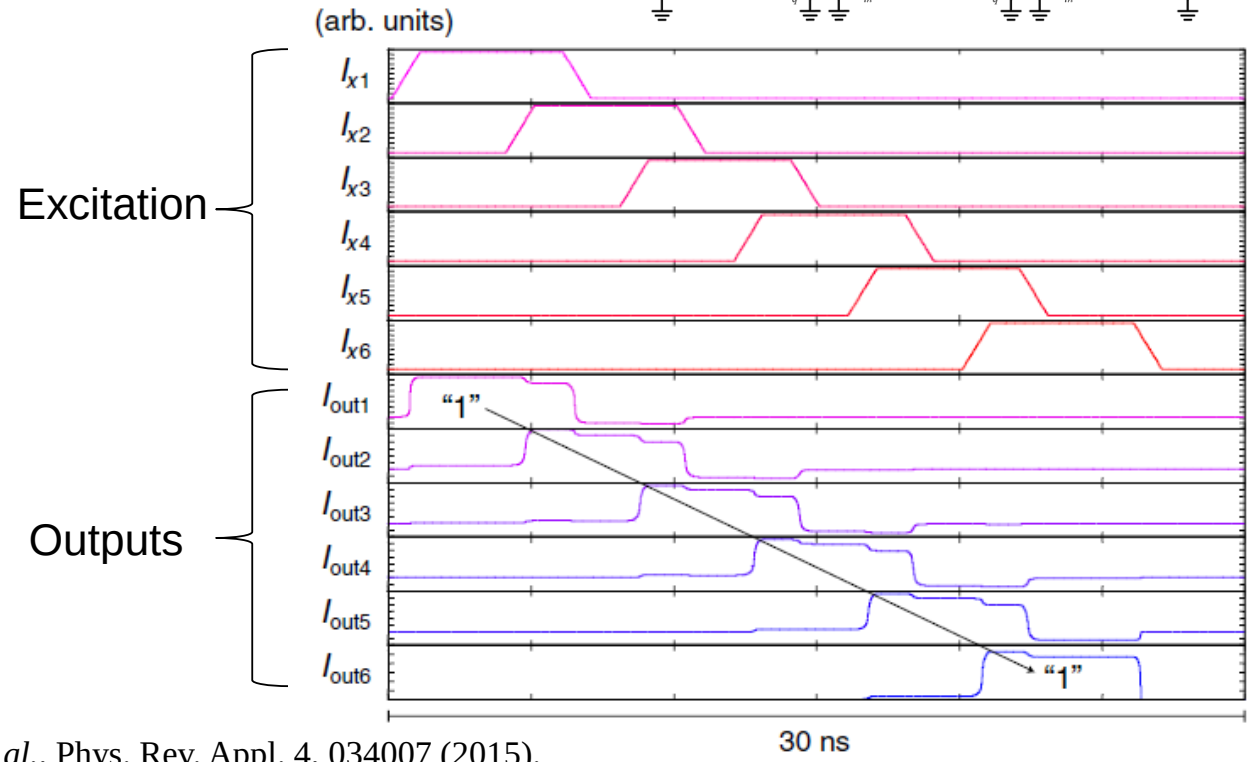
Important Metrics as a Logic Circuit

- Gain/signal reproducibility
- Functionality
- Speed
- Energy consumption
- Driving ability
- Connectability
- Robustness
- Density

Signal Propagation in AQFP Array

$\phi_x/2\pi = 0.5$,
$(\beta_L, \beta_q) = (0.2, 1.6)$,
$I_c = 50\ \mu A$,
$I_{in1} = 5\ \mu A$,
$L_{in} = L_q$, $k_q = 0.3$.



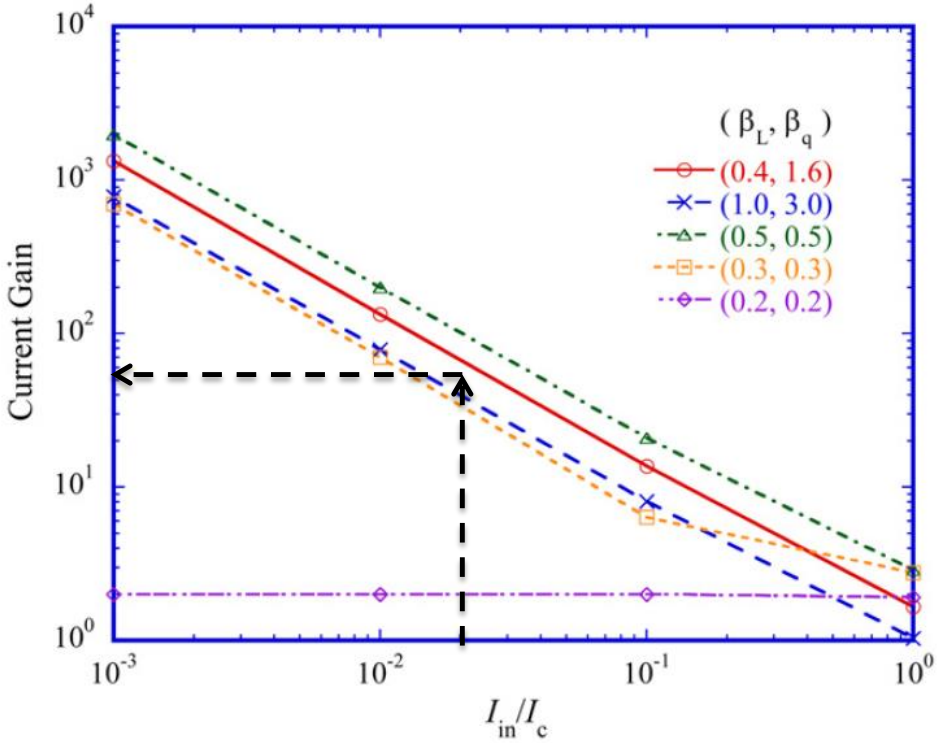


Takeuchi *et al.*, Phys. Rev. Appl. 4, 034007 (2015).

Gain

- Current gain of AQFP is considerably large.

Current gain vs. input current at T = 0K



If we assume

$\delta I_{in} \sim 1\ \mu A$, and $I_c = 50\ \mu A$,

the current gain is given by

$I_c / \delta I_{in} \sim 50$.

δI_{in}: input thermal noise

cf. In RSFQ circuits with

$I_{in} \sim 20\ \mu A$, $I_c = 100\ \mu A$,

the current gain is ~ 5.

N. Takeuchi, *et. al.*, *SUST*, 26, 035010 (2013).

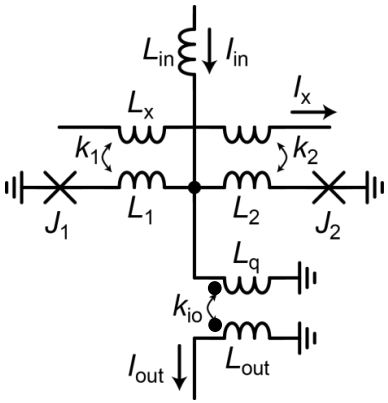
Functionality

- NOT gate is cost free.
- Majority gate is a basic logic gate.

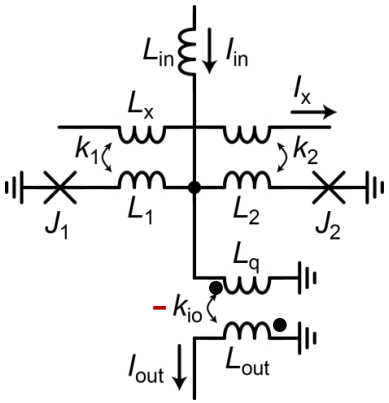
NOT gate is made by using a transformer with negative coupling.

Majority gate is made by connecting three buffer in parallel.

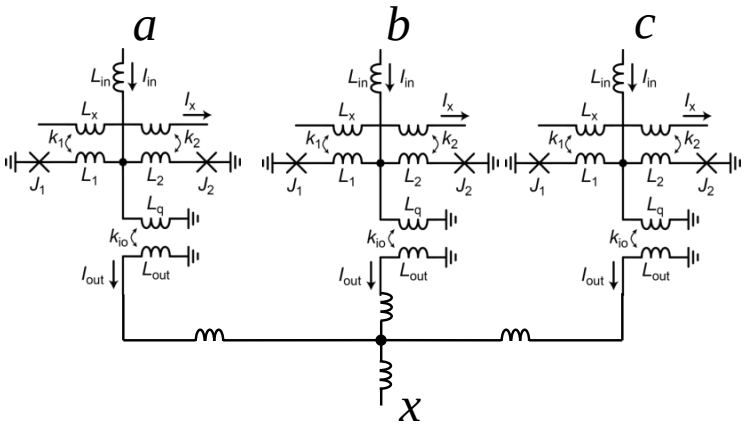
Buffer



NOT



Majority



$$x = \mathrm{MAJ}(a, b, c) = ab + bc + ac$$

K. Inoue, *et al*. IEEE Trans. Appl. Supercond., **23**, 1301105 (2013).

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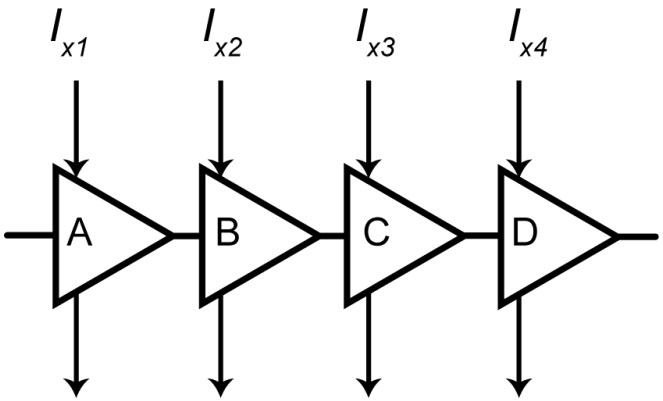
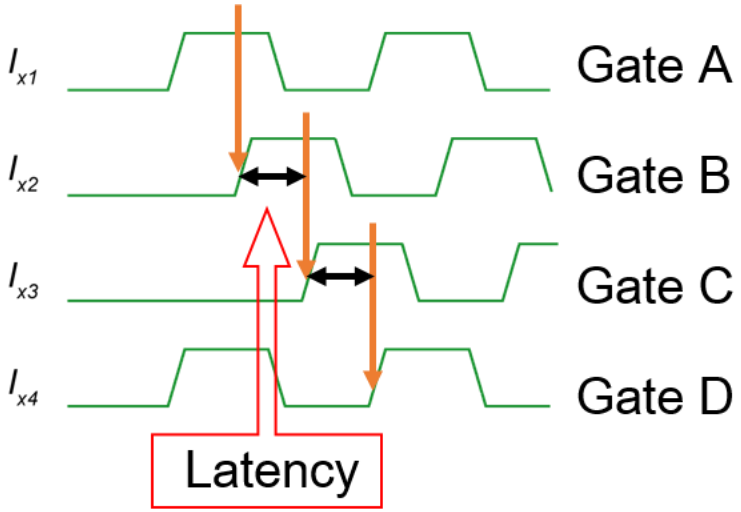
Speed

- AQFP is driven by multi-phase clocks. (4-phase is typically used.)
- Target clock frequency is 5 GHz.
- Double excitation method can increases the clock frequency [1].
- Latency is improved by increasing the number of phase.

Clocking of AQFP gates





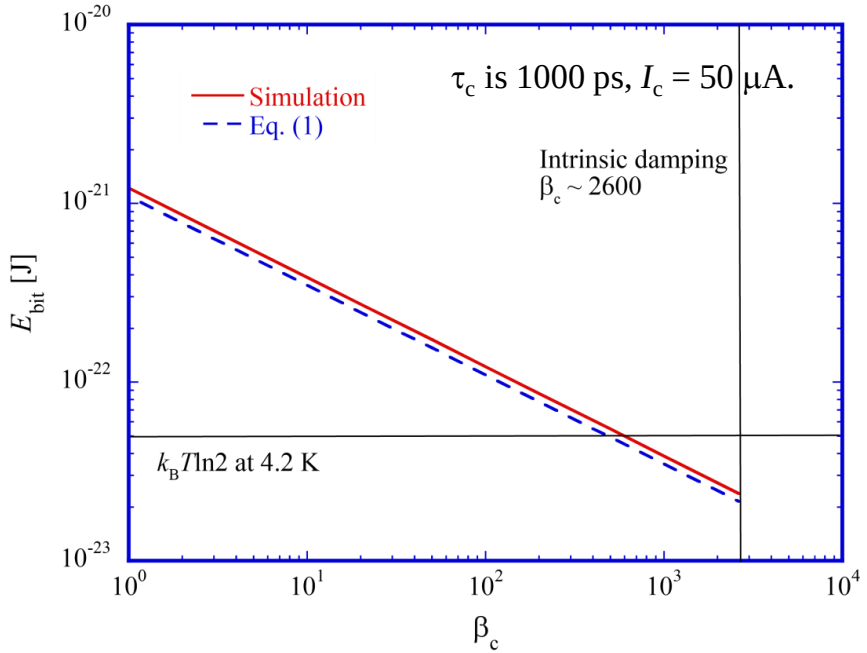
$$Latency = \frac{clock\ period}{number\ of\ phase}$$

[1] K. Fang *et al.*, J. Appl. Phys., **121**, 143901 (2017).

Energy Consumption

- The static energy consumption is zero, the dynamic energy consumption is proportional to the clock frequency.
- The energy consumption is reduced by using high-J_c and high-β_c junctions.

β_c Dependence of Bit-Energy of AQFP



N. Takeuchi, *et. al.*, APL., 103, 052602 (2013).

Bit energy:

$$E_{bit} = 2I_c\Phi_0\frac{\tau_{sw}}{\tau_{rf}}$$

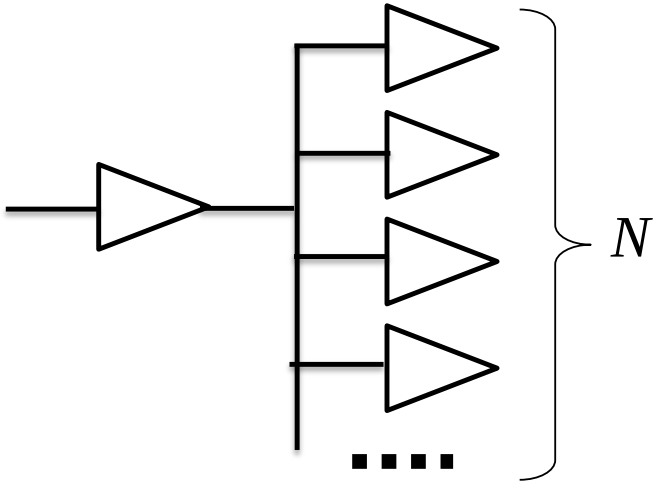
Intrinsic switching time:

$$\tau_{sw} \approx \frac{\Phi_0}{I_c R} = \sqrt{\frac{2\pi\Phi_0 c}{\beta_c j_c}}$$

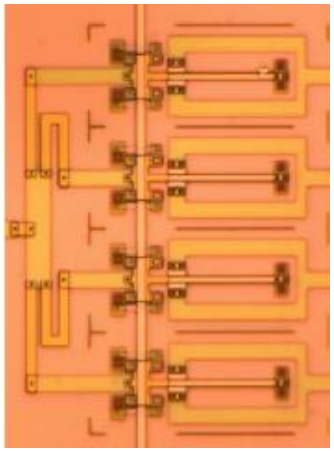
Driving Ability

- Fan-out of AQFP gate is relatively large (~ 4).

Fan-out



1:4 splitter



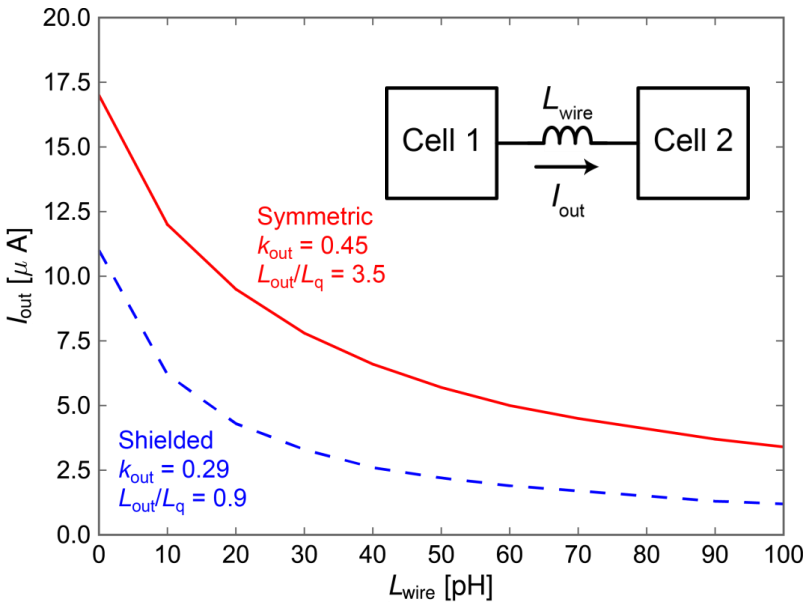
cf. optimal fan-out of CMOS is 3 ~ 4.

AIST Nb Josephson standard process (STP2) was used.

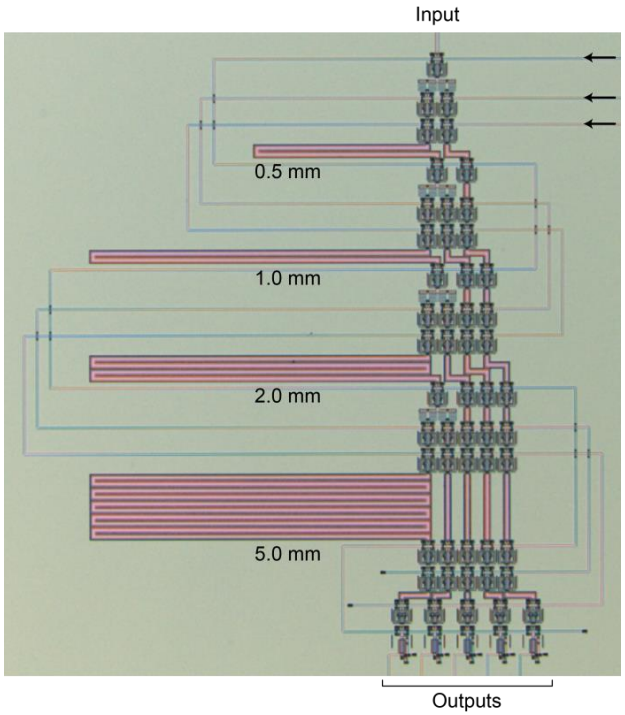
Connectability

- The output current of AQFP gate decreases with increase of interconnect inductance, which limits the wire length.
- L_{max} ~ 1 mm.

I_{out} vs. L_{wire}

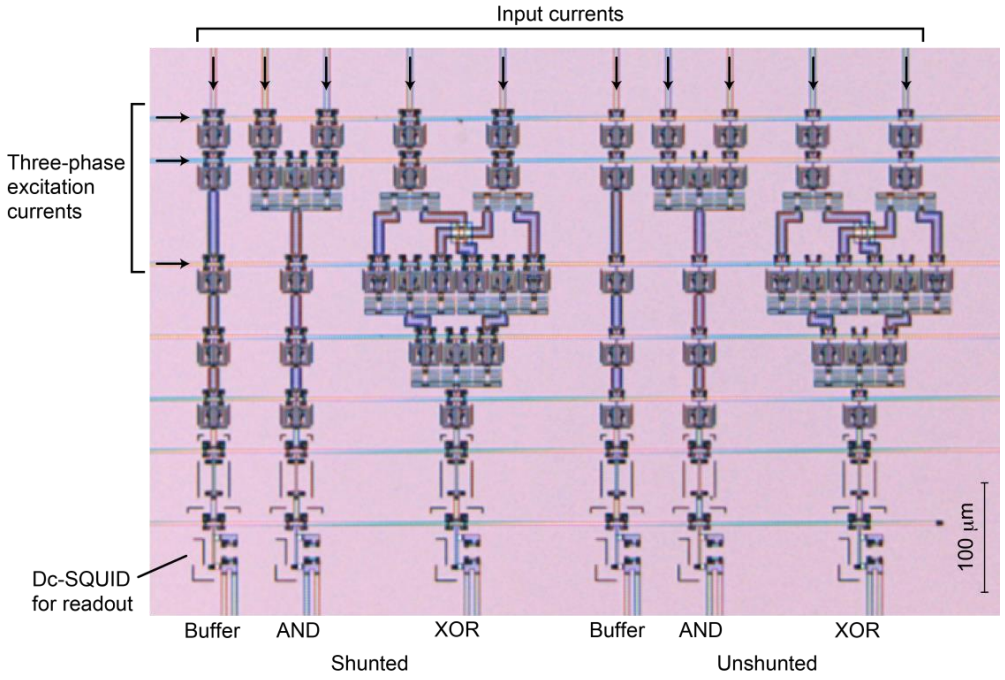


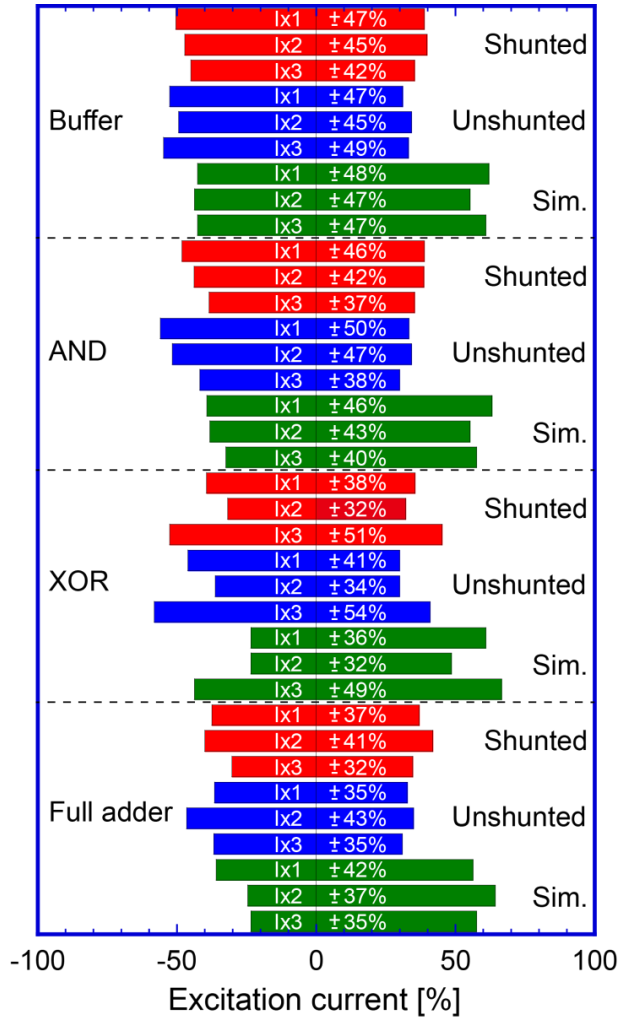
Testing of maximum wiring length



N. Takeuchi et al., J. Appl. Phys. **117**, 173912 (2015).

Robustness

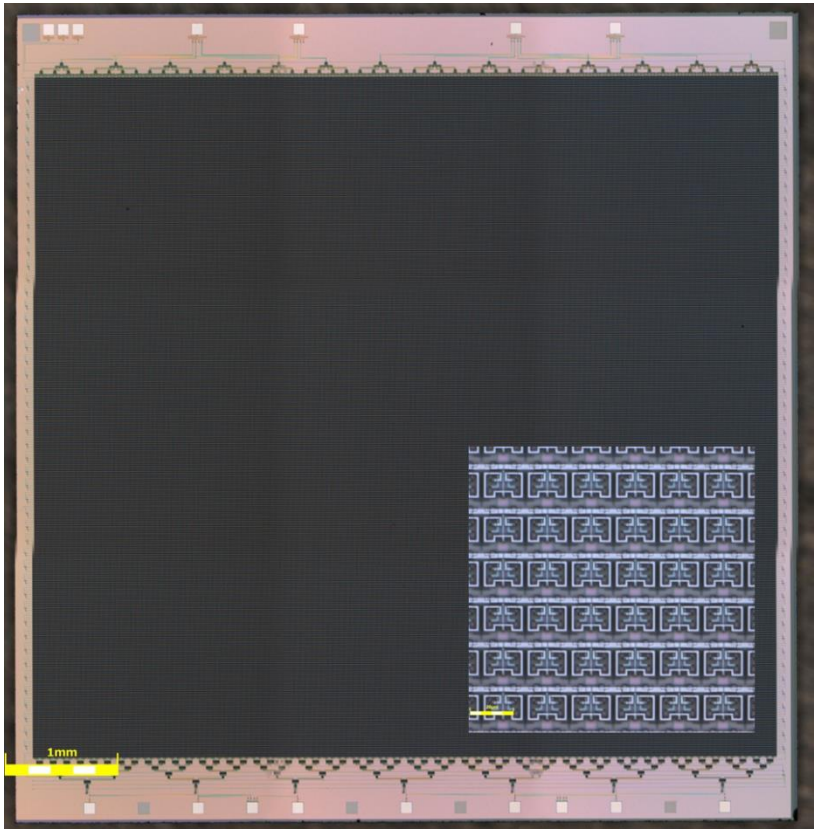




Wide operation margins were observed in experiments.

N. Takeuchi et al., J. Appl. Phys. **117**, 173912 (2015).

Demonstrated 84k-Junction AQFP buffer array



- AQFP is robust because
  - The operation is based on differential pairs of junctions and inductances.
  - The critical current of all junctions is the same.

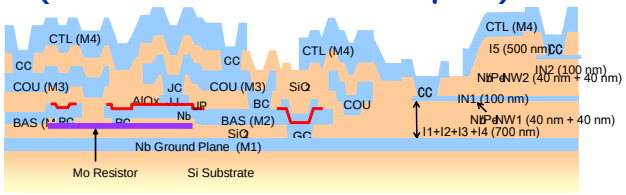
Area	6.68×6.23 mm^2
Bias Current	3.60 mA
JJ number	83736

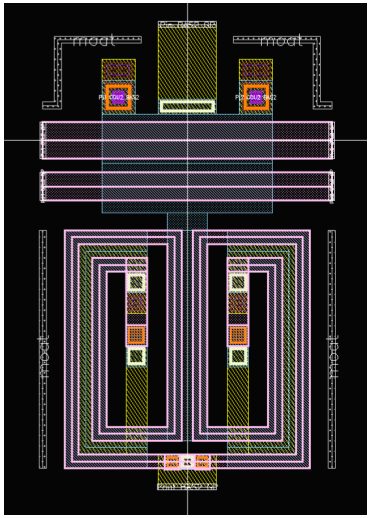
AIST 10 kA/cm^2 high-speed standard process (HSTP) was used.

Density

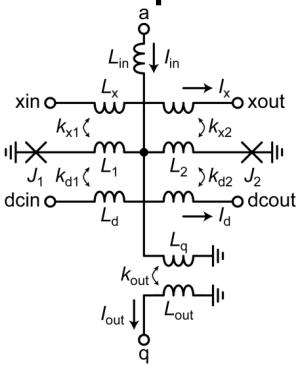
- Multi-layer processes improve the circuit density.

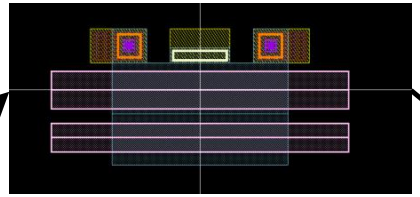
4-metal layer process (Junction size ~ 1 μm)



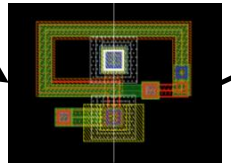


25 × 40 μm²



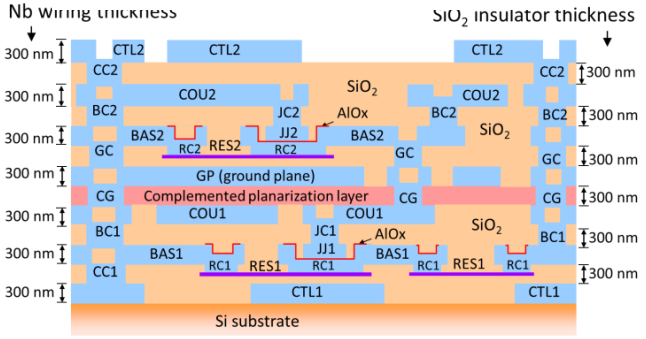


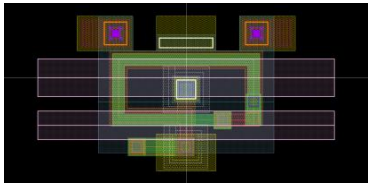
Excitation line (upper layers)



Transformer (lower layers)

7-metal layer process (Junction size ~ 1 μm)





13 × 25 μm²
(-67.5% area reduction)

~ 0.3M gate/cm²

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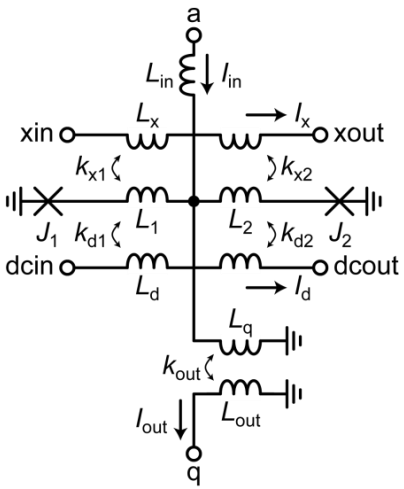
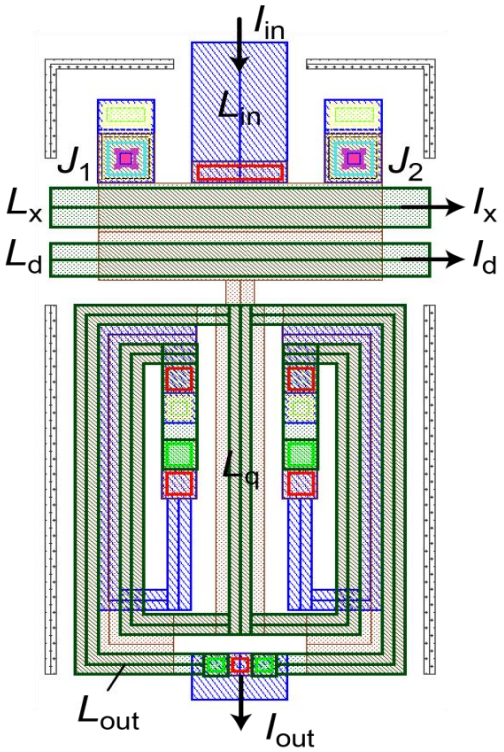
AQFP Cell Library for the MIT LL 8-Metal Layer Process

Schematic of an AQFP buffer

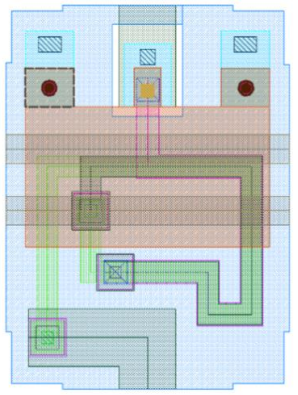


Layouts of an AQFP buffer



20 μm x 40 μm

AIST HSTP process



15 μm x 20 μm

MIT LL process (SFQ5ee)

- AQFP and an output transformer can be overlapped by using the MIT LL multilayer process.

Supported by IARPA, SuperTools project

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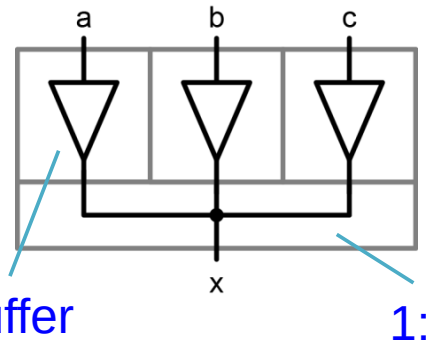
Design Methodology

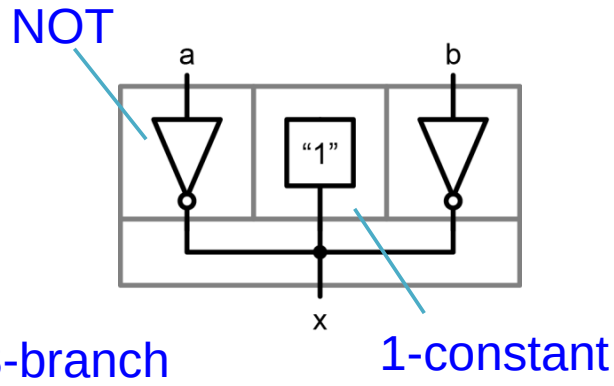
- Logic cells can be designed by placing four building blocks: Buffer, NOT, Constant, Branch

Majority



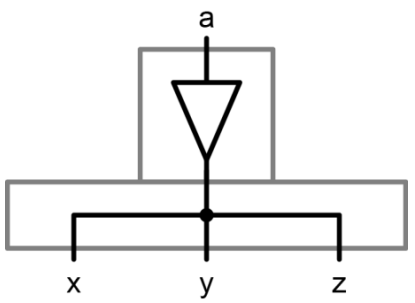
$$x = \mathrm{MAJ}(a,b,c)$$
$$= a \cdot b + b \cdot c + c \cdot a$$

NAND



$$x = \mathrm{MAJ}(\bar{a},1,\bar{b})$$
$$= \bar{a} + \bar{b}$$
$$= \overline{ab}$$

Splitter



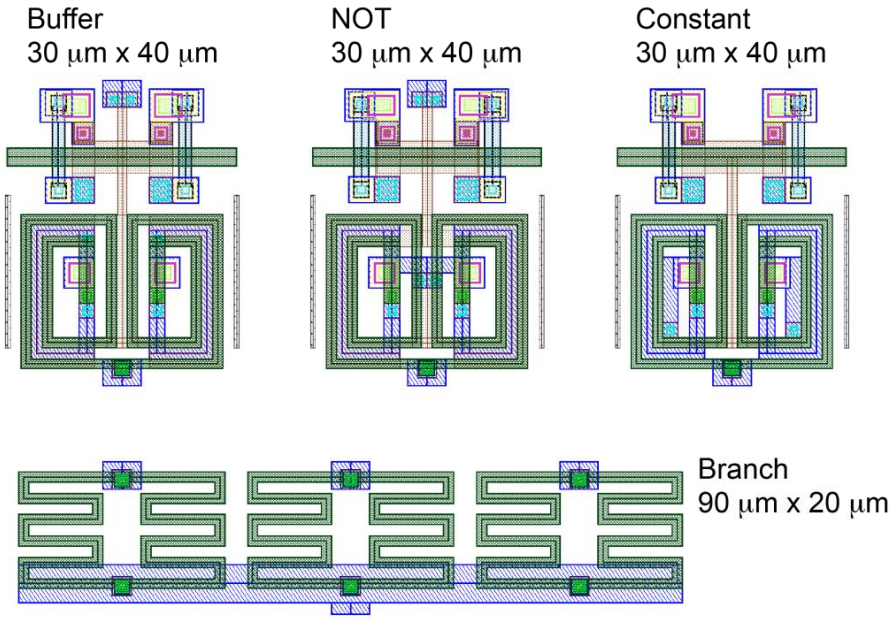
$$x = y = z = a$$

N. Takeuchi *et al.*, J. Appl. Phys. **117**, 173912 (2015).

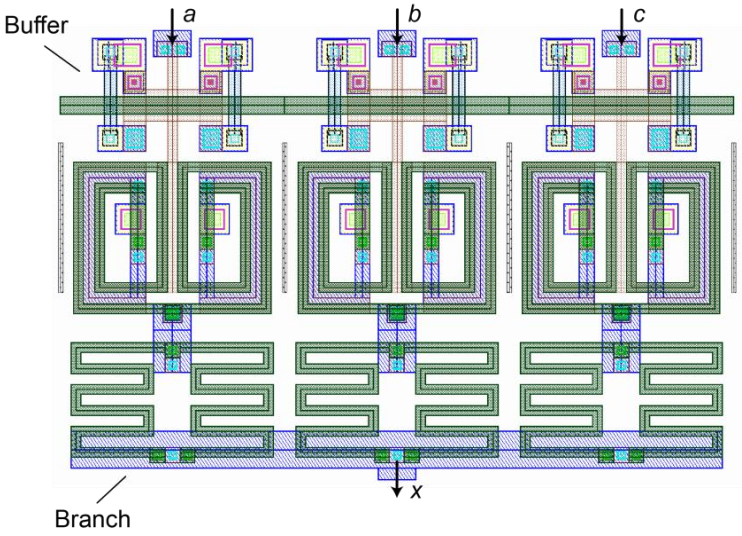
Layout of Basic Cells

- Symmetric design prevents the parasitic coupling between the excitation and output inductance

Building block cells



Majority cell



N. Takeuchi *et al.*, J. Appl. Phys. **117**, 173912 (2015).

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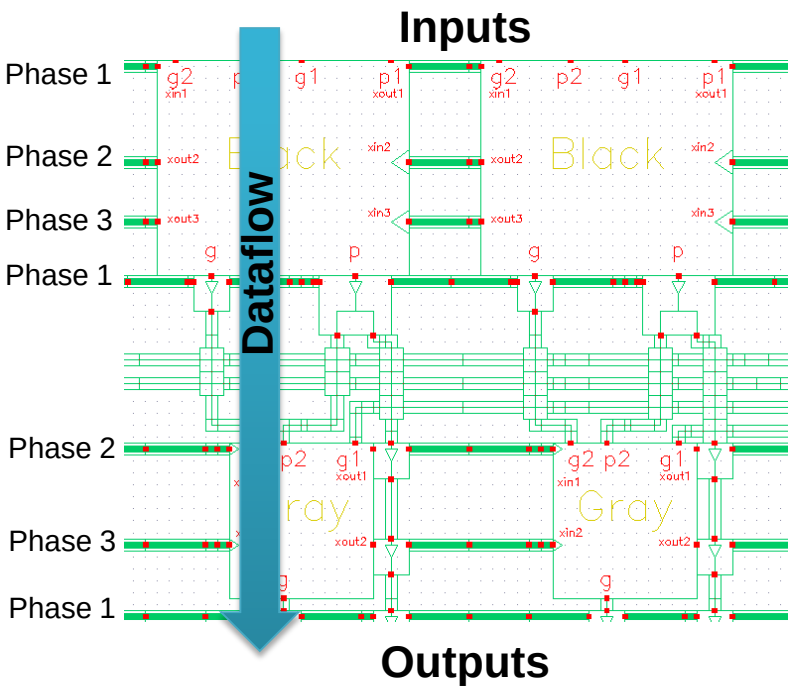
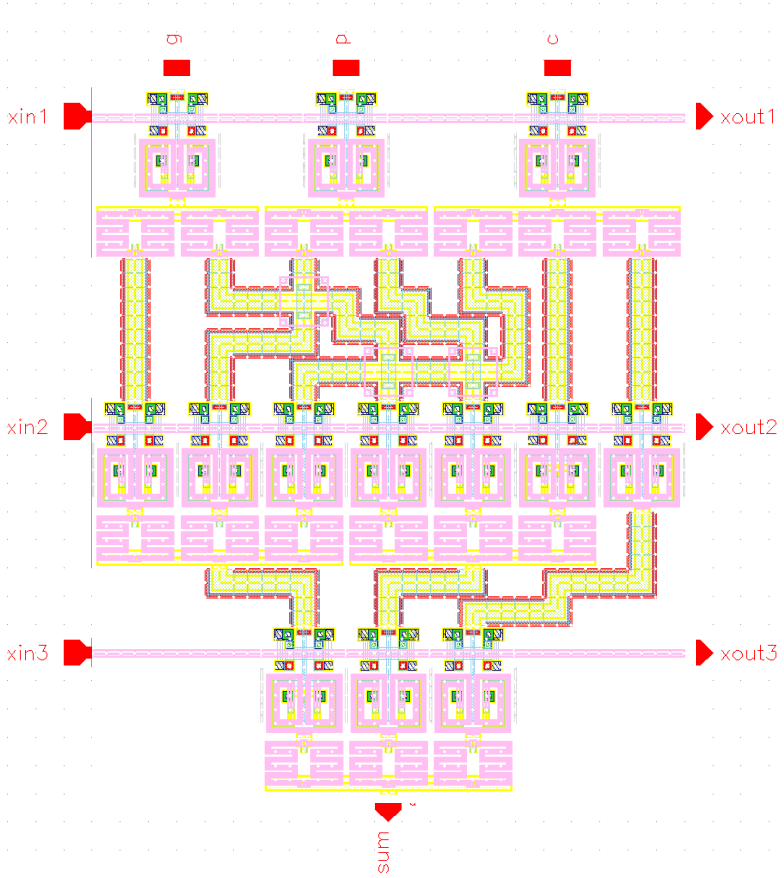
AQFP Logic Design





- Logic cells are placed together like Lego blocks
- Logic gates grouped by phase & data flow

AQFP design flow

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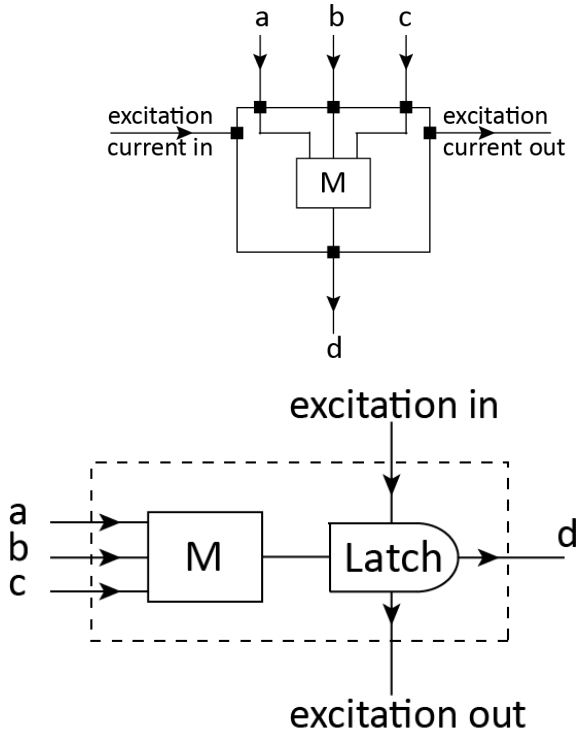
HDL-Modeling of AQFP Logic

HDL-modeling of AQFP Majority gate

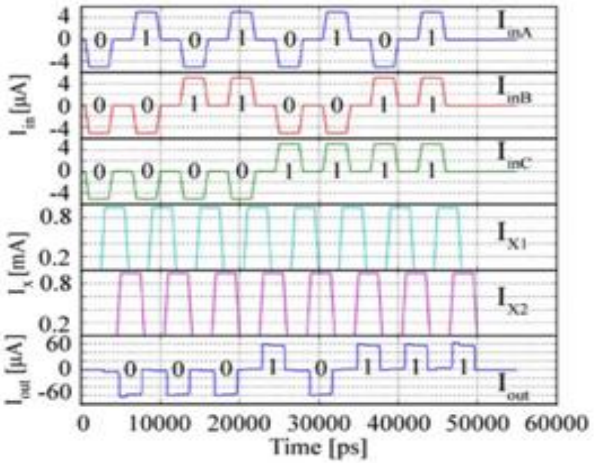


An AQFP majority gate is modeled by a combinational logic with a larch.

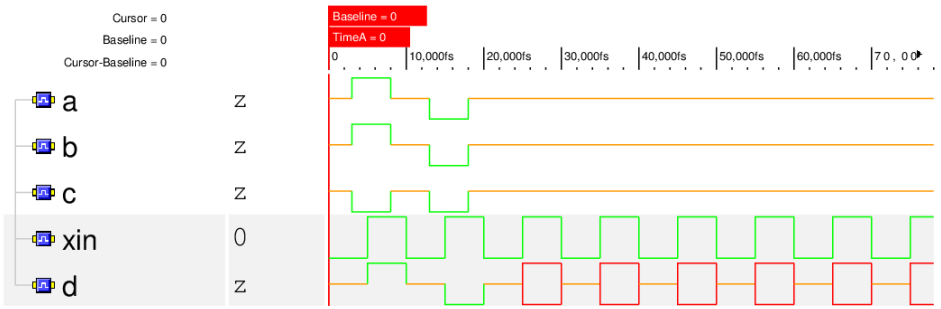
Q. Xu et al., IEEE TAS, 26, 1–5 (2016).
Q. Xu, *et al*., IEEE TAS., **27**, 1301905 (2017).

Waveform of AQFP majority gate

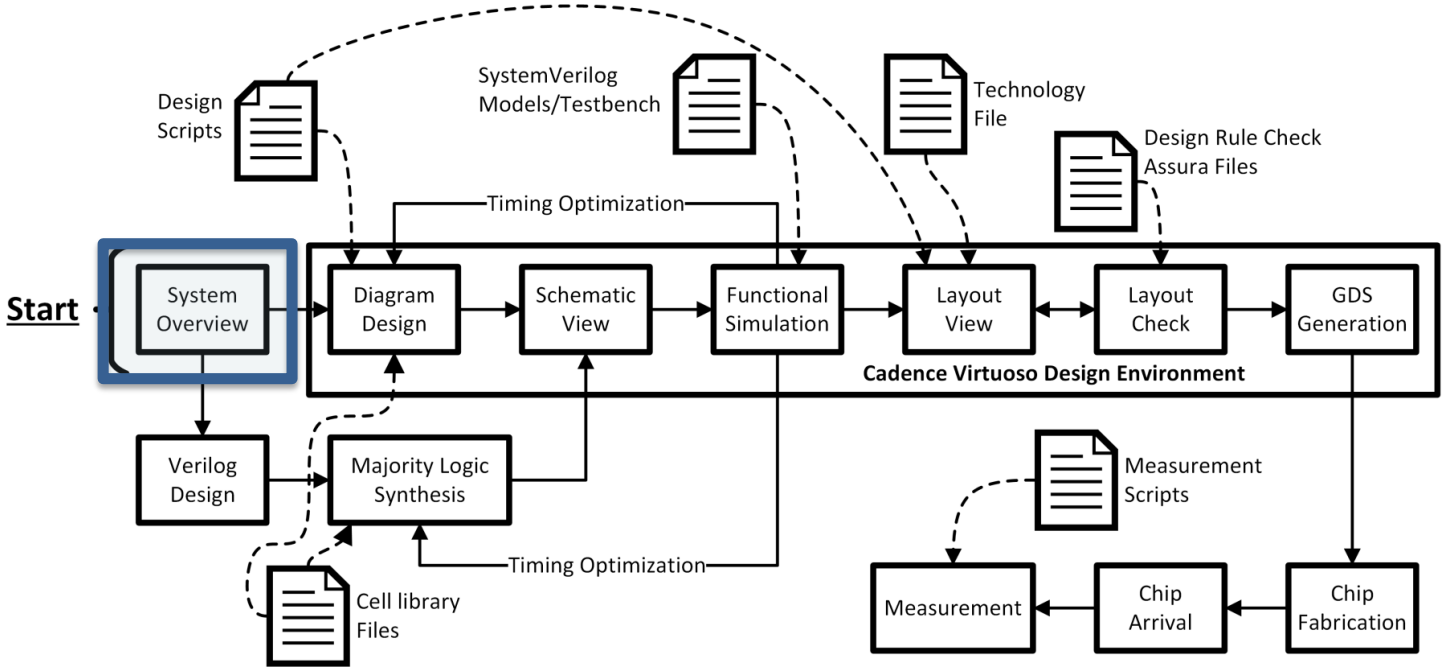
Analog simulation results



Digital simulation results

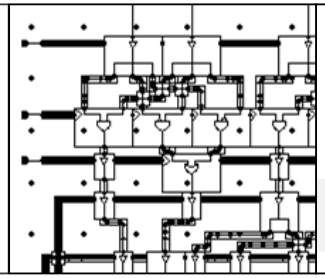


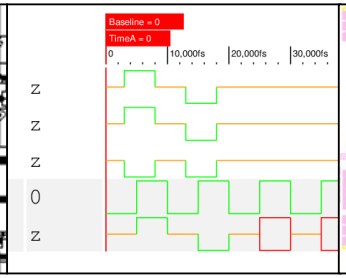
EDA Tools for Top-Down Design

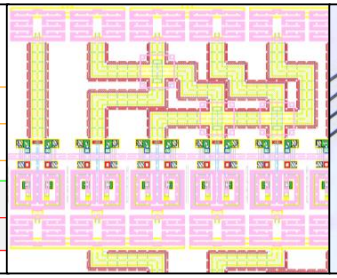


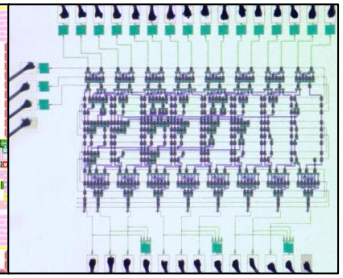
Verilog/VHDL | Schematic | Digital Sim. | Layout | Chip

```
Function: 1-bit full-adder
Pin: input (a,b,carry_in)
       output (carry_out, sum)
Lib: AQFP standard library
Behaviour description:
     sum = a + b + carry_in,
     carry_out = a*b + (a+b)*c;
```









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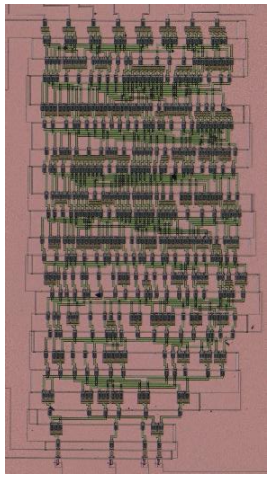
AQFP Circuits Fabricated by Top-Down Design Flow

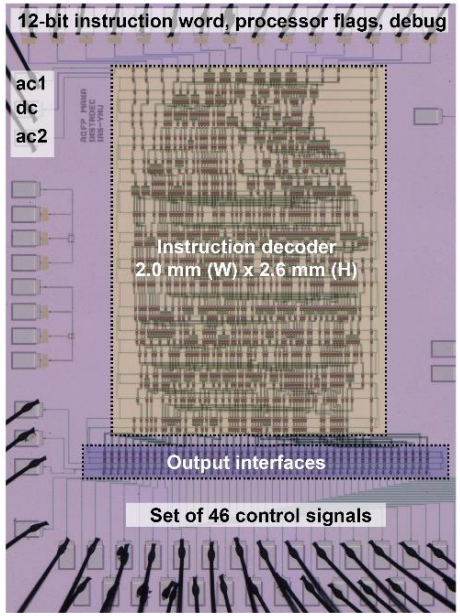
4-bit shifter



1090 JJ

Correct operation confirmed

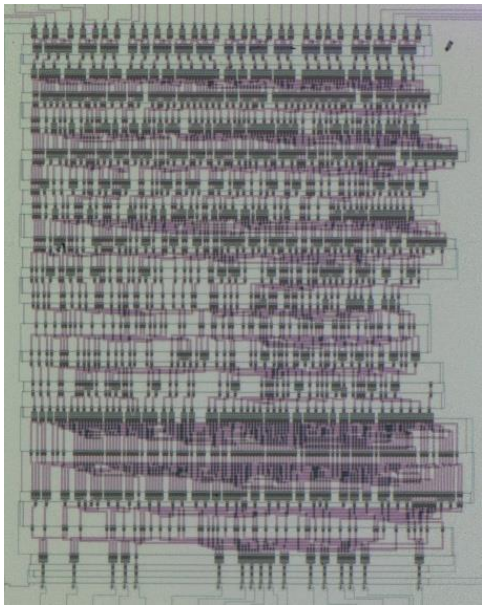
12-bit instruction decoder



2664 JJ

Partial operation confirmed

16-bit carry look-ahead adder



4976 JJ

Partial operation confirmed

8-bit shifter

7100 JJ

C. Ayala *et al.*, ISEC 2019, Riverside.
T. Tanaka *et al.*, ISEC 2019, Riverside.

Fabricated by AIST HSTP

CRAVITY AIST

Y. Murai *et al.*, IEEE TAS. 27, 1–9 (2017).
T. Tanaka *et al.*, IEEE TAS 29,1-6 (2019).

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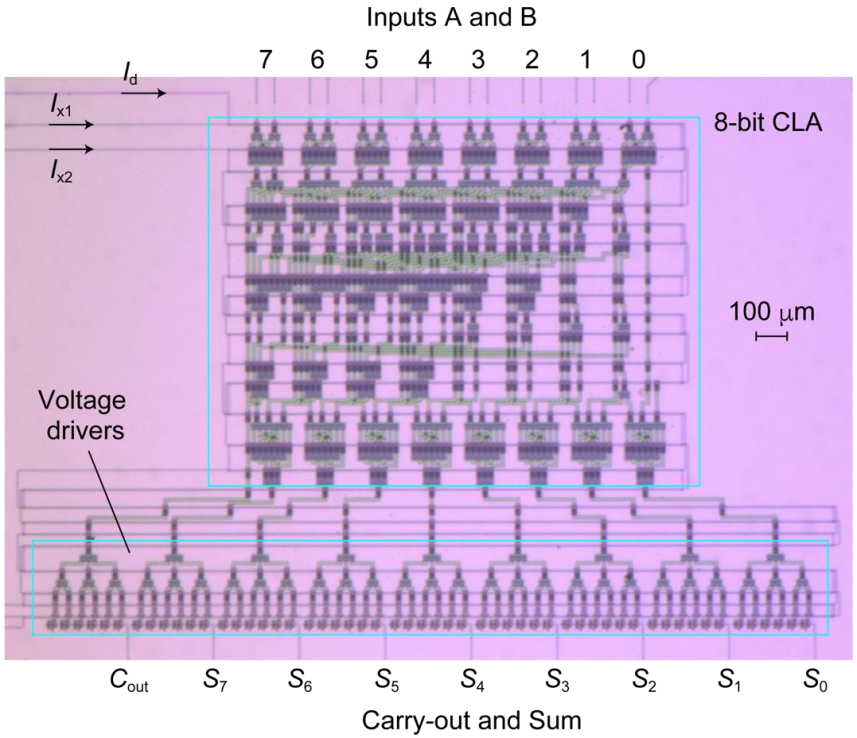
Measurement of Energy Consumption of AQFP Circuits at 5 GHz

8-bit AQFP Cary Look-ahead Adder



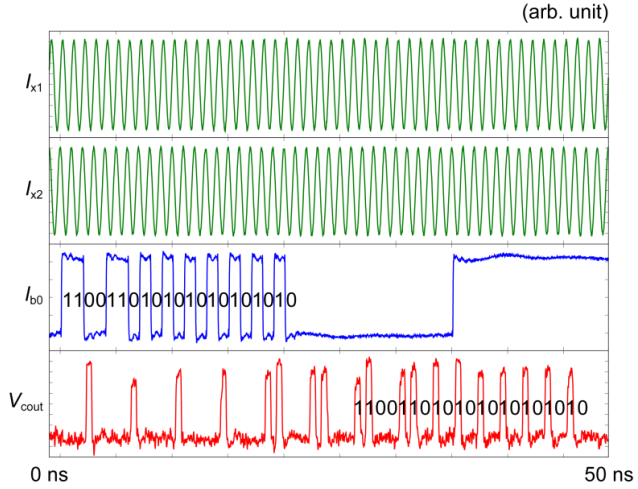
The total junction count: 1,638

Energy consumption: 1.5 aJ/operation
~ 24 k_BT/junction

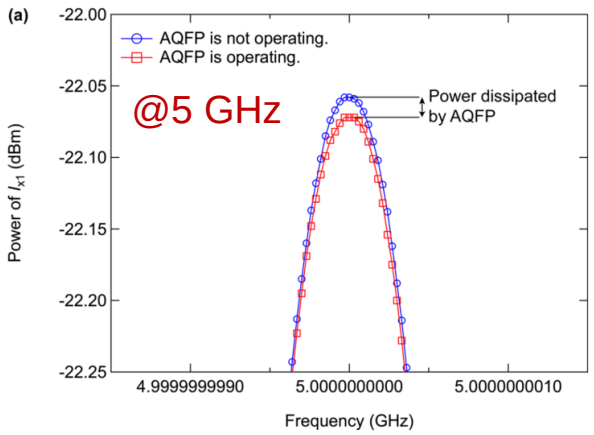
Fabricated by AIST HSTP

Takeuchi *et al.*, APL 114 (2019) 042602

Output waveform of carry @1 GHz

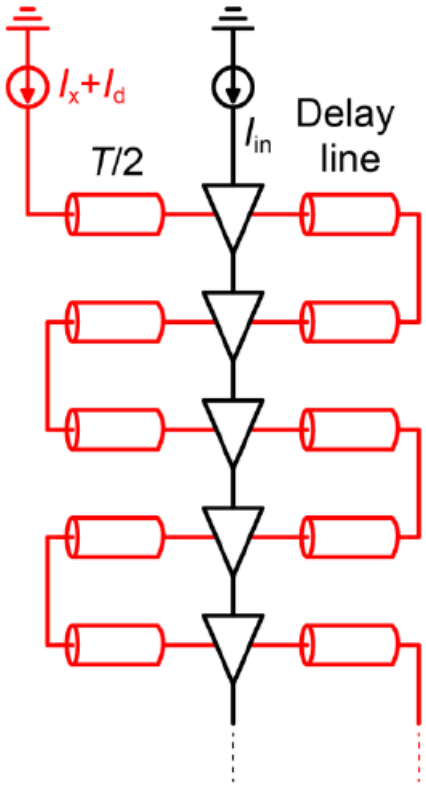


Power consumption measurements



Delay-line Clocking for Short Latency

Phase-to-phase clock delay shorten by delay line

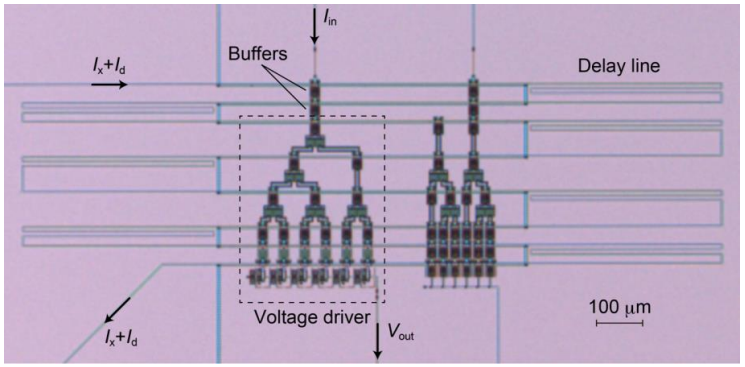


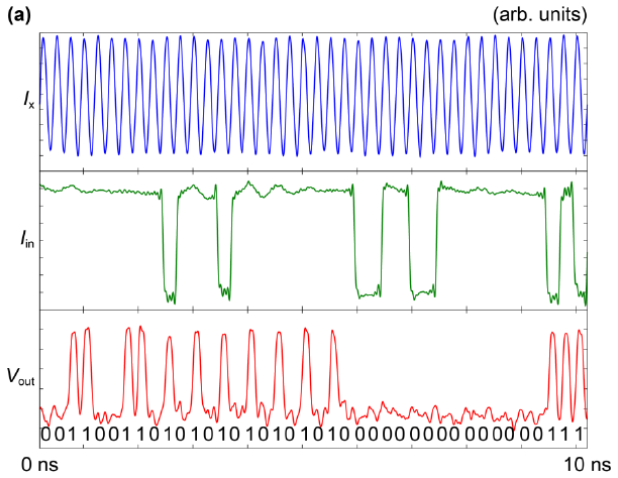
5-GHz 4-phse clock latency ~ 50 ps

Delay-line clock latency ~ 5 ps

Fabricated by AIST HSTP

4-GHz test result of AQFP buffer array with latency of 10 ps





Takeuchi *et al.*, APL to be published.

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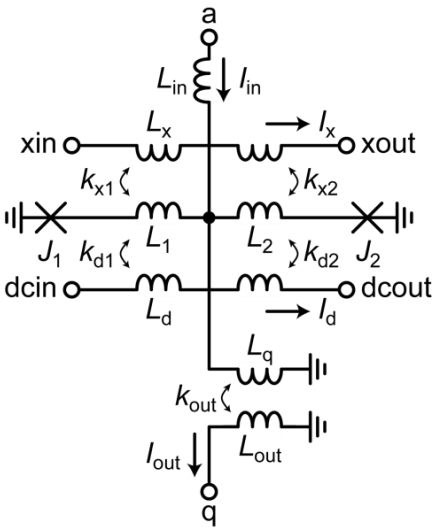
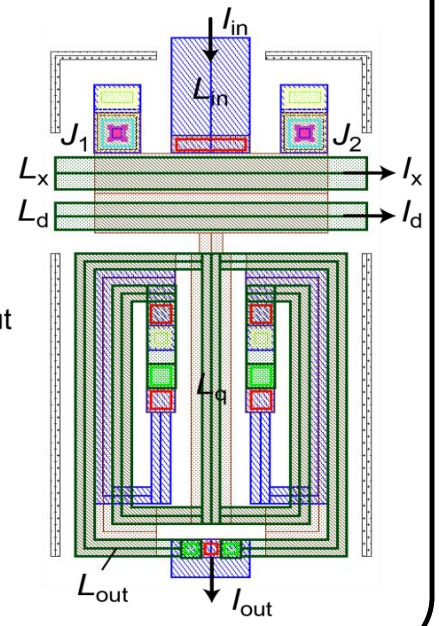
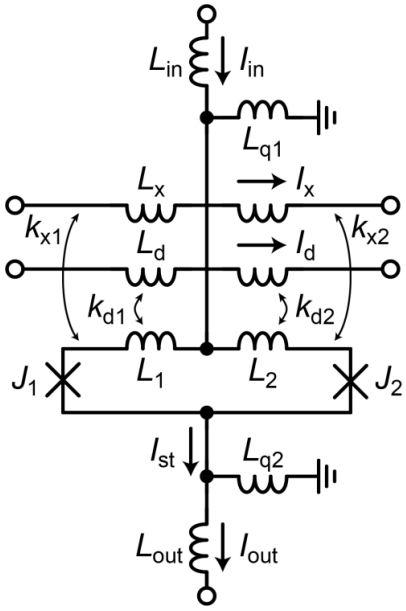
Directly Coupled AQFP Logic

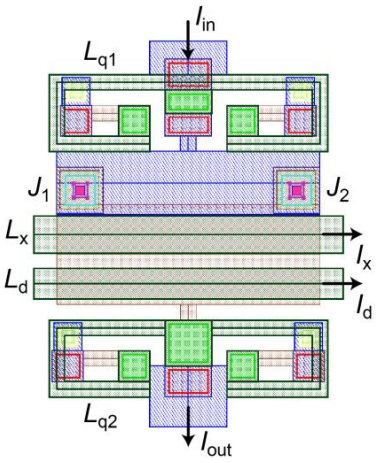
Conventional AQFP inverter





Directly coupled AQFP inverter





- Transformer was removed to decrease the cell size.
- Good for scaling down the device size in the future

Fabricated by AIST HSTP

CRAVITY AIST

Takeuchi *et al.*, submitted to Phys. Rev. Appl.,

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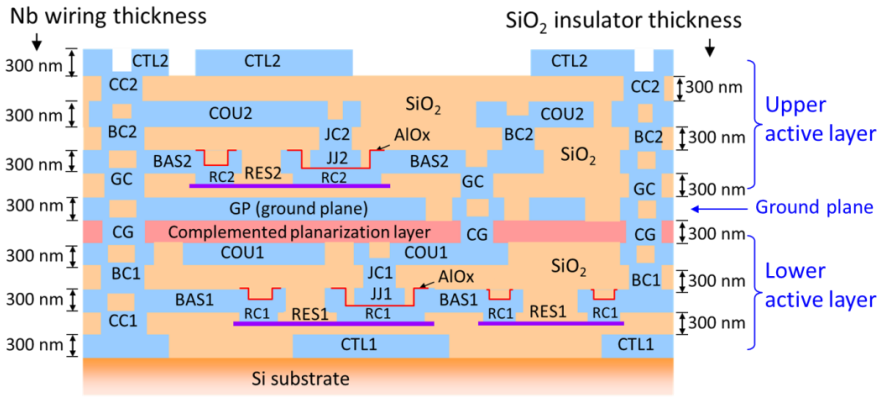
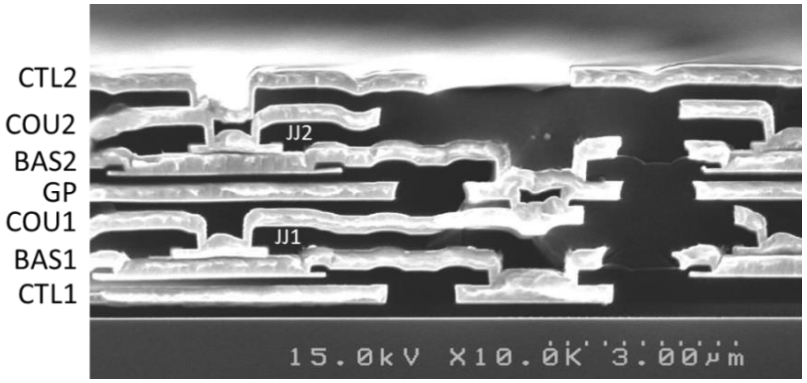
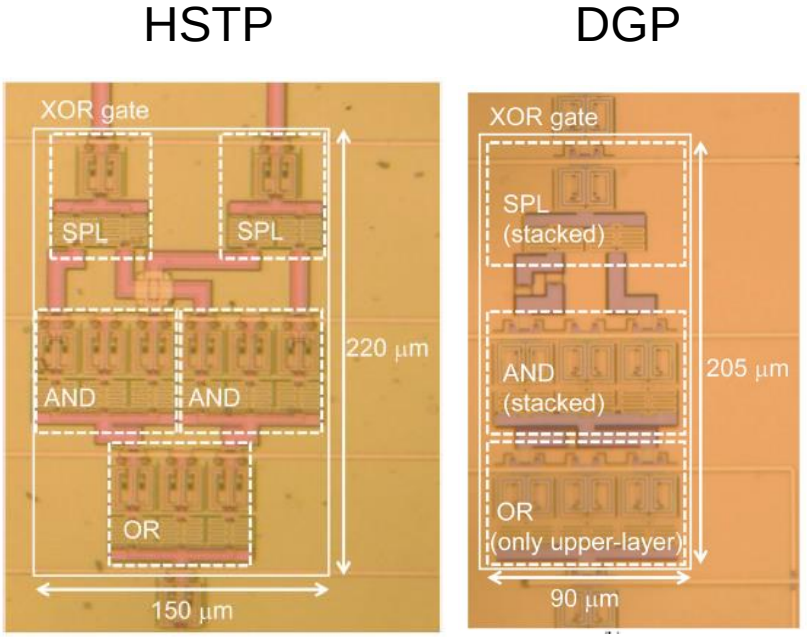
Development of 3D AQFP ICs

Double Gate Process (DGP)





Comparison of XOR Gate



The circuit area was reduced by 44%.

Fabricated by AIST DGP

CRAVITY AIST

T. Ando *et al.*, SUST 30 (2017) 075003.

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Outlines of This Talk

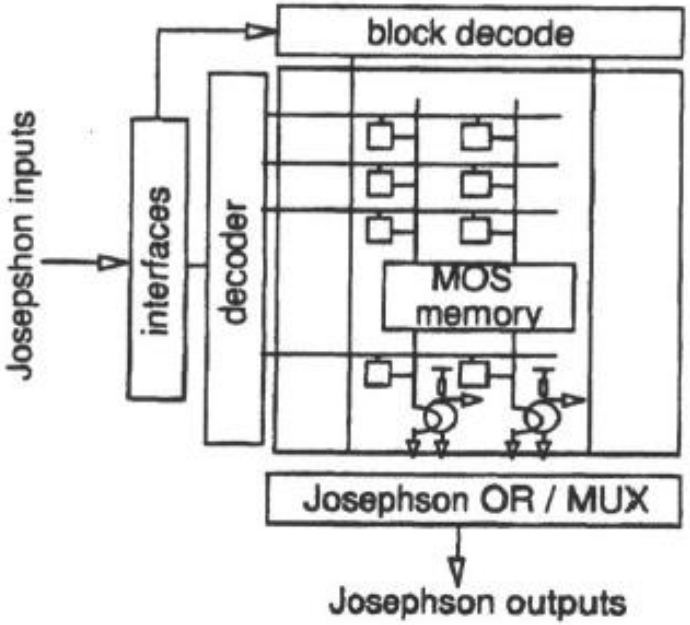
- Background and motivation
- Past and present status of superconducting digital electronics
- Operation principles of AQFP circuits
- AQFP as a logic circuit
- Recent research activities on AQFP circuits
- Future directions
  - Josephson/CMOS hybrid memories
  - Reversible logic circuits
- Summary

Future Directions

- Memories
  - Josephson-CMOS hybrid memories
  - Magnetic memories
- More energy efficient logic
  - Reversible QFP (RQFP) circuits.
- Other applications
  - Control and readout circuits for Quantum computers
  - Read out circuits for superconducting sensor arrays

Josephson/CMOS Hybrid Memory

Concept of hybrid Josephson-CMOS RAM



[1] Ghoshal *et al.*, IEEE TAS, 3, 2316, 1993.

64-kb Cryo-CMOS RAM

180 nm CMOS and 2.5 kA/cm^2 JJ processes

[2] G. Konno *et al.*, IEEE TAS, 27, 1300607, 2017.

Successful demonstration of SFQ processor with a cryo-CMOS memory:
Y. Hironaka *et al.*, ISEC 2019, Riverside.

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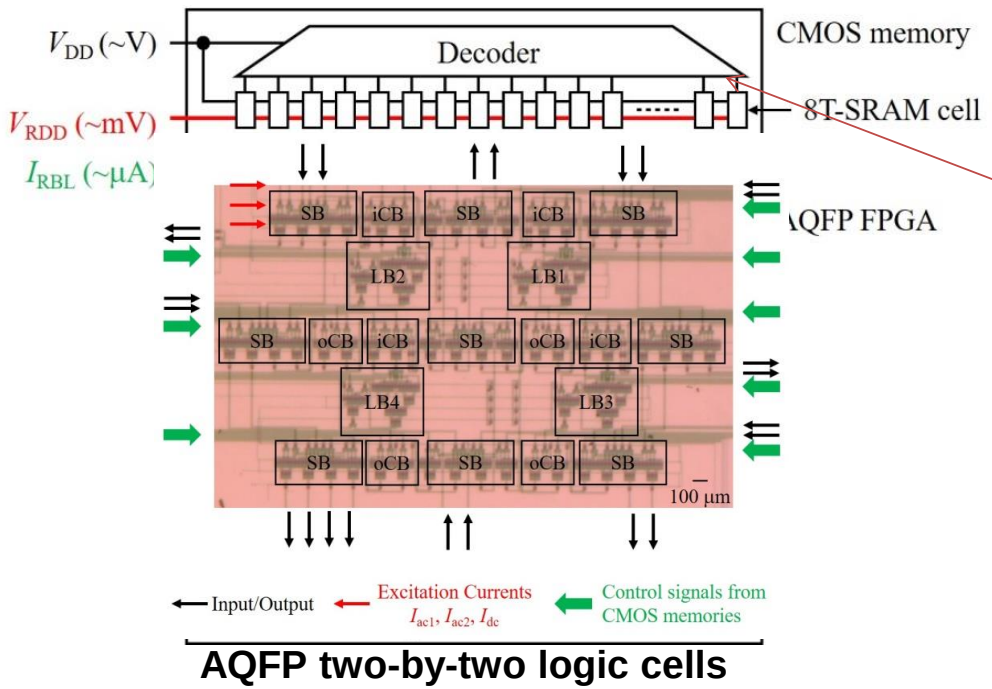
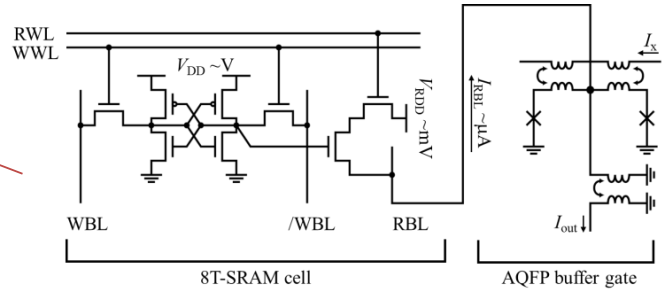
AQFP-CMOS Hybrid FPGA

Concept

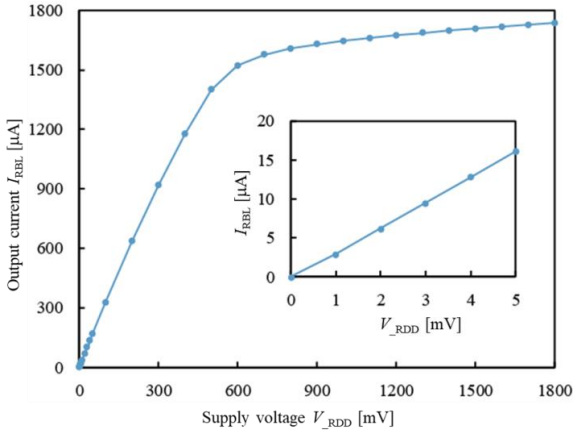


AQFP two-by-two logic cells

8T CMOS memory cell with AQFP read-out



Reduction of output current of a memory cell with reduced VDD



- CMOS memory is used as a rewritable ROM.
- Power consumption of CMOS is reduced by decreasing VDD.

Y. Okuma *et al.*, submitted to IEEE TAS.

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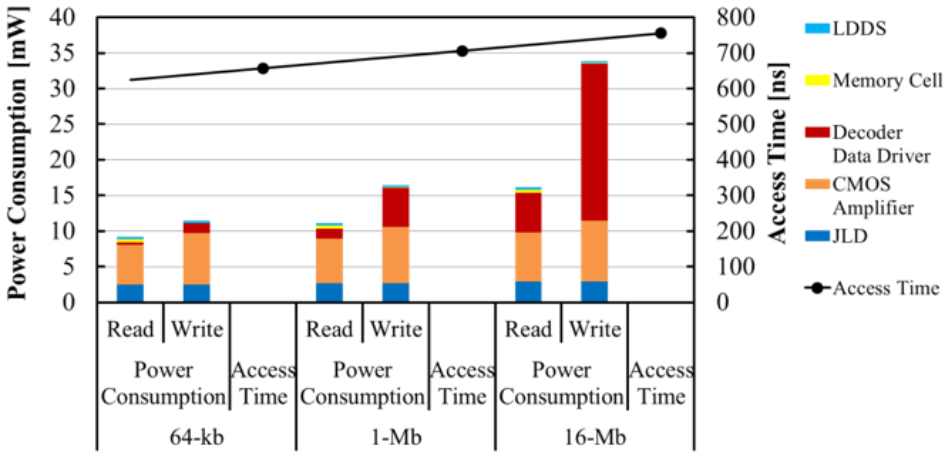
Issues in Josephson/CMOS Hybrid systems

- CMOS devices consume a lot of power.
  - 10^5 times larger than AQFP
    - Use of low V_{TH} process
    - Use of adiabatic decoder
    - Use of new amplifier (nTron)



- Connection between Josephson and CMOS devices.
  - Use of flip chip bonding : ~100 pads/1 mm^2
  - Use of monolithic Josephson/CMOS fabrication process

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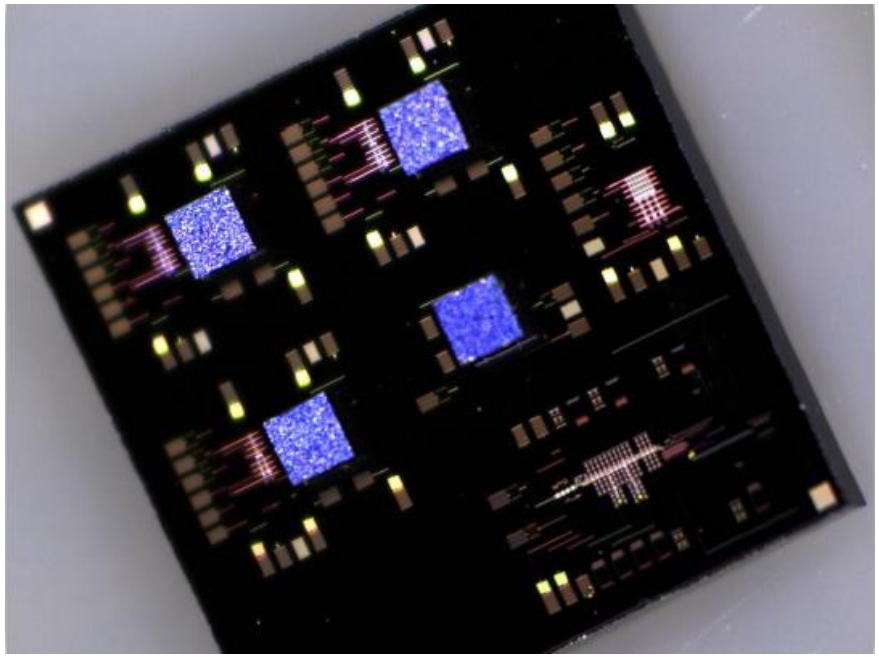
Flip-chip Bonding/ Monolithic Process

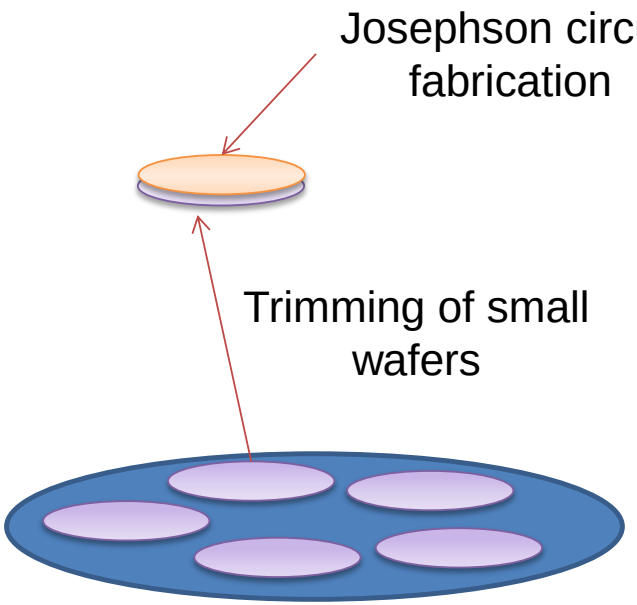
Hybrid integration of AQFP and nTron chips



Curtesy of Prof. Ortlepp and Prof. Berggren.

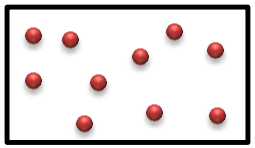
T. Ortlepp *et al*., ISEC2019, Riverside.

Monolithic integration of AQFP and CMOS circuits



Landauer's Principle

Thermodynamic entropy = Information entropy



101100010100110

- Equivalence between thermodynamic entropy and information entropy
- For computation reducing the information entropy, the minimum bit energy, $E_{bit} = k_B T \ln 2$, is consumed.
- For computation conserving the information entropy, there is no minimum limit of bit energy in computation.

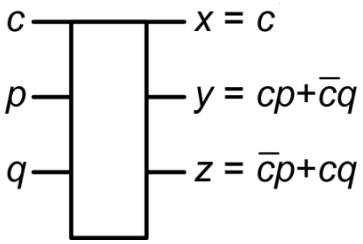
R. Landauer, *IBM Journal of Research and Development* 5, 183 (1961).
C. H. Bennett, *IBM Journal of Research and Development* 17, 525 (1973).

Reversible Computing

- The entropy is conserved during computation.
- Logical reversibility is required.

Physical reversibility, bi-directionality is also required.

Fredkin gate



Input			Output		
c	p	q	x	y	z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

E. Fredkin and T. Toffoli, *Int. J. Theor. Phys.* **21**, 219-253 (1982).

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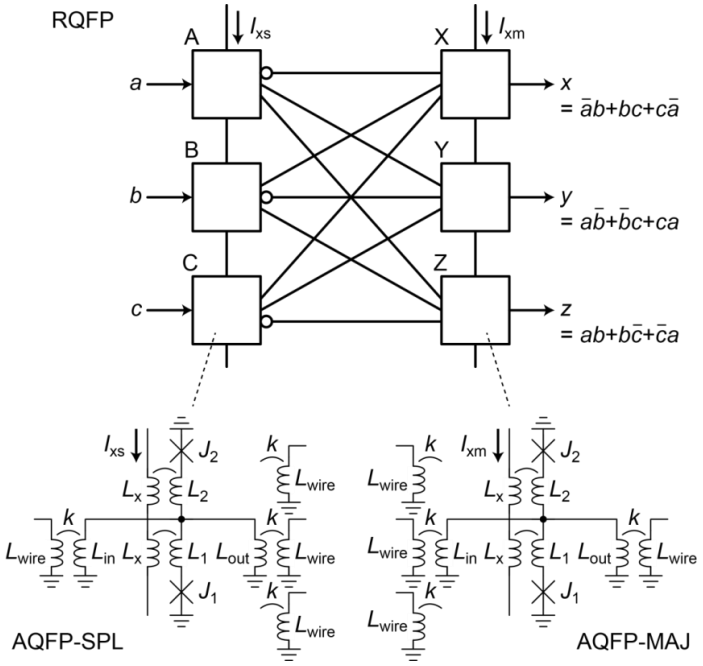
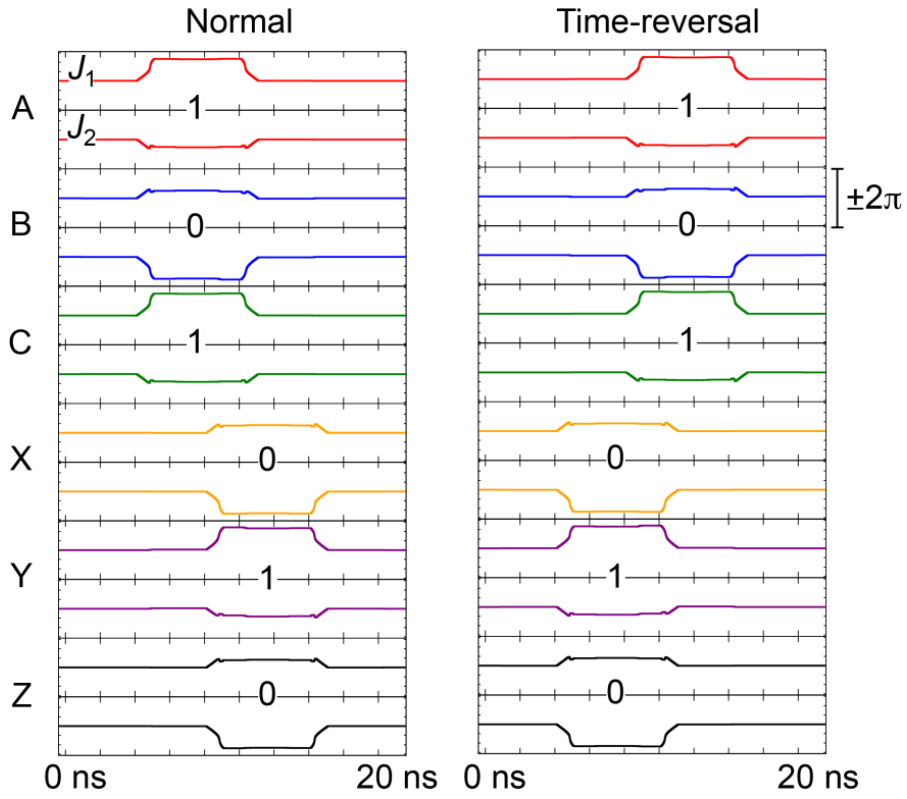
Reversible AQFP (RQFP)

Reversible majority QFP gate



Reversible majority QFP gate



A logically and physically reversible gate can be achieved by using AQFP gates.

N. Takeuchi, *et. al.*, *Scientific Reports* 4, 6354 (2014).

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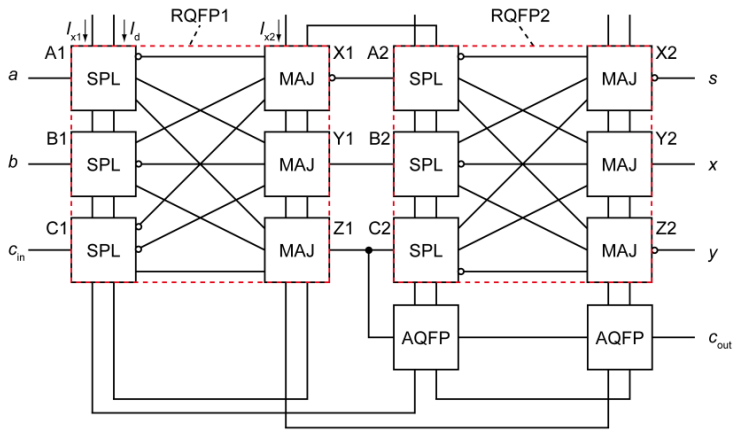
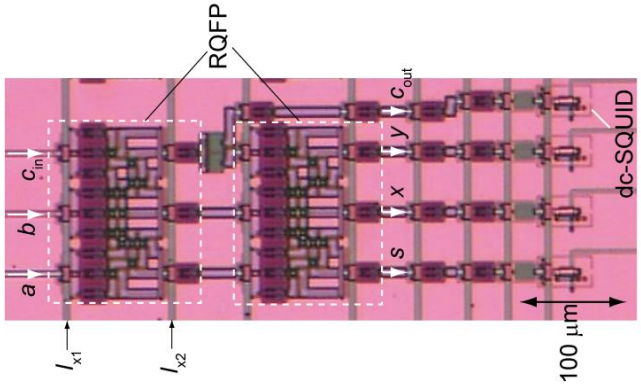
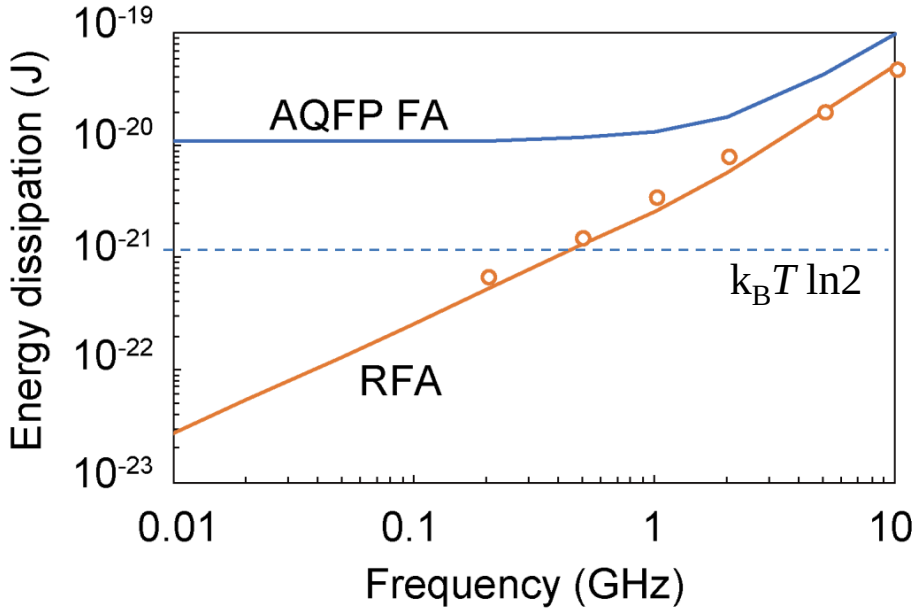
Reversible AQFP Adder

Schematic of 1b full adder





Energy dissipation of 1b full adder



Bit energy smaller than k_BTln2 is possible in RQFP circuits.

RQFP register file, see Yamae et al. ISEC 2019, Riverside.

Fabricated by AIST HSTP

CRAVITY AIST

T. Yamae *et al.*, SUST, 32, 035005 (2019).

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Summary

- Two outstanding features of superconducting logic circuits:
  - High-speed SFQ logic circuits
  - Energy-efficient AQFP logic circuits
- Memories are key devices for digital applications.
  - Hybrid Josephson-MOS memory has its potential.
- More energy-efficient logic circuit is possible by using RQFP.