IEEE/CSC & ESAS EUROPEAN SUPERCONDUCTIVITY NEWS FORUM, No. 22, October/November 2012
The published version of this preprint appeared in IEEE Transactions on Applied Superconductivity 23, 1100305 (June 2013).

Subgap Leakage in Nb/Al-AlO$_X$/Nb Josephson Junctions and Run-to-Run Reproducibility: Effects of Oxidation Chamber and Film Stress

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***Abstract*—Many applications of Nb/Al-AlO$_x$/Nb Josephson junctions (JJs) in superconducting electronics require high quality tunnel barriers with low subgap leakage that is usually characterized by figure of merit $V_m=I_cR_{sg}$, where I_c is the critical current and R_{sg} is the subgap resistance at 2 mV and 4.2 K. It is widely believed, and there is considerable literature suggesting, that quality and reproducibility of JJs depends critically on the intrinsic stress in Nb/Al-AlO$_x$/Nb trilayers, and the stress therefore should be carefully minimized and controlled. Contrary to this belief, we show that JJ quality (V_m) and reproducibility do not depend on the stress in the trilayer, at least in the studied range from -300 MPa to 300 MPa. In this range, V_m neither depends on the stress in Nb/Al base electrode nor in Nb counter electrode. We have found, however, that V_m crucially depends on the way the tunnel barrier formation by thermal oxidation of Al is done. For instance, room-temperature dynamic oxidation (in O_2 flow at low pressures) in a cryopumped chamber leads to poor run-to-run reproducibility of V_m and reduced V_m values, whereas dynamic oxidation at the same parameters but in a chamber with turbomolecular pump results in high V_m values and excellent run-to-run reproducibility.**

***Index Terms*—Nb/Al-AlO$_x$/Nb Josephson junctions, AlO$_x$ tunnel barrier, subgap leakage, intrinsic stress, hydrogen in Nb, hydrogen chemisorption, superconducting digital circuits.**

I. Introduction

JOSEPHSON TUNNEL junctions based on Nb/Al-AlO$_x$/Nb trilayer technology are the key elements of superconductor electronics both digital and analog. Many applications of Josephson junctions (JJs) require high quality tunnel barriers with low subgap leakage current, e.g., for superconducting qubits, detectors, SIS mixers, etc. The junction quality is usually characterized by figures of merit $V_m=I_cR_{sg}$ or R_{sg}/R_N where R_N is the junction normal state resistance and R_{sg} is the subgap resistance usually measured at 2 mV and 4.2 K. Digital superconductor electronics utilizes mainly externally shunted JJs in integrated circuits and high values of V_m or R_{sg}/R_N ratio may seem to be not important. However, high subgap leakage (low V_m and R_{sg}/R_N) indicates the presence of defects and/or nonuniformities in the tunnel barrier, creating channels with higher barrier transparency. Because these defects are usually induced during the fabrication process and by some often unknown and poorly controlled factors, the concentration of these defects may vary randomly from run to run, causing poor run-to-run reproducibility of JJ parameters. Also, statistical variations in the concentration of these defects may lead to nonuniformity (spreads) of junction parameters across wafers. Since low parameter spreads and high run-to-run reproducibility are required for high-yield manufacturing of digital circuits with very large integration scale (VLSI), it is likely that high V_m of JJs is also highly beneficial for applications in superconducting VLSI circuits.

Although nowadays Nb/Al-AlO$_x$/Nb tunnel junctions are made everywhere by virtually identical processes, similar to the original trilayer process developed by Gurvitch et al. [1], the resultant junction quality (V_m) varies among different groups and from run to run, apparently depending on the equipment used and some unknown process details. There have been a considerable number of publications devoted to finding correlations between the junction quality and the details of the fabrication process. For instance, minimization of the residual stress in Nb films and the associated surface roughness of Nb were identified as the most important process optimization tasks [3]-[13]. Other key factors were identified as Nb deposition rate [3,][4,], Nb and Al thicknesses and uniformities [2],[3],[14], substrate temperature and films' surface temperature after their deposition [2], [13]-[15].

Most of the results on the junction quality and its relation with fabrication parameters have been obtained on trilayers deposited on relatively small, 1" to 4", substrates and using relatively small number of processed wafers, often just a few. Therefore, statistical data on the reproducibility of JJ quality at a fixed set of optimized deposition parameters and on run-to-run variation of V_m are absent. However, making VLSI superconducting circuits would require processing of large quantities of large-diameter wafers, 150 mm and preferably 200 mm, in a way that provides high reproducibility of all junction and circuit parameters.

By running a tightly controlled commercial process for Nb superconducting circuits over a number of years we have been able to accumulate statistics on the quality of Nb/Al-AlO$_x$/Nb JJs made on 150-mm wafers and correlate it with various fabrication parameters. Contrary to the earlier data, we have

Manuscript received October 9, 2012. This work was supported in part by ONR under Grant N00014-09-1-0079.

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The published version of this preprint appeared in IEEE Transactions on Applied Superconductivity 23, 1100305 (June 2013).

found that V_m is independent of the intrinsic (residual) stress in the trilayers, and/or Nb films forming the trilayers, in a broad range of stresses inside ± 300 MPa interval. We have found that equipment used to conduct oxidation of Al layer to form aluminum oxide, AlO_x tunnel barrier has dramatic effect on V_m and its reproducibility. This effect is much more significant for high volume manufacturing than previously identified effects such as stress, deposition rates, film morphology, deposition temperature, etc. [2-15].

II. Fabrication Process and Testing

A. Trilayer Deposition and Aluminum Oxidation

Josephson junctions have been fabricated on 150-mm wafers by the HYPRES process for superconductor electronics [16], [17]. Nb/Al-AlO_x/Nb trilayers were deposited on oxidized Si wafers containing patterned Nb ground plane layer covered by a 150-nm layer of SiO_2 dielectric with patterned holes for making contacts between the base electrode layer of trilayer, M1 and the ground plane, M0. The thicknesses of layers were 160 nm, 8 nm, and 50 nm for, respectively, Nb base electrode (BE), Al, and Nb counter electrode (CE). Depositions were done in a cryo-pumped custom-made system (from Kurt J. Lesker Comp.) with a load-lock and base pressure of $1 \cdot 10^{-8}$ Torr ($1.3 \cdot 10^{-6}$ Pa), using 6" sputtering guns. Deposition parameters were optimized to target zero stress in Nb films; dc magnetron power was 4 kW, giving sputtering rate 1.4 nm/s at Ar pressure 8.5 mTorr (1.13 Pa). Also, all the precautions described in [1]-[15] were used to minimize the surface temperature of the films. Wafers were clamped to a copper pallet water-cooled by a recirculating chiller at 11 °C. Surface temperature of the films during the depositions was always below 50 °C as was verified by independent measurements. Nevertheless, the wafers were allowed to cool between Nb and Al depositions in flowing Ar gas for 10 min.

Dynamic oxidation of Al layer in flowing oxygen was used to produce the tunnel barrier. Oxidation time was always kept at 15 minutes, and a constant pressure was maintained to produce trilayers with two target Josephson critical current densities, (j_c = 4.5 kA/cm^2 and 1.0 kA/cm^2), respectively, 20 mTorr (2.66 Pa) and 175 mTorr (23.3 Pa). Static oxidation at 2 Torr was used to target j_c of 30 A/cm^2.

Two types of dynamic oxidation processes were used. The first type was done in the cryopumped deposition chamber equipped with a CTI-8 cryopump. The second type was done at identical parameters but after transferring the wafer in a separate chamber equipped with turbomolecular pump (TMP). In both cases the pump was throttled during the oxidation to reduce its pumping speed and maintain the desired oxidation pressure. The static oxidation was done only in the deposition chamber with completely closed gate valve on the cryopump.

Trilayers were deposited one at a time, allowing for at least 24-h pumping time between consecutive wafers. On average, two-three trilayers per week were deposited.

B. Junction Definition and Further Processing

Josephson junctions of circular shape were defined by deep-UV photolithography using 1x projection aligner and AZ 5214E photoresist. For making submicron junctions, trilayers right after the deposition were coated by a 30-nm layer of SiN_x deposited by PECVD at 180 °C. Then 248-nm photolithography was done using Canon FPA 3000-EX4 stepper, Fuji chemically amplified photoresist (PR) and bottom antireflection coating (BARC). Junction sizes on test chips were varied from 1 μm to 4 μm in the first case and from 0.3 μm to 4 μm in the second case.

Counter electrode (CE) (and SiN_x) etching was done in Samco RIE-10NR reactive ion etching system in SF_6 at 4 Pa and 120 W rf power, and controlled by optical end-point detector. After the etching, the exposed surface of aluminum-covered base electrode and junction side walls were anodized (with photoresist etch mask still on [18]-[21]) using anodization voltage of 21 V and ammonium pentaborate solution in ethylene glycol as electrolyte. For submicron JJs, SiN_x layer on CE prevented leaching of electrolyte under BARC/PR stack due to much better adhesion to Nb. Thus produced anodic oxide seals the interior of junctions and protects tunnel barrier from possible damage during further processing. Patterning of the base electrode follows next, and all the following processing steps are identical to those described in [16], [17].

A special care was taken not to induce plasma processing damage to junctions [22], and protective structures described in [23] were used on the test chips. Also, all the precautions were used to minimize hydrogen contamination of Nb and its effect on JJs [24]-[26].

C. Stress Measurements and Junction Testing

Stress in the deposited trilayers was measured using laser scanning stress and wafer bow measurements system FSM 128 from Frontier Semiconductor, Inc. Stress maps were built using over 20,000 points taken at 12 scans along the wafer diameter with wafer rotated about 15° after each scan. Local stress at each point was calculated using local wafer curvature before and after the deposition and the Stoney's formula. Wafer-averaged stress data will be presented below.

In order to determine stresses in the base and the counter electrodes separately, the stress measurements were repeated right after the counter electrode etching and before anodization. The remaining area of the counter electrode after CE etching (total JJs area) is ~ 1%. Hence, the change in the wafer curvature with respect to the pre-deposition state is overwhelmingly caused by the stress in Nb/Al-AlO_x base electrode. This measurement gave us the wafer-averaged stress in the BE. On the other hand, change in the local curvature with respect to the post deposition state, gave the stress in the etched CE.

Stress measurements were repeated once again after BE anodization in order to see if the anodization induced any additional stress [26]. After patterning of the base electrode, wafer shape nearly returns to its original pre-deposition state.

Current-voltage (*I-V*) characteristics of single junctions and series array of junctions were measured in LHe in a magnetically shielded set-up. $V_m = I_c R_{sg}$ was determined using

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the measured dc current at 2 mV, R_{sg} = 2 mV/I_{sg}(at 2 mV). Since this current is a sum of the subgap leakage and averaged Josephson oscillations, thus calculated V_m presents the lower limit of the true V_m (at Josephson current suppressed by magnetic field) and somewhat underestimates the junction quality. Five process monitors chips were tested from each wafer; they were located in the center of wafer and in the middle of each of 4 quadrants. V_m value averaged over these five locations will be used in the discussions below. More details of the parametric testing are given in [27].

III. Results

The typical *I-V* characteristics of JJs of different size are shown in Fig. 1.

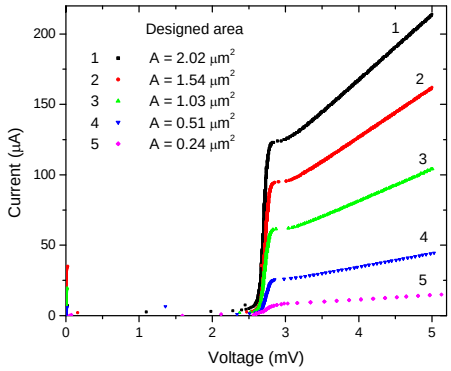

Fig. 1. Typical current voltage characteristics of circular Nb/Al-AlO$_x$/Nb junctions of different area. Junctions were defined by 248-nm lithography and SiN$_x$/BARC/PR mask for etching and anodization.

Junction normal state conductance, G_N, scales linearly with the junction designed area as shown in Fig. 2(a). Similarly, *I-V* characteristics scale perfectly with normal state resistance, indicating that JJ properties (in particular V_m) do not depend on the junction size (see Fig. 2b).

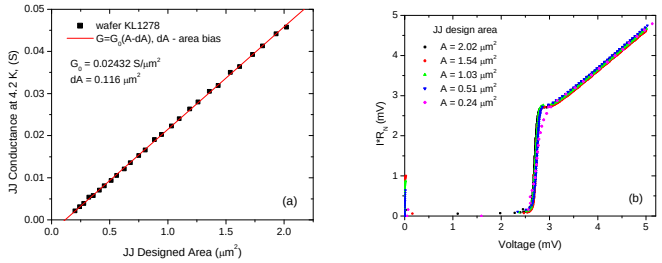

Fig. 2. (a) Normal-state conductance of JJs with different area; (b) scaling of *I-V* characteristics of JJs shown in Fig. 1 with junction normal resistance, R_N.

Despite a tight control over the deposition parameters, residual intrinsic stress in deposited trilayers, σ_{tri}, varied substantially from run to run as shown in Fig. 3(a) for the studied set of 70 wafers. Similarly, the stress in Nb/Al-AlOx base electrode, σ_{BE} , also varied as shown in Fig. 3(b). Stress in the counter electrode, σ_{CE}, is shown in Fig. 3(c). It can be seen that whereas both σ_{tri} and σ_{BE} varied, more or less randomly, from tensile to compressive, the counter electrode stress stayed tensile for most of the wafers in the studied set. There is a perfect correlation between σ_{BE} and σ_{tri}, as shown in Fig. 4. Best fit gives the following relation between both stresses in MPa

$$\sigma_{tri} = 0.826\ \sigma_{BE} + 20.7 \qquad (1)$$

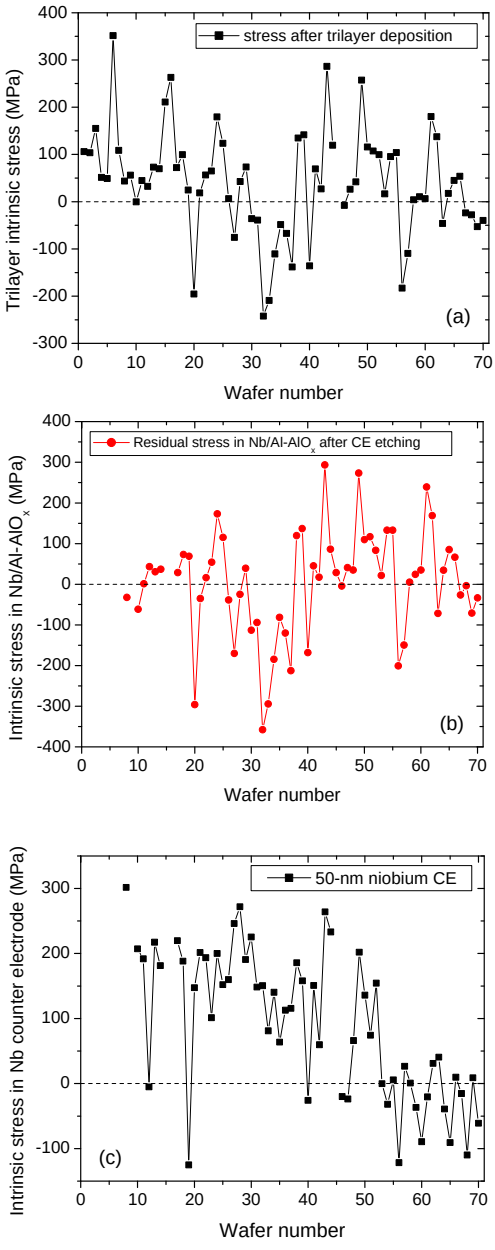

Fig. 3. Residual (intrinsic) stress in deposited trilayers (a), their base electrode (b), and counter electrode (c). In this set, the average trilayer stress is 40.5 MPa, average BE stress is 2.8 MPa, and average CE stress is 91.5 MPa.

In the simplest model, the total stress in a multilayer is related to stresses in individual layers as $\sigma_{tot}\sum t_i = \sum \sigma_i t_i$, where t_i is thickness of the *i*-th layer. Using the actual thicknesses of layers and taking Al layer into account, this becomes

$$\sigma_{tri} \approx 0.736\sigma_{Nb\ BE} + 0.036\sigma_{Al\text{-}AlOx} + 0.227\ \sigma_{CE} \qquad (2)$$

From direct measurements of the stress in Al films we concluded that the second term in Eq. (2) is within ± 20 MPa range and thus can be neglected. So the stress in BEs was mainly due to the intrinsic stress in Nb layer, whereas the

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stress in a thinner Nb layer of CE was shifted on average to more tensile. Therefore, for many studied wafers, a near zero total stress in trilayers resulted from a mutual compensation of the mainly compressive stress in the BE and a mainly tensile stress in the CE.

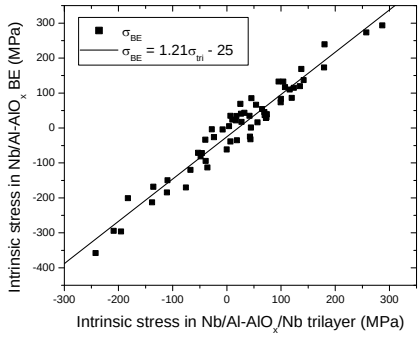

Fig. 4. Correlation between the stress in trilayer, σ_{tri}, and stress in trilayer base electrode, σ_{BE}.

A. *Intrinsic stress and V_m*

The stress data presented above included wafers with three target current densities 4.5, 1.0 and 0.03 kA/cm^2. For V_m analysis it makes sense to compare only wafers with the same j_c (the same tunnel barrier thickness), e.g., j_c = 4.5 kA/cm^2. Independently of the j_c, we have not found any correlation between the intrinsic stress and V_m.

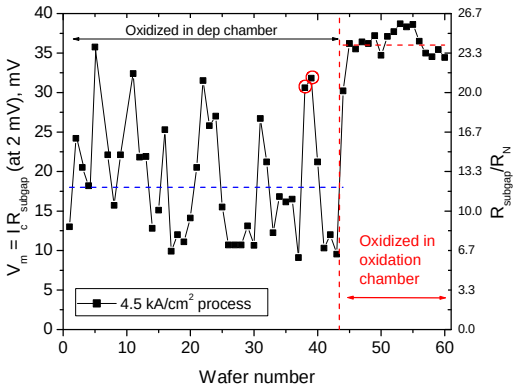

Fig. 5. Run-to-run variation of the wafer-averaged V_m for a set of wafers with j_c=4.5 kA/cm^2. The first 43 wafers, except the two indicated by circles (#38 and #39), have tunnel barriers produced by Al oxidation in the cryopumped deposition chamber. For wafers #38, 39 (indicated by circles) and 44 - 60, Al was oxidized in a separate oxidation chamber with a TMP. Horizontal dash lines show the average V_m for the each type of oxidation processes.

What we have found, however, is a strong dependence of V_m on the way the tunnel barrier was produced. For trilayers with Al layer oxidized in the deposition chamber, V_m varied randomly from run-to-run and was on average a factor of two lower than for trilayers oxidized in a separate chamber, as shown in Fig. 5. Also, the run-to-run variation of V_m for the latter type of trilayers is a factor of 6 less than for the former. Specifically, the average <V_m> and standard deviation are 18 mV and 40% for the first set, and 36 mV and 7% for the second set of wafers, respectively. We emphasize that the place of Al oxidation was the only difference and all other processing steps for the both sets of wafers were identical.

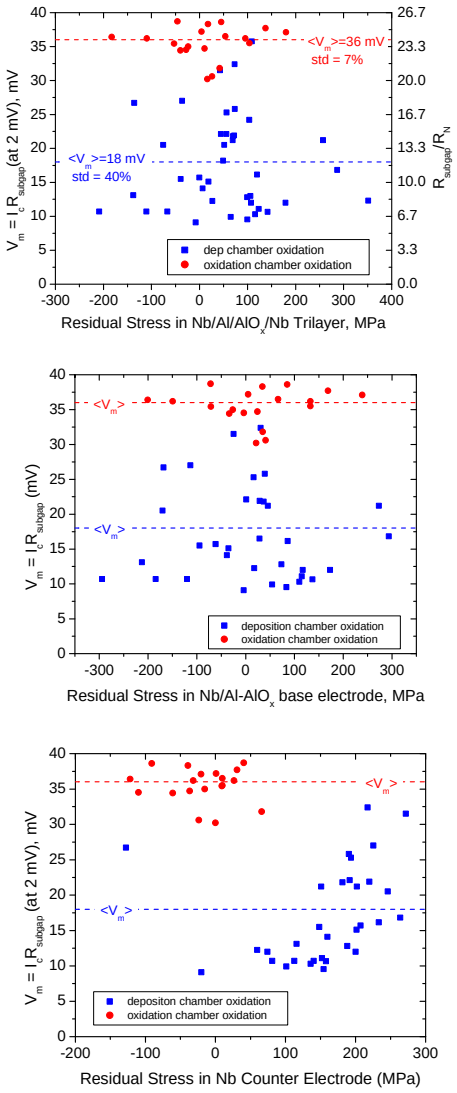

Fig. 6. Junction quality parameter V_m *vs* intrinsic stress in, from top to bottom, trilayer, Nb/Al-AlO$_x$ base electrode, and Nb counter electrode for barriers oxidized in the deposition chamber and in the oxidation chamber. There is no correlation between V_m and the intrinsic stress in any of the layers forming the trilayers in the studied range of stresses. However, there is a strong dependence of V_m on the set-up used for oxidation (oxidation chamber and the type of pump).

IV. Discussion

The important difference between the two types of chambers used for AlO$_x$ barrier formation is the pump used to pump away the flowing O_2: cryopump for the oxidation in the deposition chamber and TMP for the oxidation chamber. We suggest that this difference may result in the different concentration (partial pressure) of hydrogen during and after oxidation. While pumping O_2 during the dynamic oxidation, the temperature of the cold head of the cryopump increases. This can cause desorption of adsorbed hydrogen accumulated in the cryopump due to low condensation temperature of H_2 and low adsorption energy. Hydrogen can back-stream into the deposition chamber during and after the oxidation, and promote creation of some structural defects in AlO$_x$ tunnel

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barrier, which locally increase its transparency. For instance, it is known that dissociative chemisorption of H_2 takes place on aluminum oxide surface, resulting in formation of O-H and Al-H bonds which remain stable up to high temperatures under ultrahigh vacuum conditions. Adsorbed hydrogen affects also the structure and adhesion properties of the oxide surface [28]-[30]. With a TMP, the hydrogen pumping efficiency is almost the same as for N_2, and there is no possibility of H_2 desorption from the pump. So the concentration of H_2 in the oxidation chamber is expected to be lower and hence lower is the concentration of H-related defects inside the oxide tunnel barrier and of O-H bonds at the interface with Nb counter electrode. The proposed explanation needs further examination by analytical methods.

V. Conclusion

By studying a set of 70 wafers, we have found that intrinsic stress in Nb/Al-AlO_x/Nb trilayers and comprising layers has no effect on the quality of Josephson junctions. We have found, however, a dramatic effect of the oxidation conditions on JJ quality (V_m): the use of a TMP-pumped oxidation chamber instead of a cryopumped chamber resulted in a factor of 2x increase of the average V_m of tunnel junctions and a factor of 6x improvement of run-to-run reproducibility. We attributed the found effect to differing degree of hydrogen chemisorption during and after AlO_x barrier formation by dynamic oxidation of aluminum in different chambers.

Acknowledgment

We would like to thank Dr. Deborah Van Vechten for the interest and support of this work and Dave Donnelly for the technical support and maintenance of processing equipment. We also would like to thank Alexander Lochbaum, Simon Buehler, Saad Sarwana, and Anubhav Sahu for testing process monitors with Josephson junctions.

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