

# Planarized, Extendible, Multilayer Fabrication Process for Superconducting Electronics

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**Abstract**—We report on technique and results for superconductor electronics fabrication process, featuring customizable number of planarized superconducting layers. The novel technique enhanced yield on stackable vias of our standard planarized process (RIPPLE) by eliminating the need for an additional deposition of Aluminum as an etch stop in the metal-via stack. The drawback of the previous approach was the difficulty in processing Aluminum using either wet or dry etch mechanisms. Here, we discuss details of the novel fabrication process flow and its realization for 4.5 kA/cm<sup>2</sup> fabrication process with six Nb layers with two fully planarized layers. We report test results of various planarization diagnostics structures, accounting the influence of topology on Josephson junction quality, as well as yield and critical current of via stacks. We also report on inductance measurement results providing information on interlayer dielectric thickness for planarized layers; confirming a good uniformity over the wafer. Basic components of superconducting logic such as dc/SFQ, SFQ/dc converters, Josephson transmission lines (JTLs), and simple digital circuits such as half-adder (HA) have been designed, fabricated and tested using either conventional (RSFQ) or energy-efficient (ERSFQ) approach. The ERSFQ HA cells with bias inductors fabricated in two planarized layers were shown to function with the operational margins of +/-22%.

**Index Terms**— Superconducting integrated circuits, Josephson junction fabrication, stackable vias, planarization

## I. INTRODUCTION

HIGH ENERGY consumption of modern digital electronics became the major impediment for further scaling of high-end computing systems. To solve this problem, new circuit technologies with high energy efficiency were required. This spurred the renewed interest in superconducting circuits capable of operation with very low energy and high speed [1, 2]. Recently, superconducting single flux quantum (SFQ) circuits progressed to even lower power versions with zero-static power dissipation making them highly competitive for application in next generation energy-efficient computing systems [3-6]. However, the practical realization of superconducting digital circuits for high-end computing requires a significant increase in circuit complexity and gate density. Conventional SFQ integrated circuit fabrication technology has been proven to deliver SFQ digital ICs with tens of thousands Josephson junctions (JJs) per die [7, 8] using a fabrication process with just 4 superconducting layers and

relatively coarse (1.0  $\mu\text{m}$ ) lithography with 1.5-2  $\mu\text{m}$  minimum JJ size [9, 10]. Further increase in integration density and scale of superconducting ICs will require finer lithography to reduce size of all circuit components including JJs, vias, thin-film inductors, thin-film resistors, and interconnects, with increasing impact on circuit density, respectively. The biggest gain in the IC integration scale can be achieved by adding more superconducting layers using layer planarization techniques. Japanese Advanced Process (ADP) has demonstrated up to 10 Nb layers with submicron JJ size using planarization based on chemical mechanical polishing (CMP) [10-12]. A planarized superconducting fabrication process is also being developed at MIT Lincoln Lab [13].

In order to get the expected payoff in circuit density by adding superconducting layers, one has to have stackable vias (so-called plugs) allowing connection between multiple metal layers with minimal parasitic inductance while not compromising circuit area. This has been a difficult problem requiring the development of special fabrication techniques [12, 13].

HYPRES has been developing a higher integration density fabrication process by using both finer (250 nm) lithography [14, 15] and CMP planarized superconducting wiring layers. In this paper, we first discuss the approach and method we implemented for extending the number of superconducting layers in our standard 4-layer fabrication process. Then, we describe the technique we devised to fabricate and increase the yield of stackable vias. Also, we describe various process control monitor chips (PCMs) and simple digital circuits used for process development. And finally, we present and discuss results from the PCMs and digital circuits fabricated with the developed process.

## II. PLANARIZED FABRICATION PROCESS

Our planarized fabrication process technique is based on modification of Caldera planarization process [16] featuring pattern-independent interlayer dielectric planarization. This technique allows faster planarization with integrated in vias plugs. It is further referred to as Rapid Integrated Planarized Process for Layer Extension (RIPPLE).

### A. Caldera Planarization Based Process (RIPPLE)

Fig. 1 shows a cross-section of the developed planarized process. For compatibility with HYPRES' legacy (non-planarized) 4-layer process [17], we put additional wiring layers underneath the ground plane (layer M0). These

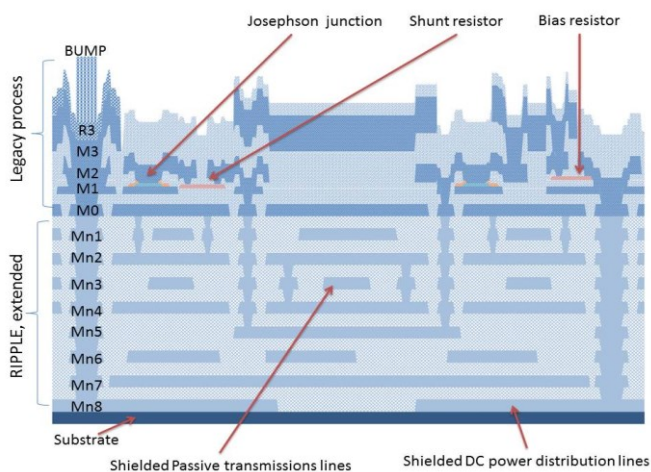


Fig. 1. Layer cross-section of the twelve superconducting metal layer process. Four metal layers (M0-M3) are left from the conventional legacy process and eight extended layers (Mn1-Mn8) are added using RIPPLE.

“underground” layers (Mn1 - Mn8, in Fig. 1) illustrate the extendible nature of RIPPLE. Naturally, “n” in the extended layer name stands for “negative”. By now, HYPRES has successfully implemented a process with only two extended superconducting layers (Mn1 and Mn2). As we will show below, there is not any evident obstacle for extending the number of wiring layers.

The process starts with a sputter deposition of Nb/Al/Nb trilayer (200 nm / 10 nm / 200 nm film thicknesses), where the top Nb film is used to define via plugs, the bottom for the wiring layer, and Al in between them as an etch stop. The first step is the via (In1) plugs definition done by etching the top niobium layer in SF<sub>6</sub> chemistry with hard etch stop on the Al layer (Fig. 2a).

The next step is removing residual aluminum. This can be accomplished by using either wet-etch or dry-etch process. The most reliable wet etch process, in our experience, is the one using ion-free metal developer at the etch rate of 5 nm/min, while the dry etch we were doing either by inductively coupled plasma reactive ion etch (RIE) in chlorine chemistry or by ion beam milling. Despite the demonstrated success, this step has some problems that will be discussed in the next section.

The next step is a deposition of 200 nm interlayer dielectric (SiO<sub>2</sub>), done with PECVD (Fig. 2b) that conformally covers the entire wafer with a 200 nm thick SiO<sub>2</sub>. Then, the wafer is patterned with a complementary to the metal pattern (Mn1) mask biased by 0.2- $\mu$ m for misalignment compensation (Mn1c). The mask has been generated automatically, omitting smaller than 0.6  $\mu$ m objects. All SiO<sub>2</sub> on top of the metal, except for a narrow ( $\sim$  0.2  $\mu$ m) rand, is etched away in CHF<sub>3</sub>/O<sub>2</sub> RIE chemistry. The resulting structure is shown in Fig. 2c. Then, the second interlayer dielectric is deposited on the entire wafer (Fig. 2d) with its thickness (200 nm) equal to the thickness of the plug layer (top Nb layer of the trilayer deposited during the first step).

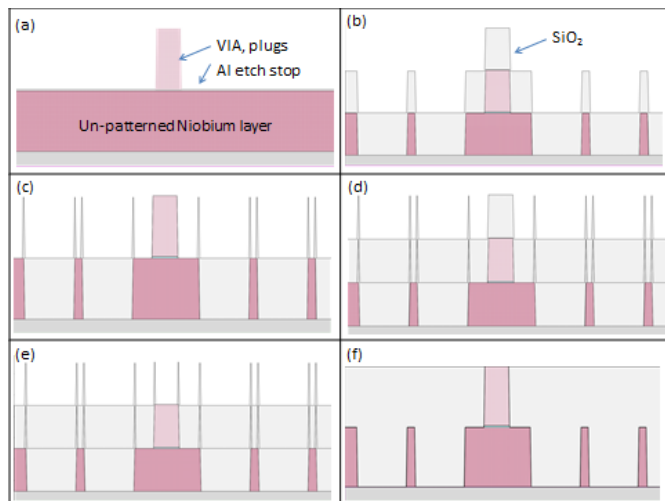


Fig. 2. Fabrication steps for adding one underground superconducting wiring layer (e.g., Mn1). (a) patterning via plugs (In1) with etch stop on Al and removal of Al. (b) defining Mn1 pattern and covering it with SiO<sub>2</sub>. (c) SiO<sub>2</sub> removal with RIE using biased Mn1 pattern. (d) Deposition of second SiO<sub>2</sub> layer. (e) SiO<sub>2</sub> on top of the plugs removal using biased In1 pattern (f) CMP planarization of the uniform spikes on top of metals/plugs.

In the next step, a mask, In1c, complementary to via mask In1, is used to pattern and remove SiO<sub>2</sub> from the top of via plugs (Fig. 2e). After this stage, the wafer is populated with 200-nm-thick by  $\sim$  200-nm-wide uniform structures (rand).

These pattern-independent structures can be easily removed from the entire wafer by chemical-mechanical planarization. The polishing rate for these structures is 3 times faster than the rate for a blanket film. The final planarized layer and a plugged via is shown in Fig. 2f. Even though the CMP step is the only step that doesn't have a direct method of determining the end-point, it has been made reliable by the pattern-independent nature of the technique. Moreover, only one CMP step is needed for defining a wiring layer and via plugs.

This sequence can be repeated for any given number of wiring layers, thus producing reliable fabrication process extension. The obvious advantage of this approach is that it is fully compatible with all designs made for the 4-layer process.

### B. Modified (Al-free via-plug) RIPPLE process

One of the requirements to a modern superconducting electronics foundry is very large (millions of gates per chip) scale integration [1]. This means a very high fabrication yield. The fabrication yield of the planarization process, introduced in the previous section, is mostly affected by the aluminum added as an etch stop for defining via plugs. Once via plugs are defined by RIE, the remaining aluminum has to be either removed or completely anodized. This step had proven to be un-reliable and prone to gross fabrication defects as shown in Fig. 3. All methods described above for removal Al suffice for comparably small integration scale, but none of them have proven to be suitable for VLSI process. The wet etch process is not compatible with submicron-size features, the ion-beam milling occasionally leaves residual Al at some locations, and chlorine ICP-IRE often creates residual polymer on the wafer. To mitigate this problem while keeping all advantages of the RIPPLE process, we found a way to avoid depositing Al.

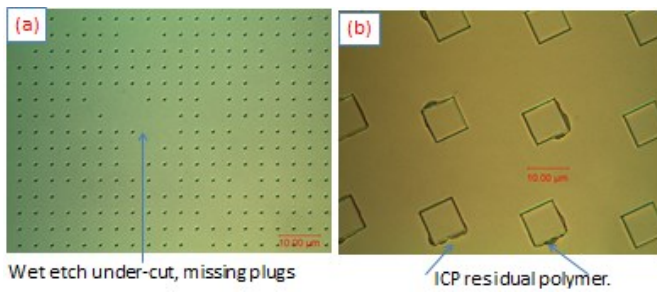


Fig. 3. Fabrication defects due to the processing of aluminum. (a) Wet etch undercuts plugs, quite a number of them missing from the array. (b) Residual polymer formation after etching aluminum in Chlorine ICP-RIE.

The simplest and successful approach was found to be the one that treats via plugs as a layer. The process starts with the deposition of 200 nm niobium thin film followed by via plugs patterning and definition (Fig. 4a). The next step is to deposit a 200-nm thick niobium film by sputtering (Fig. 4b). During this step, the via-plugs will get coated conformally and grow together with the wiring layer. At this stage, the wiring layer is patterned and defined the resulting structure is the one shown in Fig. 4(c). Then 200 nm PECVD SiO<sub>2</sub> (the same thickness as the wiring layer) is deposited, the resulting structure is exactly the same as the one shown in Fig. 2b, except for the aluminum. The rest of the process follows the RIPPLE steps described in the previous section. The other advantage of this process is elimination of the additional complementary mask for the via-plugs (In1c). This is possible because of the plug area having already been enlarged by the needed misalignment compensation of 200 nm during the deposition of the wiring layer. As a result, the same mask (In1) can be used with negative resist for etching ILD inside the via (as in Fig. 2e).

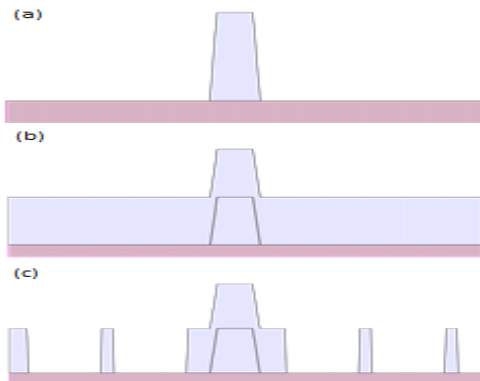


Fig. 4. Via plugs and underground superconducting wire defined without aluminum etch stop. (a) After the definition of the-via plug. (b) After the deposition of the metal layer. (c) After the definition of the wiring layer.

### III. SIX-LAYER PROCESS DIAGNOSTIC CHIPS

#### A. Design

A set of 5 mm by 5 mm diagnostic chips with process control monitors (PCMs) and various digital SFQ circuits has been designed and populated over the whole wafer to exhaustively characterize the fabrication process. The test structures include:

- Several arrays of nominally shunted JJs of different sizes in the range of interest used in RSFQ digital circuit

design for monitoring the critical current density and the over-etch (so-called missing radius).

- Several arrays of un-shunted JJs for monitoring trilayer quality, namely Nb gap voltage ( $V_g$ ) and sub-gap resistance ( $V_m$ ).
- JJ arrays placed over the edge of different combination of Mn1 and Mn2 layers for monitoring quality of planarization.
- A PCM realized as a 2- $\mu$ m mesh in Mn1 covered by the identical, 90° rotated mesh in Mn2 layer to access quality of planarized insulation between these layers (i.e., test for interlayer shorts).
- Array of 10,000 stacked vias between Mn2-Mn1-M0-M1 layers to measure their critical current and reproducibility of the planarized vias.
- Long gap test structures with gap sizes from 0.6  $\mu$ m to 1.6  $\mu$ m
- Inductance test structures [9] in Mn1 and Mn2 layers. These structures allow us extracting sheet inductance of the Nb film characterizing uniformity of ILD thickness along the wafer (i.e., uniformity of the planarization process).
- Test structures for stackable vias inductance measurement, characterizing uniformity of the plugs.
- A test bed for verifying the performance of passive transmission lines (PTLs) of various widths realized in different Mn2, Mn1, M1 or M2 layers and their combinations. Driver/receiver dc bias current margins measurement allows us to make selection of the optimal PTL for future use with 6-layer process.
- Various ERSFQ digital circuits, such as a half-adder (HA) cell [18, 19] designed in 6 layers, a single toggle flip-flop (TFF) and different-size static frequency dividers (SFD) for measuring maximum speed [20, 14], etc.

The functionality and bias margins of ERSFQ HA circuit with its main bias inductors and leads fabricated in Mn2 and Mn1 act as benchmark for HYPRES 6-layer planarized process.

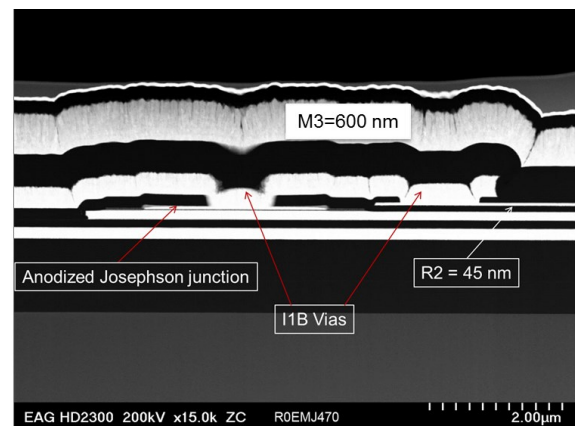


Fig. 5. Cross-section of a RIPPLE-2 – shows anodized Josephson junction with a shunt

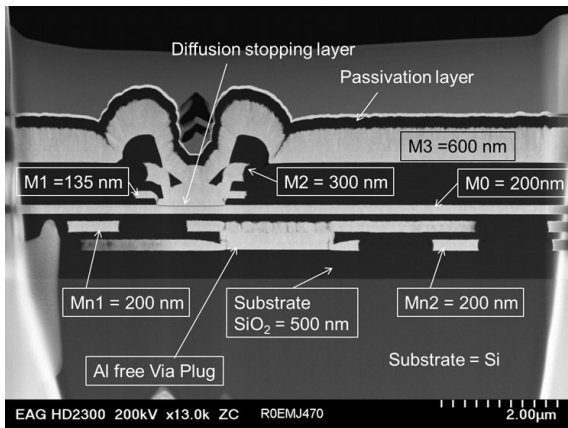


Fig. 6 Cross-section of RIPPLE-2, shows all the 6 six wiring layers, patented Hydrogen diffusion stopping layer and passivation layer

### B. Diagnostics Test Results

The diagnostic chips were fabricated with HYPRES' advanced 248 nm stepper, 6-layer 4.5 kA/cm<sup>2</sup> critical current density process. STEM cross-section of the process is shown in (Fig. 5 & 6). The first STEM details the 4-top unplanarized layers with the emphasis to the anodized Josephson junction and the bias resistor. The second STEM includes the planarized layers with an Aluminum-free via plugs, A layer introduced to stop the diffusion of Hydrogen [21, 22] and a passivation layer on top of the M3 layer.

The evaluation of PCMs and digital circuits, including functionality test and bias margins measurements, was performed with automated test system OCTOPUX [23]. The testing of unshunted JJs have shown Nb gap voltage  $V_g = 2.60 \pm 0.05$  mV and characteristic voltage ( $V_m$ ) in excess of 30 mV. The critical current of shunted Josephson junctions can be well fitted with  $I_c = \pi j_c (r-dr)^2$ , where  $r$  is the designed junction radius and  $dr$  is the process bias. Based on these measurements, we calibrate oxidation parameters for the trilayer fabrication and introduce on-mask compensation for the bias on the junctions. The variation in  $j_c$  with  $1\sigma$  within 3% and missing radius of  $dr = 0.8 \pm 0.2$  μm over 6-inch wafer was measured. The most aggressive test on planarization quality was done using a PCM with an array of 20 JJs where half the JJs were placed on the edge of the under-ground planarized layers. More than 98% of the arrays didn't show any degradation in critical current - all the JJs in the array show the same critical current. This further attests to the quality of the planarized layers.

We routinely test PCMs described in previous section, i.e. ILD shorts, Mn2-Mn1-M0-M1 stackable vias and gaps in all metal layers. The statistics collected over the wafer for the critical current of 10,000/200 Mn2-Mn1-M0-M1 stacked via plugs of design size 1.0-μm array are shown in (Fig. 7a). The 200 nm rand on top of the plug could make the via smaller (~0.6 μm) depending on whether rand was completely removed or not by CMP, correspondingly there is a big difference in current carrying capacity among the 20 chips characterized, the yield was 80% and the 16 chips current carrying capacity is plotted in Fig. 7a. Stacked via inductance and the spread is show in Fig. 7b.

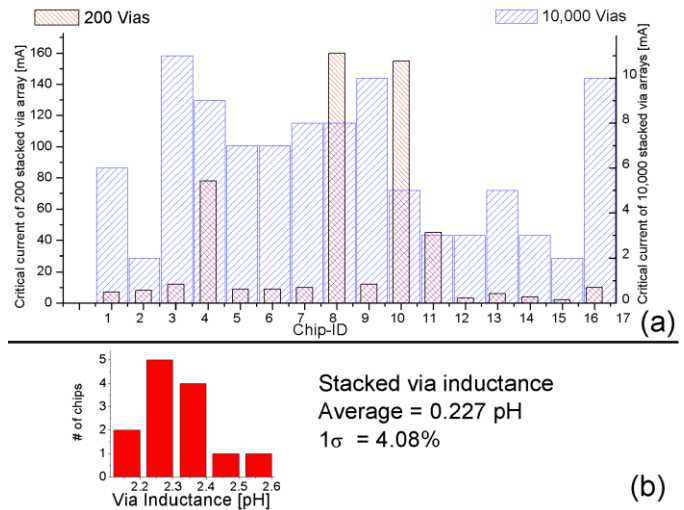


Fig. 7. Statistical data for critical current (a) of 10,000, 1.0-μm stacked vias between Mn2 and M1 layers and (b) Stacked via inductance spread.

Fig. 8 shows the sheet inductance variations for inductances fabricated in Mn1 and Mn2 layers, respectively. Sheet inductance depends only on dielectric thickness between Mn1/2 and M0 layers and Nb London penetration depth ( $\lambda_L$ ). By measuring a specific inductance of different-width lines, we extract sheet inductance and effectively monitor dielectric thickness uniformity along the wafer.

The variation of Mn1 and Mn2 inductances with  $1\sigma$  of about 6.0 % over 6-inch wafer was measured for both layers indicating good uniformity of RIPPLE planarization. An interesting fact is that the dielectric thickness between Mn2 and M0 layers has slightly better uniformity than the one between Mn1 and M0, despite the fact that it undergoes two CMP steps. This result is very encouraging and gives us confidence in increasing the number of superconducting layer beyond what is achieved with this work. The experimental data is in a good agreement with the theoretically predicted value of sheet inductance.

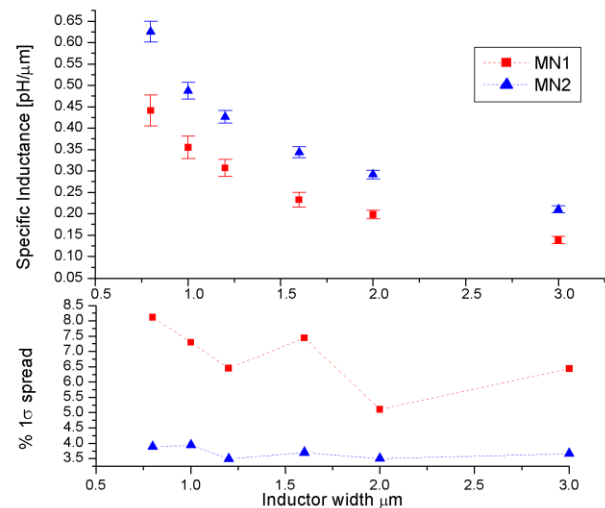


Fig. 8 (a) Inductance per unit length of Mn1 and Mn2 strip lines (in pH/μm) vs. the designed width (from 0.8 μm to 3.0 μm). The error bars represent  $1\sigma$  spread across wafer of the specific inductance value for the same width, (b) show the % deviations.

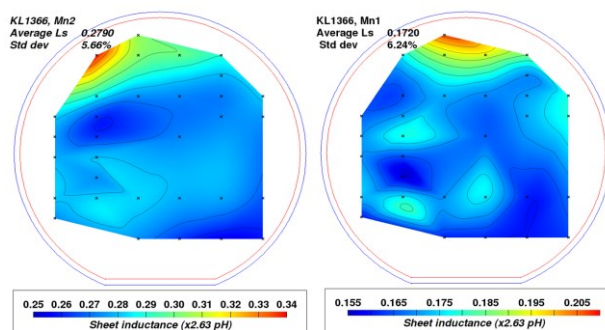


Fig. 9. Sheet Inductance ( $L_s$ ) in Mn2 and Mn1 layers spread map over 6-inch wafer.  $L_s$  (Mn2) = 0.279 (x2.63 pH)  $\pm$  5.66% and  $L_s$  (Mn1) = 0.172 (x2.63 pH)  $\pm$  6.24%

Fig. 9 shows specific inductance distribution across the wafer. The extracted sheet inductance spread across wafer from the specific inductance electrical cryogenic measurements is less than 7% across wafer for both planarized layers. The spread is exactly the same to what is measured in the fab using ellipsometer on a PECVD deposited  $\text{SiO}_2$  blanket wafer.

The correct functionality test for ERSFQ half-adder cells was observed with dc bias current margins in a range between  $\pm 6\%$  and  $\pm 22\%$ . We are going to routinely test a recently designed ERSFQ 8-bit parallel adder [24] as a chosen benchmark of moderate complexity.

#### IV. CONCLUSION

We have developed a new multi-layer planarization process for adding a custom number of superconductive wiring layers to HYPRES' legacy 4-layer fabrication process. The fabrication process based on a modified Caldera process features stackable submicron vias. The results of extensive testing of PCMs and diagnostics give us confidence in the process capability. Further development work is required to introduce planarized above ground plane layers, which is key in fabrication process that enable SFQ circuits to integrated with other type of circuits. The new extendible fabrication process allows the increase of scale integration of SFQ circuits.

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