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Fabrication Process and Properties of Fully-Planarized Deep-Submicron Nb/Al-AlO_x/Nb Josephson Junctions for VLSI Circuits

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Abstract—**A fabrication process for Nb/Al-AlO_x/Nb Josephson junctions (JJs) with sizes down to 200 nm has been developed on a 200-mm-wafer tool set typical for a CMOS foundry. This process is a core of several nodes of fully-planarized fabrication processes developed at MIT Lincoln Laboratory for superconductor integrated circuits with 4, 8, and 10 niobium layers. The process utilizes 248 nm photolithography, anodization, high density plasma etching, and chemical mechanical polishing (CMP) for planarization of SiO_2 interlayer dielectric. JJ electric properties and statistics such as on-chip and wafer spreads of critical current, I_c, normal-state conductance, G_N, and run-to-run reproducibility have been measured on 200-mm wafers in a broad range of JJ diameters from 200 nm to 1500 nm and critical current densities, J_c, from 10 kA/cm^2 to 50 kA/cm^2 where the JJs become self-shunted. Diffraction-limited photolithography of JJs is discussed. A relationship between JJ mask size, JJ size on wafer, and the minimum printable size for coherent and partially coherent illumination has been worked out. The G_N and I_c spreads obtained have been found to be mainly caused by variations of the JJ areas and agree with the model accounting for an enhancement of mask errors near the diffraction-limited minimum printable size of JJs. I_c and G_N spreads from 0.8% to 3% have been obtained for JJs with sizes from 1500 nm down to 500 nm to be utilized in Single-Flux-Quantum circuits with J_c from 10 kA/cm^2 to 50 kA/cm^2. The spreads increase to about 8% for 200-nm JJs. Prospects for circuit densities > 10^6 JJ/cm^2 and 193-nm photolithography for JJ definition are discussed.**

***Index Terms*—Nb/Al-AlO_x/Nb Josephson junctions, RSFQ, RQL, superconducting integrated circuit, superconductor electronics, self-shunted junction, 248-nm photolithography, minimum printable size, mask error enhancement**

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I. Introduction

Single-Flux-Quantum (SFQ) superconductor electronics (SCE) has many advantages over semiconductor electronics in energy efficiency, clock speed, and potential for reversible computing. Over the years, however, these advantages have mostly been unclaimed because of low integration scale and functionality of superconducting circuits. While the semiconductor industry maintained an exponential growth of electronic circuit density, the density of JJ circuits has remained nearly stagnant for the last 25 years. A popular excuse for this in the SCE community has been an insufficient funding of small companies and university groups developing SCE and lack of access to modern fabrication tools [1]-[3].

Achieving very large scale integration (VLSI) of more than 10^6 JJ/cm^2 requires decreasing the scale of all components to deep submicron. There have been a number of papers on submicron JJs [4]-[11] with both low and high critical current density, J_c. All of the work was done using e-beam lithography for JJ definition, producing a small number of JJs on small-size wafers for basic research of JJ properties, qubits, and circuit demonstrations requiring just a few, less than a dozen, JJs [12]. Therefore, there is no data and statistics on submicron JJs defined by modern steppers and scanners with 248 nm and 193 nm exposure wavelength, on a very large scale on 200-mm wafers.

The goals of this work have been to develop a robust fabrication process for Nb/Al-AlO_x/Nb junctions using a 200-mm tool set of a typical CMOS foundry, and to evaluate JJ quality, repeatability, and uniformity parameters on a large set of JJs in order to access the capabilities of JJ technology for superconducting VLSI circuits with more than 10^6 JJ/cm^2. This work is a part of broader efforts towards developing superconductor VLSI technology at MIT Lincoln Laboratory (MIT LL), which include increasing the number of niobium wiring layers from 8 in the current process [13] to 10, and decreasing the size of inductors [14], resistors, and vias [15].

II. Josephson Junction Fabrication Process

A. General process description

High-resolution photolithography requires high planarity of layers because of the small focus depth ~ $\lambda/(NA)^2$ of modern photolithography tools using a short exposure wavelength, λ,

and a high numeric aperture, *NA*, objective lens. Therefore, in the MIT LL fabrication process all layers are planarized using chemical mechanical polishing (CMP) of dielectric layers. Any metal layer is then deposited on a nearly flat surface with topography height not exceeding ~ 40 nm, except for etched vias in the dielectric which provide interlayer connections. A planarized stud-via process has also been developed [15] but was not used in this work.

Planarization allows also for placing the layer of junctions at any process level as they all become virtually identical and the choice is only dictated by SFQ circuit considerations. So, in our 4-metal-layer (4M) process, JJs are placed over one Nb ground plane layer, whereas in the 8-metal-layer (8M) process the JJ trilayer is above 4 planarized layers of Nb wiring, as shown in Fig. 1.

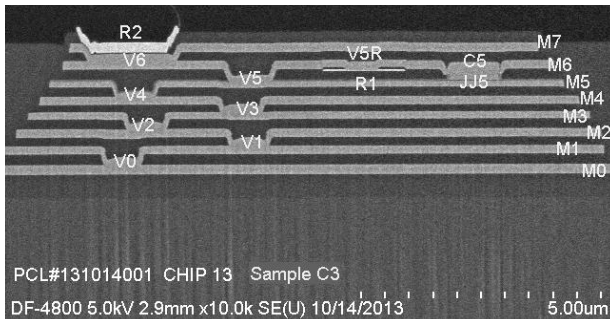

Fig.1 Cross-section of MIT-LL 8-metal layer fabrication process with 8 fully-planarized Nb layers marked as M0 – M7. JJ is marked JJ5, resistor R1, contact pad R2. Etched vias between adjacent layers are marked V0, V1, etc.

Nb/Al-AlO_x/Nb trilayers were deposited in-situ in a cluster tool with separate chambers for magnetron sputtering of Nb, Al, and for AlO_x formation by thermal oxidation. Nb base and counter electrodes were 150 nm and 250 nm, respectively, and the Al layer was 8-nm thick. The trilayer was deposited over a 200-nm thick planarized SiO_2 layer covering the bottom wiring layers M0-M4 of the 8M process or just one layer, M4, of the 4M process. 200-mm oxidized Si wafers were used, eight wafers per lot. Oxygen exposure (pressure·time) for oxidation was adjusted to target the following Josephson critical current densities: 10 kA/cm^2, 20 kA/cm^2, and 50 kA/cm^2 [16]. Most of the data were obtained for our main, 10-kA/cm^2 process, on hundreds of processed wafers, whereas the other two are intended for future process nodes.

B. Photolithography of submicron Josephson junctions

We used a Canon FPA-3000 EX4 stepper with 248 nm KrF excimer laser exposure wavelength, 5x reduction and *NA*=0.6 for photolithography of all layers. We used a positive photoresist and antireflection coating in order to minimize standing waves caused by high reflectance of Nb layers.

From the photolithography standpoint, photolithography of JJs reduces to photolithography of posts or contact holes in semiconductor manufacturing. The important differences are that, first, a very high accuracy of the area definition is required as I_c is proportional to JJ area, and second, a broad range of JJ sizes needs to be printed in a manner preserving the proper relationship between their areas and, hence, I_cs.

We used a circular-shaped design for JJs, as it retains circular symmetry after diffraction and gives the minimum area for a given critical dimension (CD). The square shape used in [17]-[19] gives the maximum area but requires resolution enhancement techniques (RET) to correctly print corners rounded by diffraction effects, making the area control more difficult. The implemented JJs were circular-shaped polygons (manhattans) defined on a 5-nm grid (25-nm grid on 5x photomask). Hereafter we give all dimensions in the 1x wafer scale after the 5x reduction rather than in the photomask scale.

For the specified exposure parameters, the theoretical resolution limit for a line-space structure with pitch $p = w + s$ is $p_{\min} = (\lambda/NA)\cdot 1/(1+\sigma)$, where w, s, and σ are the linewidth, space, and exposure coherence factor, respectively [20]. This gives $p_{\min} = 413$ nm for coherent exposure ($\sigma = 0$) and 250 nm for partially coherent exposure with $\sigma = 0.65$. There is no theoretical resolution limit for single circles or squares. A practical limit exists, however, and is set by the photoresist properties, focus depth budget, and the desired linearity of the relationship between the printed size on the wafer, d_w, and JJ drawn size on the mask, d, which needs to be established.

Typical SEM images of photoresist features used for JJ definition are shown in Fig. 2. After photoresist exposure and development, the diameter of obtained features, i.e., the photoresist mask for JJ etching, was measured using a Hitachi CD-SEM by taking the mean of the measurements of the feature diameter at 49 points around the feature perimeter, as shown by the dotted white line in the right panel of Fig. 2. Thus measured dependence of the photoresist features on wafer, d_w, on the drawn size, d, of 1x exposure mask is shown in Fig. 3. It is close to the dependence we reported earlier for printing Nb posts in our stud-via technology [15]. Over a very wide range of JJ diameters, it was found that the dependence can be very well approximated by

$$d_w = (d^2 - d_c^2)^{\frac{1}{2}} + b \tag{1}$$

at $d > d_c$ and $d = 0$ otherwise, where d_c is the minimum printable size or photolithography cut-off and b is the process bias. The typical value of d_c we observed on a very large number of runs is 245 nm ± 20 nm, and the minimum value was ≈ 225 nm.

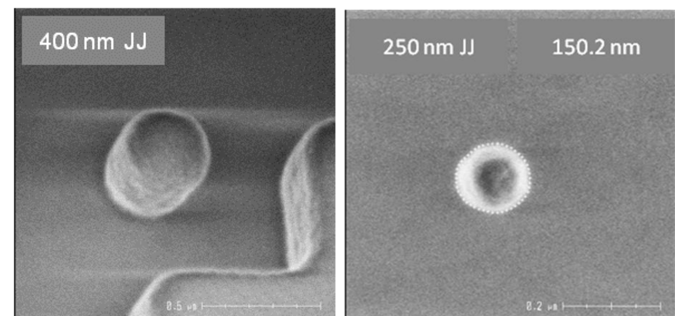

Fig. 2. SEM images of photoresist features. Left panel shows a tilted view of the photoresist JJ etch mask at $d = 400$ nm. Right panel shows the top view of the photoresist JJ etch mask at $d = 250$ nm, giving $d_w = 150$ nm; white dots around the perimeter show 49 points used for measuring the mean feature diameter, d_w.

The origin of the cut-off is as follows. The requirement to print a range of JJ sizes sets an exposure dose - dose to print -

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that gives the proper sizing of the desired features. Diffraction of light on the mask features creates a nonzero exposure of the photoresist in the "dark" region of the geometric shade. This exposure increases with the feature size decreasing. At a certain size, d_c, the exposure becomes so high that the photoresist is developed away.

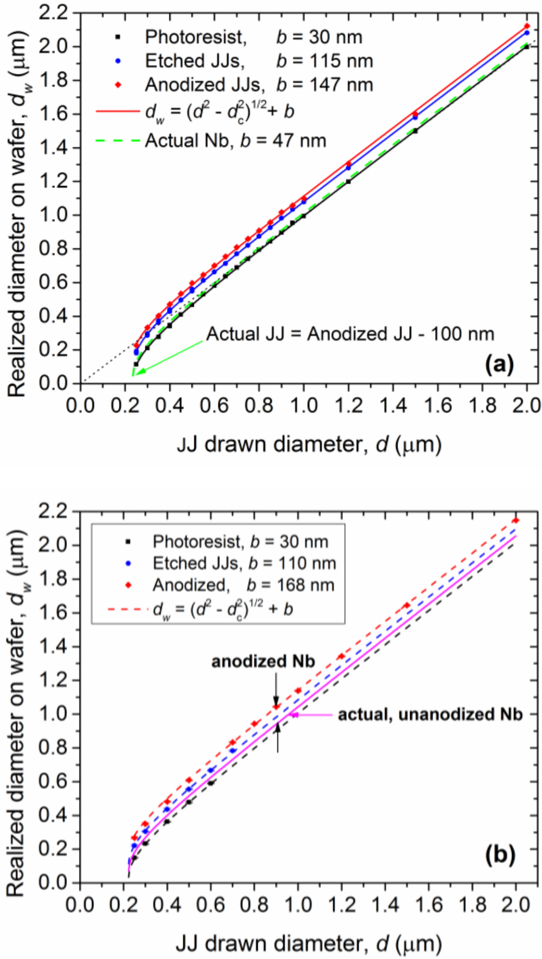

Fig. 3. The on-wafer diameter, d_w, of circular features formed during the steps of Josephson junction fabrication as a function of JJ drawn diameter on the photomask: (■) – photoresist etch mask, (●) - etched counter electrode of JJs, (♦) - anodized counter electrode of JJs. Lines show fits to (1), giving d_c = 235 nm and 223 nm, respectively, for the data in Fig. 3(a) and Fig. 3(b). The data in Fig. 3(a) and Fig. 3(b) were taken during two fabrication runs of the 8-metal layer process, about a year apart, and demonstrate the high stability and reproducibility of the fabrication process. The size bias increases from b = 30 nm for the photoresist etch mask to ~ 150 nm after anodization of JJs. However, the real diameter of the un-anodized Nb counter electrode, i.e., the actual JJ size is ≈ 100 nm less than the anodized JJ seen in the SEM. The desired, ideal, relation $d_w = d$ is shown by dotted line in Fig. 3(a).

In order to provide a mathematical description of the image size for comparison with the measurements, we use the standard theory of image formation in optical imaging systems based on Fraunhofer scalar diffraction theory and Fourier optics [21],[22]. In this theory, the image formed by an objective is a Fourier transform of the diffraction pattern of the optical mask filtered by the finite numeric aperture of the objective (exit pupil). For coherent illumination, the amplitude of light in the image plane on a wafer can be written as

$$E(x,y) = \iint_{-\infty}^{+\infty} \tilde{P}(f,g)\tilde{O}(f,g)e^{-i2\pi(fx+gy)}df dg, \quad (2)$$

where $\tilde{O}(f,g)$ is the mask spectrum, i.e., the Fourier transform of the mask pattern, $\tilde{P}(f,g)$ is the so-called pupil function describing the response of the projection system to space frequencies (f,g), and $\exp[i2\pi(fx+gy)]$ term represents the interference of light rays propagating in a direction θ given by $|\sin\theta| = \lambda\sqrt{f^2+g^2}$ [23].

For an opaque disk with diameter d on the photomask (a drawn JJ), the mask transmittance function is

$$O(x,y) = 1 - circ(2r/d)$$
$$O(x,y) = 0 \text{ if } 2r/d \le 1, \text{ and } O(x,y) = 1 \text{ if } 2r/d > 1 \quad (3)$$

where $r = \sqrt{x^2+y^2}$. The Fourier transform of $circ(r)$ function is a very well known Airy function [22], so the mask spectrum is

$$\tilde{O}(f,g) = \delta(f)\delta(g) - \frac{\pi d^2}{2}\frac{J_1(\pi d q)}{(\pi d q)}, \quad (4)$$

where $q = \sqrt{f^2+g^2}$, δ is Dirac delta-function, and $J_1(u)$ is a Bessel function of the first kind, first order.

For the circular-symmetric imaging system with coherent illumination, the pupil function is

$$\tilde{P}(f,g) = 1 \text{ if } \sqrt{f^2+g^2} \le NA/\lambda, \text{ and 0 otherwise} \quad (5)$$

I.e., the image is formed only by the light rays coming at angles with $|\sin\theta|$ lesser than the numeric aperture of the lens, and all higher space frequencies are filtered out. This sets the limits of integration in (2) from $-NA/\lambda$ to $+NA/\lambda$.

In general, (2) requires numerical integration. In order to get an analytical expression, we consider the case of very small mask diameters $d \ll \lambda/NA$ and use zero order expansion of the Airy function $J_1(u)/u = 1/2$. Then, the mask function in (4) becomes

$$\tilde{O}(f,g) \approx \delta(f)\delta(g) - \pi d^2/4, \quad (6)$$

and the integral in (2) can be evaluated [22] to get the field distribution in the image plane

$$E(\rho) \approx 1 - \frac{1}{4}\left(\frac{\pi d NA}{\lambda}\right)^2 \frac{2J_1\left(\frac{2\pi\rho NA}{\lambda}\right)}{2\pi\rho\left(\frac{NA}{\lambda}\right)}, \quad (7)$$

which has the circular symmetry of the photomask, and ρ is the distance from the center of this aerial image. The normalized intensity of light at any point is $I(\rho) = E(\rho)^2$.

To find the size of the image in photoresist, we apply the standard model of an infinitely thin, threshold resist [23], [24]. In this model, the photoresist is developed away at any point on the wafer that receives an exposure dose higher than the threshold dose corresponding to normalized light intensity I_{th} and remains on the wafer otherwise. The contour of the image is then given by points in the image plane satisfying the solution of the equation

$$E(x,y)^2 = I_{th}, \quad (8)$$

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which in our circular-symmetric case reduces to $E(\rho) = \sqrt{I_{th}}$. A solution of this equation exists only if the mask diameter (JJ drawn size) is larger than the minimum size, d_c, given by

$$d_c = \frac{2\lambda}{\pi NA}(1 - \sqrt{I_{th}})^{1/2}, \quad (9)$$

Otherwise, the light intensity at any point of the image is larger than I_{th} and the resist will be developed away. Indeed, at the center of the image where $2J_1(u)/u = 1$, the light intensity is $\left[1 - \left(\frac{\pi dNA}{2\lambda}\right)^2\right]^2$, so eq. (8) can only be satisfied if $d \geq d_c$ given by (9). A similar treatment for square posts can be found in [25], giving a factor of $2/\sqrt{\pi}$ smaller result for the minimum printable size of squares.

For mask diameters slightly above the d_c, the size of the image in photoresist can be found by expanding the Airy function in (7), $2J_1(u)/u = 1 - u^2/8$, and using (8) to obtain

$$d_w = \frac{2\sqrt{2}\lambda}{\pi dNA}(d^2 - d_c^2)^{1/2}, \quad (10)$$

with d_c given by (9). For $d - d_c \ll d_c$, (10) gives the same functional dependence as the empirical relation (1). Note, that according to (7) the light intensity grows as d^4 for $d << NA/\lambda$, so the cut-off at d_c is very sharp.

A value of I_{th} giving a good representation of the typical photoresists is $I_{th} = 0.3$ [23]–[25]. This gives $d_c = 177$ nm for our exposure conditions, a bit lower than the typical values of $d_c > 220$ nm observed in this work. The difference is due to the assumed purely coherent exposure, finite thickness of the photoresist, defocusing, and other photoresist effects.

Light intensity distributions following from (7) are shown in Fig. 4 for several mask diameters d below and above the minimum printable size d_c. A photoresist with lower I_{th},

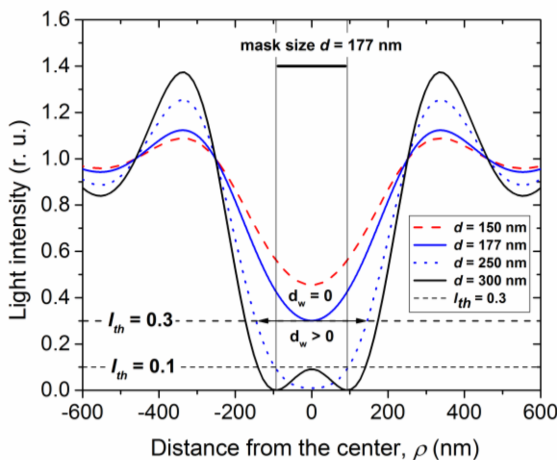

Fig. 4. Light intensity distribution in the image plane (aerial image of JJs) for several diameters of the opaque disc representing various drawn JJs on the photomask. The distance is counted from the center of the aerial image. If $d \leq d_c$ (e.g., two upper curves), the light intensity everywhere is larger than the photoresist exposure threshold I_{th} so that there is no image in photoresist , i.e., all the resist is developed away, and hence there is no photoresist mask for JJ etching. The diameter of the resultant photoresist image as well as the cut-off diameter d_c depends on the photoresist threshold intensity.

e.g., $I_{th} = 0.1$ also shown in Fig. 4, gives a larger value of d_c and a smaller photoresist image.

For a wider range of sizes, approximation (6) for the mask function (4) is not sufficient and (2) needs to be integrated numerically. Numeric results obtained using photolithography simulator PROLITH 9.0 [26] are shown in Fig. 5 both for coherent and partially coherent illumination. Not surprisingly, near the cut-off size the numerical results agree nearly perfectly with our analytical result (10) for coherent illumination. For the partially coherent illumination, σ = 0.65, the cut-off diameter increases to 192 nm, becoming closer to the actual d_c observed.

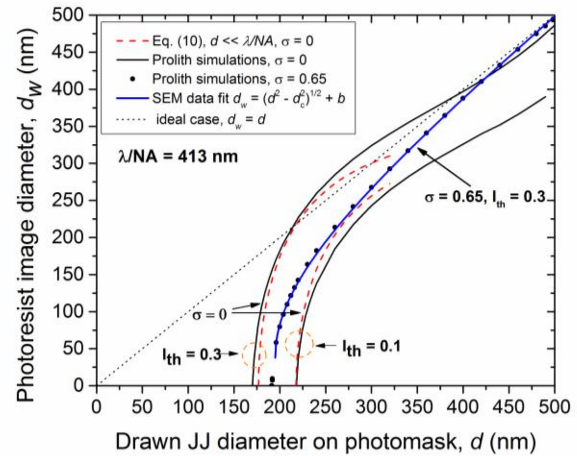

Fig. 5. Results of the analytic and numeric calculations of the image diameter in the threshold photoresist as a function of the drawn diameter on the photomask for different exposure parameters and photoresist threshold intensity, I_{th}. Dash lines are the analytical result (10) for coherent illumination, σ = 0, and $d << NA/\lambda$ at two different threshold intensities; solid lines are numeric results obtained using PROLITH for the same parameters. PROLITH simulations at σ = 0.65 are shown by dots (●) along with the fit to (1) shown by the solid line; they are virtually indistinguishable.

Also, we have found that the results of PROLITH simulations of the photoresist image diameter at σ = 0.65 used in this work can be perfectly fitted by the empirical function (1) that was found to be the best fit to SEM data on the photoresist feature diameter as a function of the drawn diameter, see Fig. 5 and Fig. 3. This gives yet another justification for using (1) in further discussions of JJ properties.

C. Etching and anodization of Josephson junctions

After forming the photoresist mask described above, the JJ counter electrode was etched using a high density plasma etcher and anodized after that to prevent degradation of the exposed AlO_x barrier [27]-[29]. The sizes of the etched JJs were measured before and after the anodization, and are shown in Fig. 3 along with the size of the photoresist features used as an etch mask. For statistics, multiple JJs of the same nominal size were measured on the same test chip at different locations on the wafer.

It can be seen in Fig. 3 that etching adds a constant bias, Δb to the size of JJs in comparison with the size of the photoresist etch mask. Similarly, anodization adds yet another bias component, increasing the JJ diameter by about 50 nm. This increase is caused by the Nb_2O_5 layer grown on the sidewalls of JJs during the anodization. Its thickness was measured using cross-section TEM, and was found to be ≈ 50 nm, see Fig. 6. During the anodization, about 0.9 nm/V of Nb is

consumed and converted in about 2.5 nm/V of niobium oxide. Therefore, the actual diameter of the niobium counter electrode of JJs, i.e., the final JJ size as seen in SEM, is given by $d_w = d_{anod} - 100$ nm , where d_{anod} is the JJ size measured by the SEM after the anodization. This dependence is shown in Fig. 3(a) by a dash line and in Fig. 3(b) by a solid line, and corresponds to the final bias b in the range from 50 nm to 70 nm in (1). Note that etching and anodization do not affect the d_c that is completely determined by the photolithography process.

D. *Planarization and further processing of JJs*

After patterning the base electrode of the JJs using the described photolithography and high density plasma etching, the junction mesa was planarized by depositing a thick layer of SiO_2 and polishing it down to the level of the JJ counter electrode by using CMP. This forms a flat interlayer dielectric to deposit and pattern a wiring layer for contacting the tops of the JJs. The SiO_2 thickness was measured using an ellipsometer.

Further processing steps involve depositing and patterning the layer of resistors, adding an interlayer dielectric between the resistors and the next wiring layer, opening contacts to the buried base electrode of the JJs, and depositing and patterning the wiring layer contacting the JJs and the resistors; see the final process cross-section in Fig. 1. A cross-section TEM of a fully processed 500-nm JJ is shown in Fig. 6.

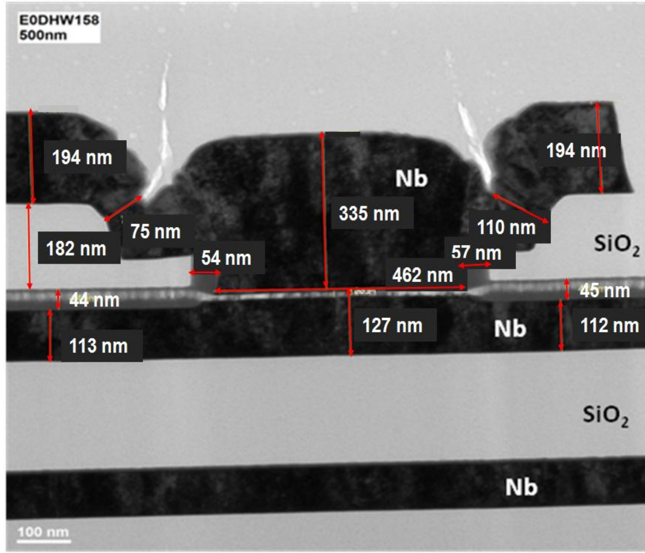

Fig. 6. A cross-section TEM image of fully processed Josephson junction with drawn diameter $d = 500$ nm. Lighter region along JJ sidewalls and base electrode is anodized niobium.

E. *Electrical characterization of Josephson junctions*

The electric resistance of individual JJs on the processed wafers was measured by semi-automated wafer probers, using 4-probe measurements of JJs in a cross-bridge Kelvin geometry (CBKR). JJ design with a minimum surround of the JJ by the counter electrode and the top wiring layer was used to minimize the parasitic contribution of the surround to JJ tunnel barrier resistance. For JJ sizes used in this work, this parasitic contribution is negligible, but it may become noticeable at $d > 5$ µm or even less for higher-J_c junctions. For testing JJ repeatability, a number of nominally identical JJs was measured, typically 36, 44 or 60 JJs of each size on each of 9 dies spread over the wafer, giving from 324 to 540 JJs of a given size per wafer for statistics, over 4000 JJs per wafer. JJ conductance vs. size dependences were used to infer the tunnel barrier specific conductance and estimate the J_c from room-T measurements, using 160 JJs with drawn sizes from 200 nm to 15 µm at each location. The same JJs were later measured at LHe temperature after dicing the wafers and wire bonding the chips. Current-voltage (I-V) characteristics of individual JJs and 1000-JJ series arrays were measured in a magnetically shielded cryoprobe allowing for automated testing of up to twelve 5 mm by 5 mm chips at LHe temperature.

III. Experimental Results and Discussion

A. *10 kA/cm² process*

Fig. 7 shows the relation between JJ resistance, R_{300}, measured at room temperature and JJ normal state resistance, R_N, at 4.2 K measured from I-V characteristics. The relation is perfectly linear $R_{300} = kR_N$ with $k = 0.905 \pm 0.010$. Value of k lesser than 1 is consistent with the tunnel nature of the barrier and indicates negligible contribution of Nb resistance in contact with the barrier [30]-[32]. I-V characteristics also show high junction quality as indicated by high subgap resistance $R_{sg}/R_N > 10$ and high gap voltage $V_g = 2.75$ mV. R_N is related to I_c of a junction by the Ambegaokar-Baratoff relation $I_cR_N = V_{AB}(T)$ [33]. At 4.2 K, $I_cR_N = 1.75$ mV for our junctions.

The linear relation between R_{300} and R_N and respective conductances $G_{300} = 1/R_{300}$ and $G_N = 1/R_N$ allows us to use automated measurements of R_{300} on a wafer prober for fast screening of a very large number of JJs on 200-mm wafers instead of time consuming measurements of JJs at 4.2 K. This enables assessing JJ uniformity and reproducibility on a wafer scale as well as a meaningful prediction of JJ critical currents and trilayer's J_c based on room-T measurements and the I_cR_N.

Both JJ conductance G_{300} and I_c are proportional to JJ area

$$G_{300} = G_0 \frac{\pi}{4}(d_w - d_0)^2 \text{ and } I_c = J_c \frac{\pi}{4}(d_w - d_1)^2, \quad (11)$$

where parameters d_0 and d_1 account for a possible deviation of the diameter of, respectively, the conducting and superconducting parts of the junction from its physical diameter d_w measured by a SEM. Since d_w is described by (1), parameters d_0 and d_1 simply modify the size bias b. Parameters G_0 and J_c characterizing the tunnel barrier can be found by fitting $\sqrt{G_{300}}$ and $\sqrt{I_c}$ to (11) with d_w given by (1) and G_0, J_c, and b as fitting parameters. An example of such a fitting is shown in Fig. 8 for 9 locations on a 200-mm wafer.

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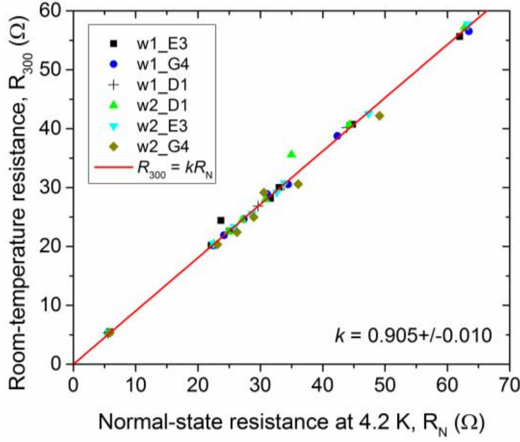


Fig. 7. The room temperature resistance of JJs in CBKR configuration *vs* their normal state tunnel resistance from *I-V* characteristics at 4.2 K for multiple junctions and different locations on two wafers of 10 kA/cm^2 process.

The typical histograms of the conductance of nominally identical junctions at room-*T* are shown in Fig. 9 for all JJs tested on the wafer. The distributions can be fitted well by a Gaussian distribution with standard deviation, σ_G, depending on the junction size. The data in Fig. 9 represent cumulative distributions of JJs located on 9 chips over 200-nm wafers, so the σ_G values shown represent the wafer-level spreads of JJ conductance. Local, on-chip spreads which are more important for SFQ circuits are lower as will be discussed below. The wafer spread is a convolution of several factors: local variations of JJ area and tunnel barrier transparency within a 5x5 mm^2 chip, global variation of the mean area caused by focus variations from one exposure field to another, and global variation of the trilayer tunnel barrier specific conductance on the wafer scale.

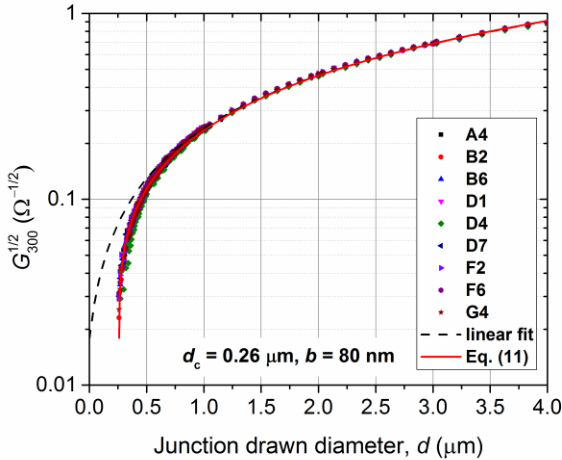


Fig. 8. The typical data showing the square root of JJ conductance at room temperature, $G_{300}^{1/2}$, as a function of the drawn diameter of JJs on the photomask. The data were taken on 18 chips at 9 different locations on the typical wafer from 10 kA/cm^2 process run. The locations, labeled as A4, B2, etc., are shown on 7x7 grid (A,B,…,G;1,2,…,7) corresponding to the exposure grid of the wafer. 160 junctions with drawn diameters from 0.20 μm to 15 μm were measured at each location. The data for 1296 JJs are shown for the range of sizes in Fig. 8. Solid line is the fit to (11) with d_w given by (1). Dash line (linear fit) is a fit to $G_{300} = G_0(\pi/4)(d - d_0)^2$, where d_0 is the so-called "missing diameter," giving d_0 = 80 nm. The full fit to (11) with (1) gives G_0 = 64 mS, d_c = 0.26 μm, and b = 80 nm.

Since JJ conductance is proportional to I_c, we expect that σ_G characterizes the distribution of the critical current of these JJs as well. To verify this we measured the *I-V* characteristics of series arrays of 1000 JJs shown in Fig. 10 and determined the distribution of switching currents of the JJs in the arrays shown in Fig. 11. At sufficiently large I_c, the switching current is very close to the actual I_c, whereas for small JJs with small I_cs the switching current can be significantly affected by thermal and external noise. We have found a very good agreement between the on-chip variations of JJ conductance at room-*T*, characterized by standard deviation σ_G, and the on-chip variations of the critical current of JJs characterized by standard deviation σ_I. This allows us to use in the following discussions the results on the conductance distribution, implying that the same results apply to the distribution of JJ critical currents both on-chip and on-wafer. We use hereafter the relative standard deviations expressed as a percent of the mean value.

The conductance distribution standard deviation depends on the size of the junctions. This dependence is shown in Fig. 12 for the on-chip and wafer-averaged conductance standard deviation. If we assume that all variations of JJ conductance come from the variations of the JJ area on the wafer and the barrier is absolutely uniform, we can develop a simple model to describe the data. The JJ actual area is $A = (\pi/4)\, d_w^2$, and the area fluctuations are twice the fluctuations of JJ diameter. If we assume that the area fluctuations on the wafer come from fluctuations of the JJ mask area on the photomask, the so-called mask errors, we obtain using (1) that

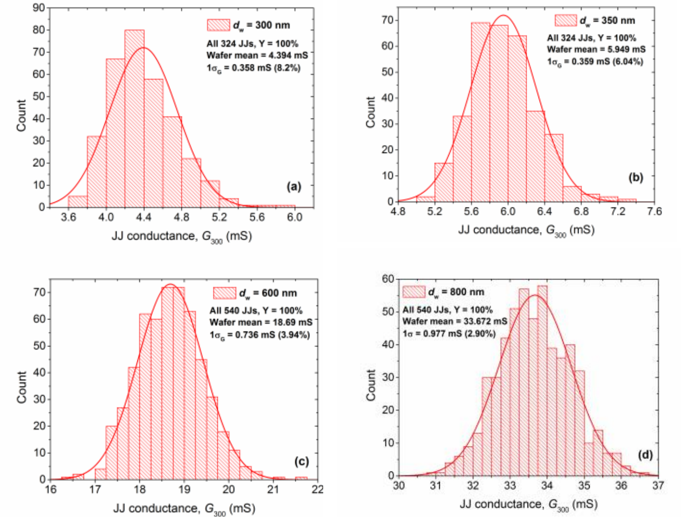


Fig. 9. The cumulative distributions of JJ conductance at room-*T* for several realized sizes of JJs on wafer, d_w: (a) – 300 nm, (b) – 350 nm, (c) – 600 nm, (d) – 800 nm. The distributions represent 324 JJs measured at 9 locations (36 JJs pre chip) for (a) and (b), and 540 JJs from the same locations (60 JJs per chip) for (c) and (d). JJ conductance at room-T is proportional to the normal-state conductance at 4.2 K and to I_c of JJs. Therefore, the standard deviations shown here represent the standard deviation of the I_c of JJs on the wafer scale. JJ yield, *Y*, was 100%.

$$\frac{\partial A}{A} = \frac{2(\delta d_w)}{d_w} = \frac{2d(\delta d)}{(d^2 - d_c^2)^{1/2}[(d^2 - d_c^2)^{\frac{1}{2}} + b]}, \qquad (12)$$

where δd is the typical variation of the JJ diameter on the photomask introduced by the photomask fabrication process. Since the address size used to e-beam-write the junction photomask is 5 nm, it is reasonable to assume δd to be about that and treat it as a fitting parameter in fitting (12) to the data in Fig. 12.

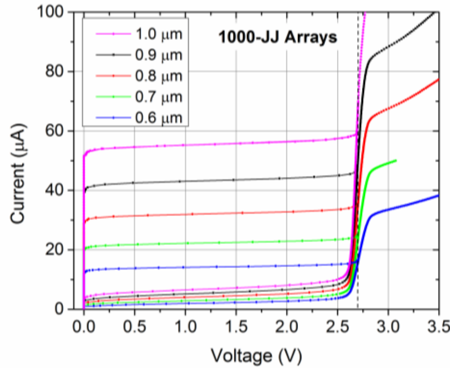


Fig. 10. The *I-V* characteristics of 1000-JJ series arrays of Josephson junctions with drawn diameters from 1.0 μm to 0.6 μm (from top to bottom). Up to 40k JJs per chip were measured using these arrays. The *I-V* curves were used to build the switching distributions shown in Fig. 11 and characterizing the on-chip distributions of the critical current of JJs, I_c.

In order to check this model, we measured the on-chip variations of the JJ diameters at different steps of JJ fabrication, using a Hitachi CD-SEM as was described above. Unfortunately, the accuracy of the SEM measurements suffers at JJ sizes larger than about 1 μm because a relatively low magnification needs to be used to image the JJ and nm-scale variations become undetectable, whereas 200k magnification was used for the smallest JJ sizes.

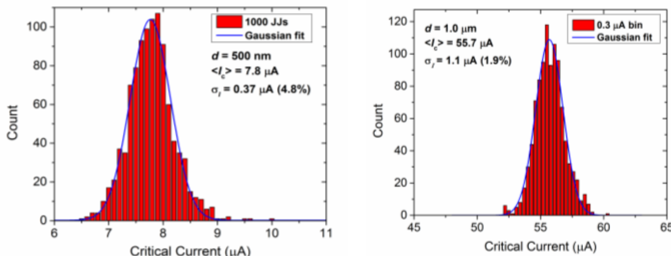
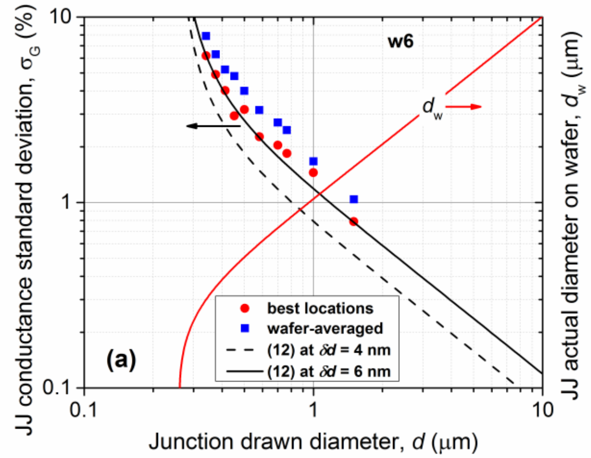


Fig. 11. The typical switching current distributions obtained from the *I-V* characteristics of 1000-JJ series arrays shown in Fig. 10 and similar. For the critical currents much larger than the thermal noise, these distributions characterize the I_c distributions.

The measured relative standard deviation of the diameter, $\sigma_d/<d>$, where $<d>$ is the mean diameter, was converted into the relative standard deviation of the area $\sigma_A/<A>$. The results shown in Fig. 13 are for a typical wafer from the 8M process run.



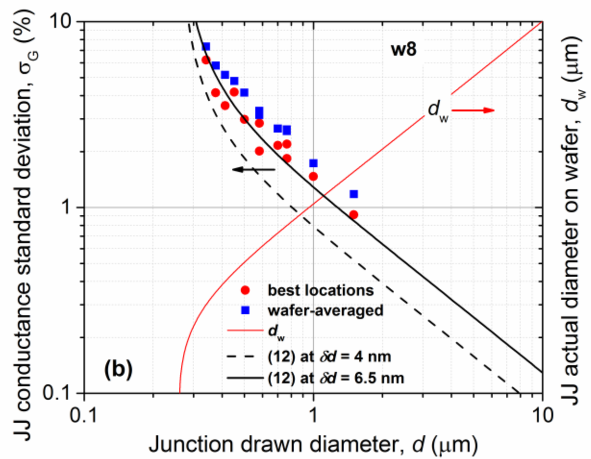


Fig. 12. The relative standard deviation of JJ conductance, in percent of the mean, as the function of JJ drawn diameter on the photomask for the two typical wafers. The actual diameter of the JJs on the wafers is shown on the right axis. The data were obtained by measuring 9 chips per wafer and the minimum of 36 to 60 JJs of the same size per chip. The wafer-averaged data are shown by squares, whereas the data from the best locations on the wafer are shown as dots. The expected conductance variations following from the model of JJ area variations (12) at $\delta d = 4$ nm as measured in SEM, see Fig. 13, is shown by the dash curve. The best fit to the best data are shown by the solid curves and give $\delta d = 6$ nm and $\delta d = 6.5$ nm for w6 (a) and wafer 8 (b), respectively.

It can be seen that the measured area variation can be explained by the model (12) at $\delta d = 4$ nm. This value is very close to the grid size of 5 nm used to define the JJ polygons (manhattans) approximating the circular JJs and to the address size used for e-beam writing of the photomask patterns, and thus is reasonable.

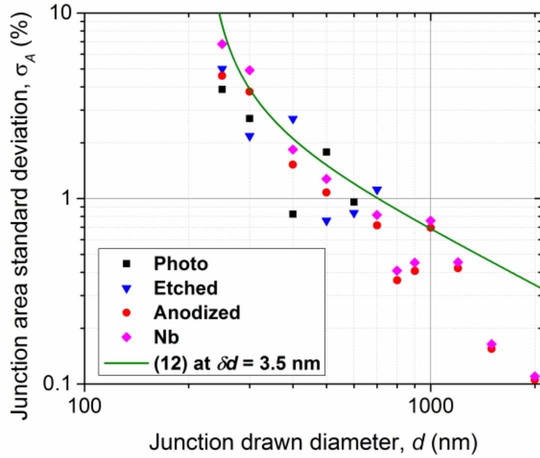


Fig. 13. The relative standard deviation of JJ feature area variations at different steps of JJs fabrication: photoresist mask, etched counter electrode, anodized counter electrode, and un-anodized part of niobium counter electrode. The diameters of multiple JJs were measured by CD-SEM to calculate the standard deviation. The accuracy of the measurements decreases at large sizes because progressively lower magnification needs to be used to image the features. Equation (12) at δd = 3.5 nm is shown by a solid curve.

The best fit to the JJ conductance variations gives a 50% larger $\delta d \approx 6$ nm, see the solid lines in Fig. 12. Although the range of mask errors is small, and likely independent of the JJ mask size, the strong enhancement of the area fluctuations observed near the minimum printable size is due to the strongly nonlinear relation between the drawn and realized sizes (1), as was explained in Sec. 2B. This enhancement makes printing of sizes near the cut-off size d_c unpractical if a tight area control is required.

The range of sizes of JJs that can be implemented in VLSI SFQ circuits with J_c = 10 kA/cm^2 is from 700 nm to 2000 nm, giving the I_c range from 38 μA to 314 μA because smaller sizes would give unacceptable bit error rates. For this range, the on-chip spread of I_cs is less than 2% as follows from Fig. 12 and the on-wafer spread is less than 3% as shown in Fig. 9. We believe that these spreads are sufficiently low for yielding SFQ circuits with 10^6 JJs and beyond, and meet the requirements formulated in [1] and [46].

B. 20 kA/cm^2 process

Further increasing the speed of SFQ circuits may require higher J_c than 10 kA/cm^2, the present target of our 8M and 10M processes, and respectively smaller JJ sizes. To evaluate the expected parameter spreads we made a process run targeting J_c of 20 kA/cm^2 and 50 kA/cm^2. We used exactly the same set of photomasks and the same processing as was used for 10 kA/cm^2 process presented above.

The *I-V* characteristics of individual JJs and 1000-JJ arrays were measured at 4.2 K and are shown in Fig. 14. The switching distributions were extracted from the *I-V*s, and the room-*T* measurements on multiple individual junctions were done on the same set of JJs as was used in Sec. 3A.

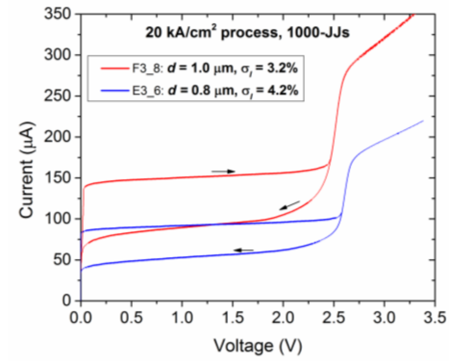


Fig. 14. The *I-V* characteristics of 1000-JJ arrays of Josephson junctions with drawn sizes 1.0 μm and 0.8 μm, from top to bottom. The exact value of J_c on this wafer was 23.8 kA/cm^2 determined from the scaling of I_cs in the range of drawn sizes from 0.6 μm to 2.0 μm. The specific normal state resistance was found to be R_{N0} = 7.57 Ω μm^2 and J_cR_{N0} = 1.80 mV.

C. 50 kA/cm^2 process

The same fabrication and electrical measurements were done for a 50 kA/cm^2 process run. The typical *I-V* curves for single JJs are shown in Fig. 15.

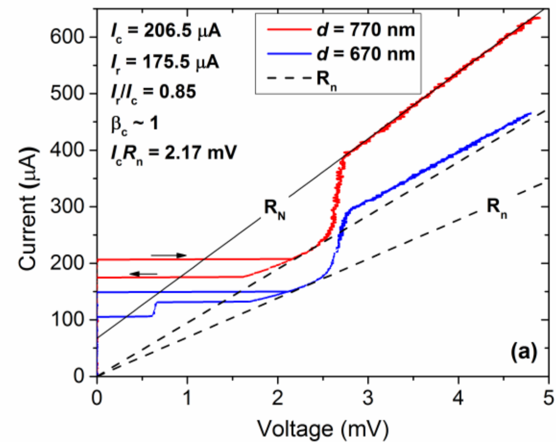


Fig. 15. The *I-V* characteristics of junctions with J_c = 45 kA/cm^2 and drawn diameters 770 nm and 670 nm, respectively, for the top and bottom curves. At this J_c, the junctions are self-shunted with damping parameter β_c close to 1 as indicated by the return current I_r = 0.85I_c. Dash lines show the subgap resistance, R_n damping the JJs at these voltages. The solid line shows the normal state resistance above the gap voltage, R_N for d = 770 nm. A current step on the return branch at V ~ 0.65 mV is a geometric resonance of Josephson oscillations in the JJ leads. The normal-state specific resistance, R_{N0}, at this J_c is 4.45 Ω μm^2 and J_cR_{N0} = 2.01 mV.

An "excess" current can be seen in *I-V* curves defined as the zero voltage intercept of the solid line in Fig. 15(a). It is about 0.33I_c. This "excess" current is the result of nonzero time average of Josephson oscillations above the gap voltage of the current-biased JJs [34], [35].

The advantage of the 50 kA/cm^2 process is that JJs at this current density become almost nonhysteretic as can be seen in Fig. 15. The return current is about 85% of the critical current, indicating self-shunting with the damping parameter $1 < \beta_c < 2$. Therefore, the junctions can be used in SFQ circuits without external shunts. Their damping is provided by the internal subgap resistance, R_n, and the resultant I_cR_n product is about 2 mV, a factor of 2 higher figure than for the externally

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shunted JJs in the 10 kA/cm^2 process at the critical damping $\beta_c = 1$. This should enable much faster and denser circuits at our future technology nodes.

The JJ conductance spreads and I_c spreads for JJs with 24 kA/cm^2 and 45 kA/cm^2 are shown in Fig. 16. They are somewhat larger than the typical spreads shown in Sec. 3A for the 10 kA/cm^2 process, but follow the same trends.

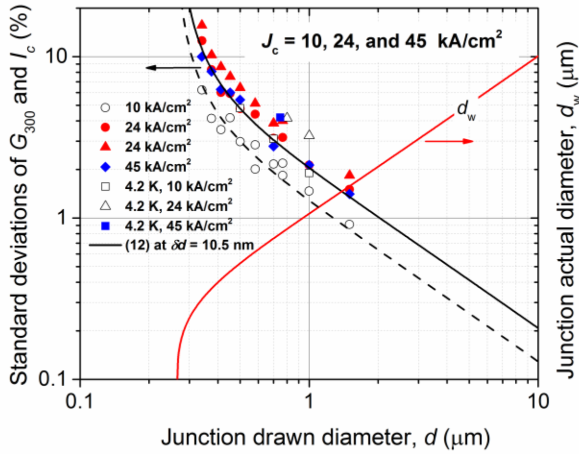

Fig. 16. The standard deviation of JJ conductance at room-T and of the critical current at 4.2 K for single junctions and 1000-JJ arrays fabricated with critical current densities J_c = 10 kA/cm2, 24 kA/cm2, and 45 kA/cm2. The data from top to bottom correspond to the best locations on wafers at J_c=10 kA/cm^2 and 24 kA/cm^2, wafer-averaged data for 24 kA/cm^2, best locations at 45 kA/cm^2 and 4.2 K data after that. The solid line shows the expected standard deviations from model (12) at δd = 10.5 nm and fits the data for high-J_c junctions very well. The fitted δd is 75% higher than that for the 10 kA/cm^2 process shown by dash line, see also Fig. 12.

The spreads can be fitted by (12) with δd = 10.5 nm. Since we used exactly the same photomasks and fabrication process, this difference may indicate the existence of another factor contributing to the spreads of the effective, electric, area of JJs in addition to the geometric fluctuations described by (12) and scaling with JJ diameter in the same manner. It may be a result of some contamination near the sidewalls around the perimeter of the junctions, affecting the electrical diameter or variations of the barrier transparency. The nature of the higher variability of high-J_c JJs has not been established yet. We believe that these initial spreads for 20 kA/cm^2 and 50 kA/cm^2 processes can be reduced to the same level as those for the 10 kA/cm^2 one by making more fabrication runs and practicing the processes to the same level of maturity.

D. Discussion

In the prior discussion we left aside a few other possible contributions to JJ variability additional to the enhanced mask errors described by (12). The first one is the variation of the cut-off size d_c caused by variations of focus, local photoresist chemistry, etc. This contribution is also enhanced by the nonlinear projection near the cut-off. Indeed, differentiating (1) with respect to d_c we get a similarly diverging expression

$$\frac{|\partial A|}{A} = \frac{2d_c(\delta d_c)}{(d^2 - d_c^2)^{1/2}[(d^2 - d_c^2)^{\frac{1}{2}} + b]}, \tag{13}$$

where δd_c is the variation of the cut-off size. The contribution of (13) to on-chip variability should be much smaller than (12) due to the much smaller numerator because δd_c within the die should be very small. But it may contribute to on-wafer variation of the mean value due to possible focus variation between the stepped exposure fields, which could produce δd_c in the range of ±10 nm across the wafer.

The second is variations of electric biases d_0 and d_1 in (11), which is equivalent to variations of b in (1)

$$\frac{\partial A}{A} = \frac{2(\delta b)}{[(d^2 - d_c^2)^{\frac{1}{2}} + b]} \tag{14}$$

These δb variations could be caused by some contamination of Nb around JJ sidewalls, e.g., hydrogen absorption during etching [36]-[39], that affects superconducting properties of Nb near the Nb/Nb_2O_5 interface. The size of this potential variability and whether it exists are not known. The total area variance is the sum of all variances described by (12)-(14).

As we have shown above, the on-chip and on-wafer spreads we have achieved in our 10 kA/cm^2 processes with 4 and 8 metal layers are at the level that should enable fabrication of VLSI superconducting circuits with 10^6 JJs and beyond. The spreads reported here are significantly lower than those reported for the best industrial [41]-[45], and advanced research processes [17],[19],[40]. However, further lowering of JJ spreads is always desirable especially for higher-J_c processes with smaller JJs. The results obtained in this work show three clear approaches to this.

The first one is the reduction of “mask errors” – fluctuations of JJ area on the photomask – by implementing the smaller grid size for JJ design and smaller address size for photomask e-beam writing. We are planning to utilize photomasks with 1 nm design grid and address in the future process runs. This should also allow us to verify our model (12).

The second one is the minimization of the mask error enhancement caused by the proximity of the sizes to print to the photolithography cut-off size d_c at which the area fluctuations diverge. This can be done by significantly reducing d_c by transitioning to 193-nm photolithography. Indeed, for our 193-nm exposure tool with NA = 0.75, using (9) we can estimate the cut-off size for coherent illumination to be 110 nm for the threshold resist and about 130 nm for the real one, which is a factor of 1.6 to 2 less than for the 248-nm tool used in this work. Then, the ratio of the minimum JJ size we need to print d_{min} ~ 500 nm for, say, 50 kA/cm^2 process to the cut-off size will increase from the present d_{min}/d_c ~ 2 to d_{min}/d_c ~ 4, moving the region on nonlinear projection - the nonlinear part of $d_w(d)$ dependence and the associated mask error enhancement - farther away from the range of the sizes of interest.

The third direction is the identification and elimination of the extra JJ variability causing about 50% increase of the conductance spreads with respect to the geometric area fluctuations described by (12), see Fig. 12 and Fig. 16. We leave the implementation of these approaches for future work.

IV. Conclusion

We have developed a fabrication process for fully planarized Nb/Al-AlO_x/Nb Josephson junctions on a 200-mm-wafer tool set of a CMOS foundry with 248-nm photolithography. We have measured the on-chip and on-wafer spreads of the junction conductance and critical current for junction sizes, d_w, from 200 nm to 1.5 µm in diameter and critical current densities up to 45 kA/cm^2. We have worked out the relationship between the drawn junction size, the size realized on the wafer, and the minimum printable size, d_c, for circular-shaped junctions. We have shown that a model accounting for the enhancement of mask errors near the minimum printable size accurately describes the variations of JJ parameters as a function of the drawn size. For the range of JJ sizes intended for use in SFQ circuits, we have achieved levels of JJ repeatability and yield that should allow us to get into very large scale integration of superconducting circuits with 10^6 JJs and beyond.

Acknowledgment

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