Power Hardware-in-the-Loop Testing of a YBCO Coated Conductor Fault Current Limiting Module

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Abstract— **In recent years, good progress has been made in improving the quality and quantity afforded by the manufacturing process for YBCO coated conductors. As a result, several programs have started to develop electrical power applications like motors, transformers, and fault current limiters (SCFCL) with these conductors. High voltage resistive type SCFCLs may typically be assembled from modules connected in series and parallel to accommodate the required voltage and current levels. The limited length of such a SCFCL module simplifies the configuration, manufacturing, and maintenance. It also allows testing of these modules under laboratory conditions at reduced power levels. In order to test SCFCL modules under conditions they will experience in high voltage electrical networks, advanced test methods such as power hardware-in-the-loop (PHIL) can offer significant advantages. This method allows studying conditions such as voltage stability and severe system perturbations with the actual SCFCL module in the loop. Hence, the quench and recovery behaviour of the SCFCL module can be investigated under conditions characteristic of real electrical power networks without elaborate experimental setups. This paper presents results from PHIL experiments with a SCFCL module consisting of an approx. 10 m coated conductor.**

Index Terms— **Superconducting fault current limiter, Power-Hardware-in-the-Loop, Test method,**

I. INTRODUCTION

THE availability of long lengths of coated conductors with high critical currents (I_c) and good homogeneity characteristics have made them applicable for several prototypes and first demonstrators of superconducting fault current limiters (SCFCLs) at medium voltage levels in recent years [1], [2].

The proper design of a fault current limiter requires the specification of a number of parameters, including rated current, limited current magnitude, number of limited half

cycles, voltage levels, and recovery time. Additionally, careful consideration must be made for placement of the device within the power grid, as well as for the impact of the device on protection systems. The internal layout of normal conducting layers of a coated conductor as well as the external wiring with shunt impedances are necessary to investigate in order to adjust the behaviour of a fault current limiter to obtain the desired behaviour [3], [4].

Furthermore, to cope with high operating voltages and currents in the medium and high voltage power grids SCFCLs tend to feature a matrix arrangement of individual modules connected in series and parallel. Such a design introduces a large number of additional degrees of freedom into the design process.

Testing of such modules under a large number of different circuit and operating conditions is vital for rigorous validation of the respective simulation models. Traditional test setups for SCFCL module testing consist of a voltage source (short circuit generator or grid connection) a current limiting impedance to adjust the prospective fault current, and a switch to make and break the current. In addition, a load impedance maybe used to establish continuous current flow. Changing the characteristics of such a setup to achieve different X/R ratios of the grid impedance typically requires a significant amount of time and labour. Furthermore, introducing external shunt coils of different values in parallel to the SCFCL module often requires new prototypes to be built and introduced to the test setup.

An alternative test method is to make use of Power-Hardware-in-the-Loop (PHIL) simulation. PHIL extends the common procedure of Hardware-in-the-Loop (HIL) to electrical power equipment [5]. This paper presents the results of testing a superconducting fault current limiting module under different test conditions using a PHIL test assembly.

To the authors' knowledge, this is the first such application of PHIL simulation for testing a superconducting fault current limiting module with instantaneous power above 1 MW.

II. EXPERIMENTAL SETUP

A. Fault current limiting module

The device under test was a superconducting fault current

limiting module with an approx. 10 m long coated conductor as the limiting element (see Fig. 1). The 12 mm wide coated conductor was stabilized by a 1.5 μm thick silver cap layer and a 96 μm thick substrate of Hastelloy®. The basic design of the module consisted of a single-layer coated conductor wound into spiral coil as depicted in Fig. 1.

The SCFCL module was neither built as an applicable prototype in power grids nor optimized in terms of magnetic fields and recovery after an over current. It was designed to investigate the quench behavior of a strongly inhomogeneous coated conductor due to the magnetic field. Therefore, the windings of the module are expanded to enable voltage measurements of 1 m sections along the tape.

Fig. 1 shows the SCFCL module before the experiments. The copper current leads are visible in the center and at the upper left corner of the module. The voltages were measured on the silver cap layer with clamped voltage taps. The voltage measurement system was connected to the voltage tabs with a specially isolated D-Sub connector in the center of the module. Not shown in Fig. 1 are additional spacers between the windings for the avoidance of deformation due to magnetic forces. The single windings were moreover isolated with a parallel wound polyimide foil (Kapton® tape) in case of deformation.
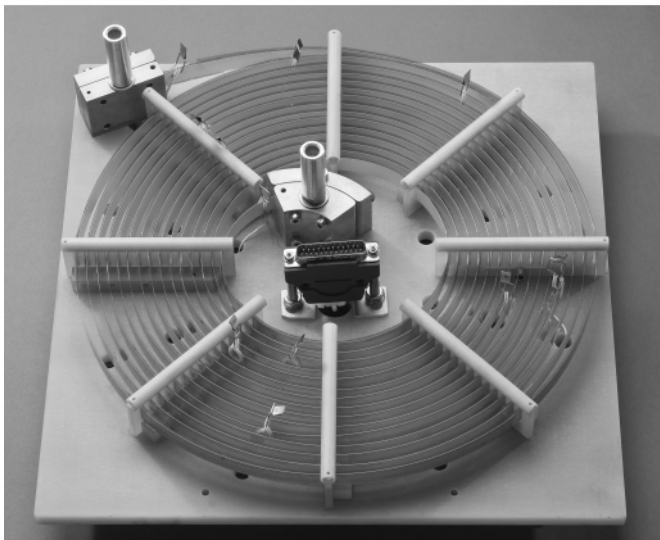

Fig. 1. Superconducting fault current limiting module made of a single spirally wounded, approx. 10m long coated conductor.

To examine the coated conductor for damage the critical current was measured after each fault current test. Fig. 2 shows the inhomogeneous distribution of I_c of the coated conductor due to the inhomogeneous magnetic field along the radial axis of the winding. Thus, the sectional I_c increases from the inner sections with the higher magnetic field to the outer sections with lower magnetic field as expected. Consequently, I_c could not be directly determined neither along the total conductor length of 10 m nor along a single 1m section using the 1 μV/cm criterion.

To avoid damage to the coated conductor, the current was stepwise increased till the measured total voltage along the

10 m tape was above 60 μV. With these data, I_c of the module was calculated with the known power law to 236 A. Based on this I_c, the nominal current (I_n) was determined to be $I_n=I_c/\sqrt{2}\cdot0.85\approx140$ A. The factor of 0.85 is arbitrarily chosen to allow for a safety margin. According to the I_c measurements the inner sections of the coil quenched first by applying a fault.
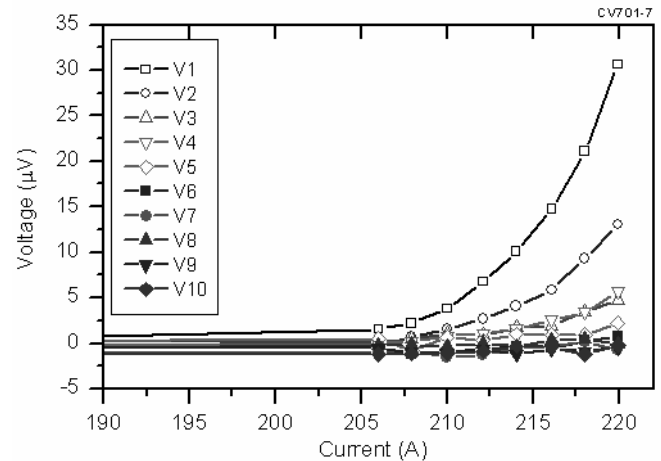

Fig. 2. Exemplary critical current measurement along each 1m section of the module. The sectional voltages start with the inner section (V1) to the outer section (V10). The inhomogeneity of I_c is due to the different magnetic field in each section.

While the superconductor showed no damage due to the fault current experiments defects appeared close to the current leads at the ends of the tape over the course of subsequent warm-up-cool-down cycles. In order to avoid burnout those defected sections were removed. Hence, between experiments the total active length of the module was gradually reduced from 10 m to 9.91m or 0.9% of the original length on both ends of the coated conductor. Thus the resistance of the module decreases by 0.9%. The influence of this 10%small reduction in length and resistance respectively was insignificant to the results.

B. PHIL Simulation setup

A very simple single phase representation of a utility system, modeled by a 50 Hz voltage source (V_{source}) with series impedance (Z_{source}) supplying a resistive load (R_{Load}), is simulated on a commercial real time digital simulator (RTDS) [6]. The RTDS simulator is capable of simulating relatively large electrical power systems in real time with time step sizes on the order of 50 μs. For the simple system described herein, a time step size of 25 μs was employed. The simulator is interfaced to a 2.5 MW/4.16 kV variable voltage source converter used to reproduce arbitrary voltage waveforms from the simulation with a maximum current of approx. 750 A.

RTDS has been used for testing superconducting cables in the recent years. However, no feedback signal from the hardware back into the simulation was used in the setup reported in [7]. In contrast, the PHIL setup presented here feeds the voltage measured across the SCFCL element back into the simulation. Furthermore, current feedback control was used to improve tracking of the current requested by the

simulated system. A schematic diagram of the PHIL setup and the corresponding control system is shown in Fig. 3.
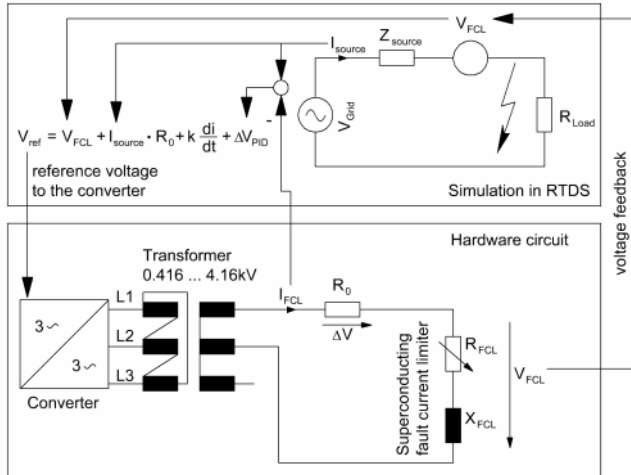

Fig. 3. Illustration of the conceptual PHIL setup.

The reference voltage for the converter consists of four terms. First, the sum of the estimated voltage drop across the load bank resistance ($I_{source} \cdot R_0$) and the voltage drop across the FCL (V_{FCL}) was needed to drive the requested current through the device. Furthermore, it was necessary to compensate for the voltage drop across the converter transformer leakage reactance ($k \cdot di/dt$). The gain factor k was determined empirically. This open loop control was completed with a correction term (ΔV_{PID}), using a PID controller in an attempt to better track the reference current.

In this way, when a fault is applied in the simulated system, the fault current in the system flows through the SCFCL module. When the superconducting material quenches it developed a voltage drop across the device which was inserted as a voltage source in the simulated system. Therefore, the behavior of the SCFCL element appeared in the simulated system where it limiting the fault current. The real current through the SCFCL module matches the requested current of the simulation sufficiently for these experiments as illustrated in Fig. 4.

The voltage drop across the source impedance is a suitable indicator for the quality of the PHIL system. This voltage is the difference between the simulated source voltage and the voltage drop across the SCFCL module. As illustrated in Fig. 4 the waveform of this voltage is close to a sine wave after the quench transient of the SCFCL module indicating the good quality of the PHIL setup.
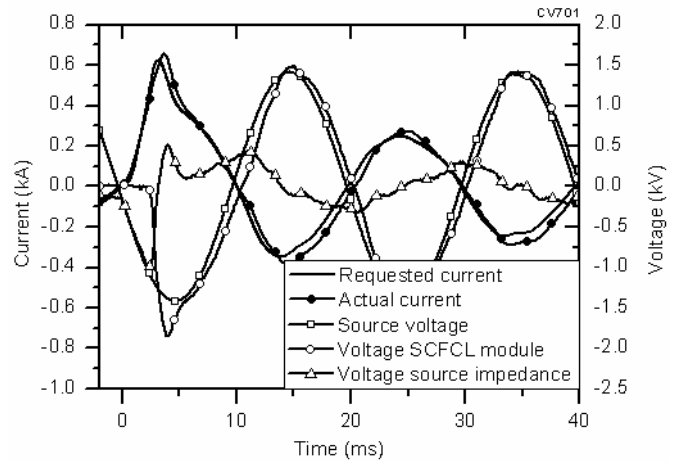

Fig. 4. Comparison between the requested current and the actual current in the hardware circuit. The polarity of the voltage is inverted for better visualization.

The maximum time of current limitation of a SCFCL module depends on the total energy absorbed during a fault limitation event. This energy depends on the applied electrical field and the development of resistance in the normal conducting state. In this case, the tested SCFCL module was able to withstand a voltage of 1 kV(rms) for more than 60 ms without the danger of damage [8].

III. TEST CONDITIONS AND RESULTS

Assuming a 10×10 matrix arrangement of individual modules the voltage level of the simulated circuit was set to 10 kV and the rated current to 1400 A. With these specifications, and the idealized assumption of a homogenous matrix arrangement each SCFCL module carries a tenth of the current and develops a tenth of the applied voltage for the requested time of limitation.

Several tests were conducted through modifications to the simulated system such as

- variation of the source impedance,
- addition of parallel shunt with different impedances, and
- introduction of the temperature dependency of the shunt impedance.

Changes to the testing conditions were introduced solely through modifications to the simulated test circuit within the RTDS environment shown in Fig. 3 while no change of any hardware was required.

For each of the tests the SCFCL module was immersed in open bath liquid nitrogen under normal pressure (at approximately 77 K).

A. Variation of the source impedance

The values used for the source impedance of the simulated test circuit were based on typical values of grid impedances in the medium voltage levels with a constant X/R ratio of 10. The lowest tested source impedance was 0.95 Ω and the highest 1.89 Ω which corresponds to a source inductance of 3 mH and 6 mH, respectively. The prospective fault currents

for the different grid impedances range from 10.6 kA to 5.3 kA.

The stability of the PHIL simulation generally depends on the ratio of source impedance and impedance of the SCFCL module [5]. Furthermore, time delays in the feedback signal to the simulation introduced another potential cause for instability of the PHIL setup. In order to avoid difficulties with these instability issues, experimentation was limited to inherently stable configurations. Therefore, a minimum value for the ratio of the effective system impedance to the SCFCL impedance was required, resulting in the choice of 0.95 Ω as the minimum source impedance. Below this value oscillations in the SCFCL current were perceivable indicating the onset of instabilities.

Fig. 5 shows the limiting behaviour of the SCFCL module with different values of source impedance. The voltage amplitudes across the SCFCL module show no significant changes due to the changes in source impedance. A small decrease in the first peak of the fault current is noticeable as the source impedance is increased. However, the effects of varying the source impedance do not appear to be significant after the first half-cycle, as in this case the impedance of the SCFCL is dominant in this system.
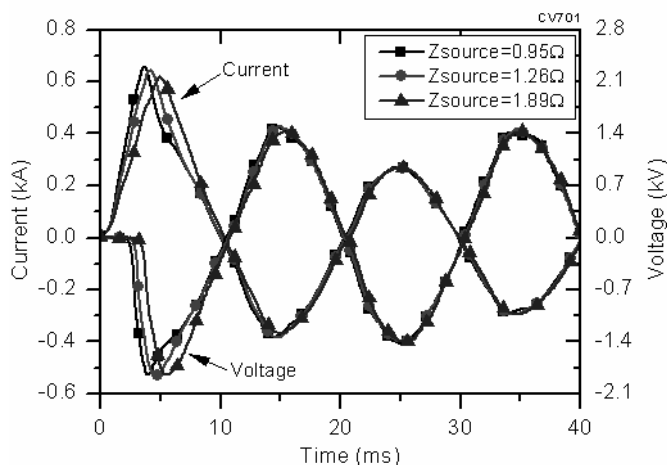

Fig. 5. Effect of source impedance on fault current and voltage along the SCFCL module. The polarity of the voltage is inverted for better visualization.

B. Adding of a parallel shunt with different impedances

For the second set of tests, a resistive-inductive shunt was added in parallel to the SCFCL module. Again, the stability of the test system depends generally on the ratio of source impedance and the impedance of the SCFCL module.

A parallel shunt lowers the effective impedance of the simulated system and causes instabilities in the PHIL test system at low effective impedances of the simulated system. For these cases, the source impedance was held constant at 0.95 Ω. In this configuration, the approach to instability with decreasing shunt impedance was noticed by oscillations in the SCFCL current when the shunt impedance reached about 2.5 Ω, as shown in Fig. 6. Thus, the effective Thevenin impedance of the simulated system at the stability limit was found to be the 0.69 Ω (0.95 Ω in parallel with 2.5 Ω).
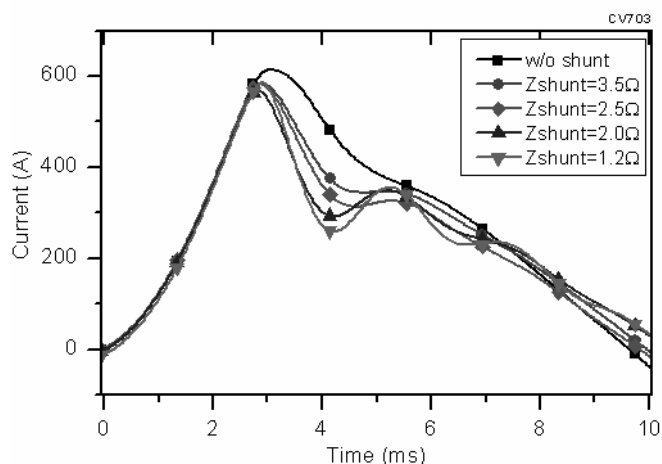

Fig. 6. Effect of adding parallel to the stability PHIL test system. The current through the SCFCL module begins significantly to oscillate with a shunt impedance below 2.5Ω (source impedance 0.95Ω).

Initial experiments were made with a temperature independent shunt impedance. Nevertheless, the presence of the parallel impedance to the SCFCL module strongly influences the source current, while the influence on the current through the SCFCL module was marginal. Fig. 7 shows the source current of the simulation in the 10 kV system. Note that the voltages and currents at the SCFCL module were only one tenths of the values shown in Fig. 7. In contrast to changing source impedance, the change of the parallel shunt impedance affects the current amplitude during the full current limitation.
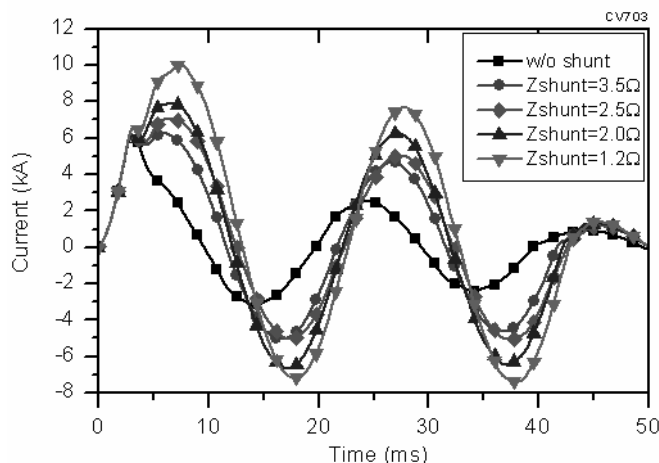

Fig. 7. Effect of additional parallel impedance on the simulated source current of the SCFCL (current through SCFCL module and shunt). The amplitude of the source current shows a strong dependence on the shunt impedance.

The effects of the increase in resistance that might be expected for a physical shunt were also studied by performing tests with a temperature dependent shunt model implemented in simulation. Results from these tests, illustrating the reduction in the shunt current as the shunt resistance increases, are shown in Fig. 8.

Shortly after the current commutates from the SCFCL module to the parallel shunt, the temperature of the shunt starts to rise which is associated by a rise of the shunt resistance. The effect of the rising resistance is the change of

the X/R ratio of the parallel shunt and of the system respectively. This causes a change of amplitude as well as a phase shift of the shunt current relating to the source current.
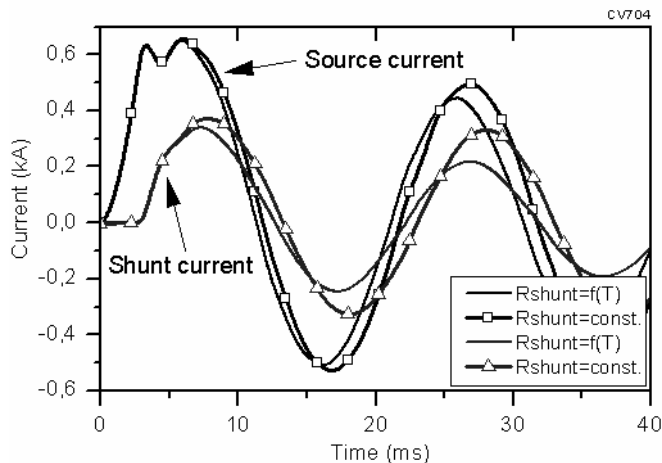

Fig. 8. Influence of temperature-dependent shunt impedance. The thin lines show the profile with temperature independent shunt impedance. The thicker lines, marked with symbols, show the current profile with the temperature-dependent shunt impedance.

As expected a parallel shunt is suited to reduce the dissipated energy in the SCFCL module. Generally, the lower the dissipated energy in the coated conductor the shorter the recovery time of the coated conductor. With the real measured data on the SCFCL module the dissipated energy of the module was calculated. Fig. 9 shows the cumulative dissipated energy of the SCFCL module for different parallel shunt impedances. The dissipated energy drops significantly by adding parallel impedances while the limited source current increases (compare Fig. 7).
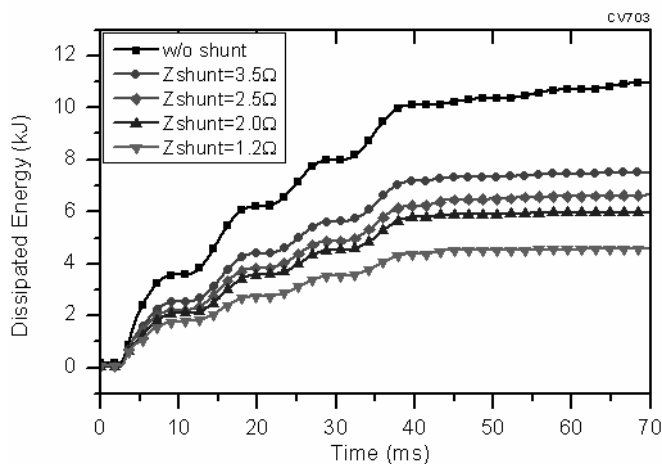

Fig. 9. Dissipated energy in the SCFCL module with different shunts in parallel. The fault was cleared after 40 ms. The increase of dissipated energy after clearing the fault is due to a small load current through the test circuit.

IV. CONCLUSION

The first test of a SCFCL by using the Power-Hardware-in-the-Loop test method with closed loop approach (controlled current) was successfully demonstrated on a SCFCL module using approx. 10 m segment of YBCO coated conductor as limiting element. The results of this work demonstrate the potential of this test method. Especially the transient of the SCFCL module from the superconducting state to the normal conducting state, which is difficult to simulate can be rigorously evaluated under different operating conditions. Furthermore, Power-Hardware-in-the-Loop testing affords a method for accurately incorporating different power system phenomena, system configurations, and SCFCL configurations when studying the insertion of SCFCL module into power grids. It was found that instabilities in the PHIL setup can occur which may require advanced control measures to be devolved and implemented in the future. Future work will focus on improvement of the very simple interfacing method utilized herein in order to obtain better current tracking and accommodate a wider range of test scenarios.

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