IEEE/CSC SUPERCONDUCTIVITY NEWS FORUM (global edition) October 2014
Invited Presentation 1EOr2A-01 given at ASC 2014, Charlotte, August 10 – 15, 2014

Applied Superconductivity Conference, ASC 2014
August 10-15, Charlotte, NC

MIT LL Superconductor Electronics Fabrication Process for VLSI Circuits With 4, 8, and 10 Niobium Layers

Sergey K. Tolpygo, Vladimir Bolkhovsky, Terry Weir, William D. Oliver, Leonard M. Johnson, and Mark A. Gouker

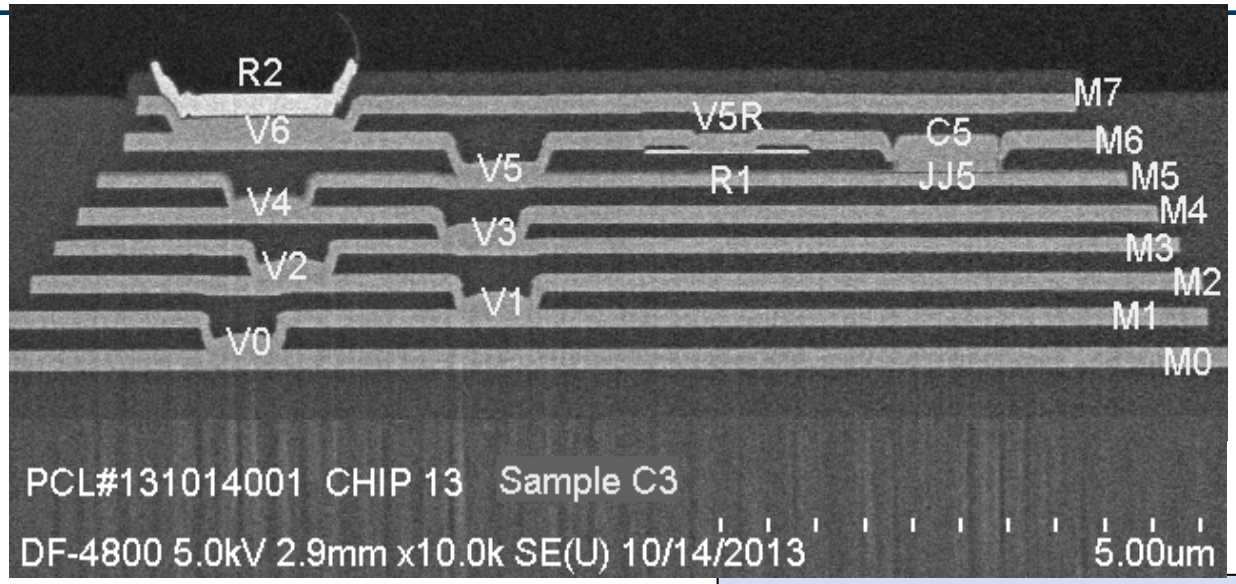
Quantum Information and Nanosystems Technology Group
Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02420

This work was sponsored by the IARPA under Air Force Contract FA872105C0002. Opinions, interpretations, conclusions, and recommendations are those of the authors, and not necessarily endorsed by the United States Government.

Outline

- **SFQ Process Overview**
  - **SFQ fabrication process nodes**
  - **General process description (4M, 8M, and 10M)**
  - **Multi-chip module process**
- **SFQ fabrication process highlights**
  - **Process Control Monitors and test examples**
  - **Junction properties and sizing, inductors, vias**
  - **SFQ5ee and beyond: shrinking feature size to 180 nm, stud vias**
  - **See also our poster presentations 2EPo1A-02 and 2EPo1A-03 on Tuesday morning for more info on JJs, inductances, etc.**

MIT LL Fully Planarized SFQ Process



Process Features

- Nb/Al-AlO_x/Nb JJ technology
- 10 kA/cm^2 (100 μA/μm^2) baseline
- 200-mm Si wafers
- 4-, 8- &10-Nb layer nodes
- Min feature sizes 350 nm
- Full planarization for uniformity
- Transition to stacked/stud vias

- RQL circuits with > 7.2·10^4 JJs per chip have been successfully demonstrated in the 8-layer SFQ4ee process node, see Micah Stoutimore, et al. presentation 4EOr3A-06 on Thursday
- New-SFQ circuits with > 2.1·10^4 JJs have been successfully demonstrated in the 4-layer SFQ3ee process node, see Vasili Semenov, et al. presentation 4EOr3A on Thursday
- ERSFQ 8-bit adders, see Alex Kirichenko et al. presentation 2EOrC-04 on Tuesday

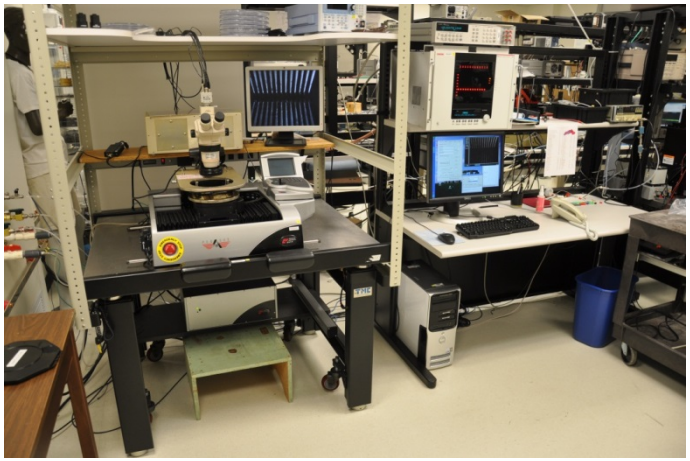
Lincoln Microelectronics Laboratory

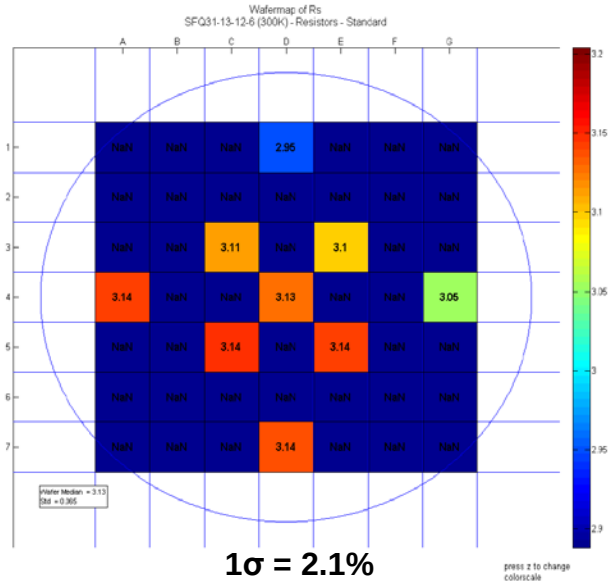
- **Classification**
  - **Total: 6,400 m^2 (Class-10: 740 m^2; Class-100: 910 m^2)**
- **Production-class 90-nm CMOS, 200-mm tool set**
  - **Cluster metallization (sputter & MBE), etch, CMP, …**
  - **Advanced lithography: i-Line, 248-nm, 193-nm, e-beam**
  - **Full SPC, electronic traveler, technicians**
  - **~ 10,000 wafer starts per year**
- **Cryogenic electronics fabrication**
  - **SFQ with deep submicron JJs and wiring features**
  - **Superconducting MCM**
  - **Superconducting qubits and ion traps**
- **SFQ program 200-mm tool set**
  - **Dedicated metal deposition tools**
  - **Dedicated etch and dielectric deposition tools**
  - **Shared lithography, CMP, and defect inspection tools**
  - **248-nm and 193-nm photolithography tools**

Microelectronics Laboratory

Room-Temperature and 4 K Process-Yield Testing

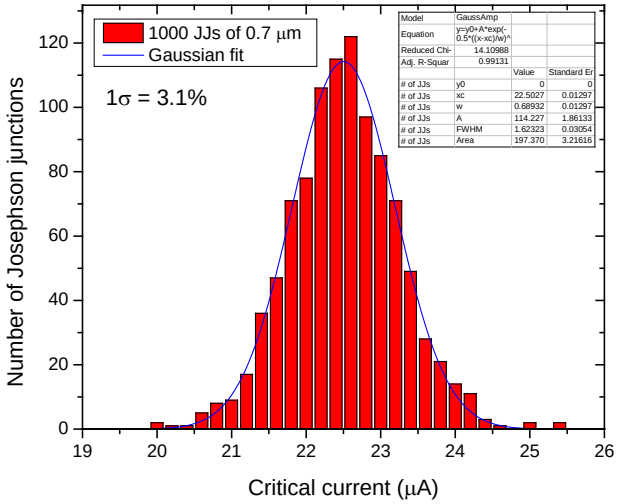
- **Room-temperature wafer-scale testing**
  - **Three semi-automatic probe stations**
  - **Automation software**
- **Cryogenic testing**
  - **14-chip LHe immersion probe**
  - **Switch matrix and test equipment**





1σ = 2.1%

Mo room-temperature sheet resistance



4 K I_c spread data

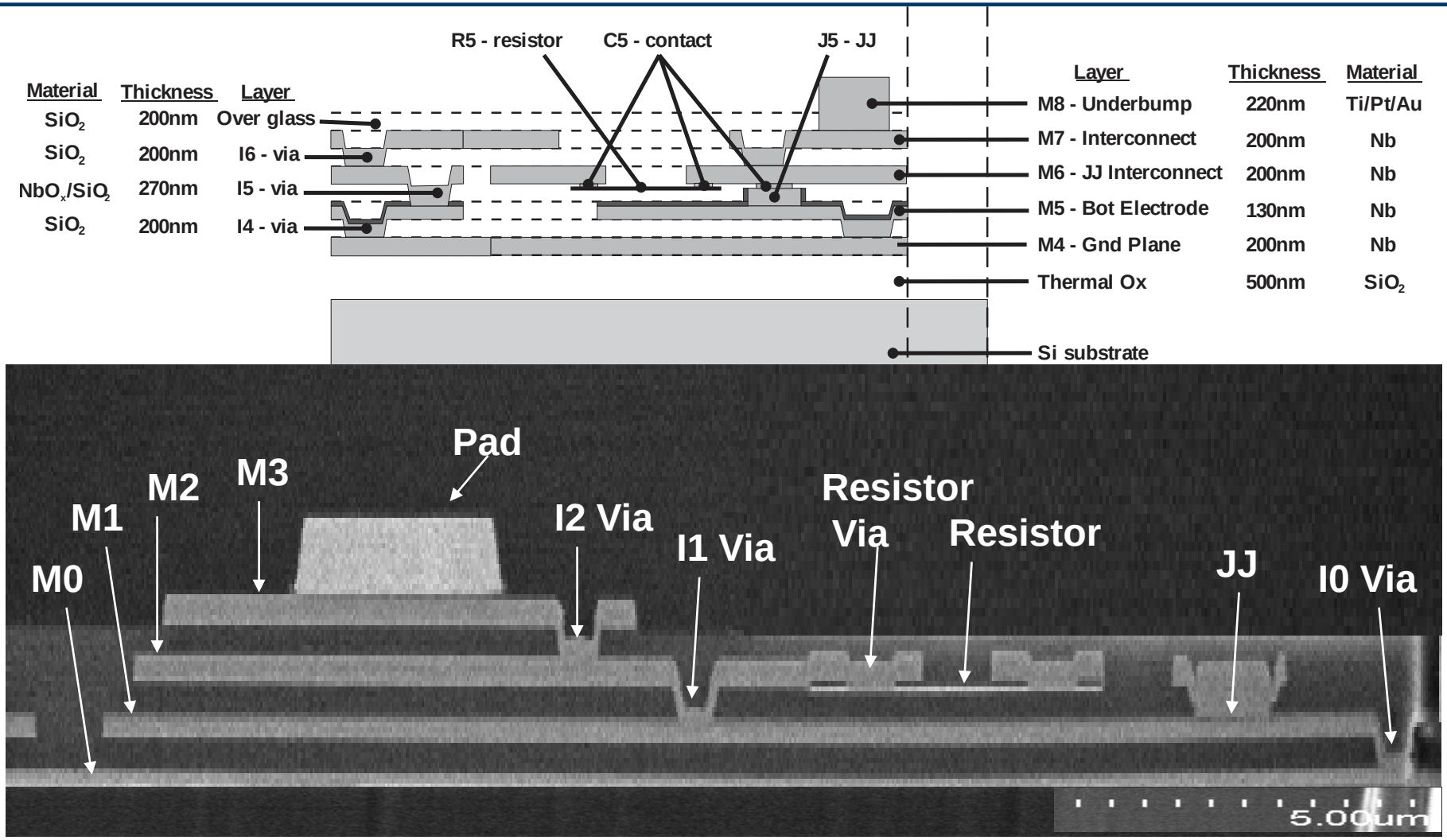
Government Furnished Foundry for C3 Program

- **MIT Lincoln Laboratory support for IARPA Cryogenic Computing Complexity C3 program**
  - **Superconducting integrated circuit fabrication (RQL, SFQ, ERSFQ, eSFQ, etc.)**
    - **Digital logic and memory applications (no magnetic material)**
  - **Superconducting MCM fabrication and indium-bump die attachment**
  - **Process testing & monitoring**
- **Snapshot**
  - **Fully planar process, 100 μA/um^2 (10 kA/cm^2), 500 nm JJ**
    - **Years 1 - 2: 4 Nb metal layers**
    - **Years 1 - 2: 8 Nb metal layers**
    - **Years 2 - 5: 10 Nb metal layers**
  - **C3 program participants design into these processes**
    - **6 tape-outs per year**
    - **Average 3-month cycle time depending on process**
  - **Work with design teams to maximize utility and output of GFF to meet C3 program goals**

MIT-LL SFQ Process Nodes

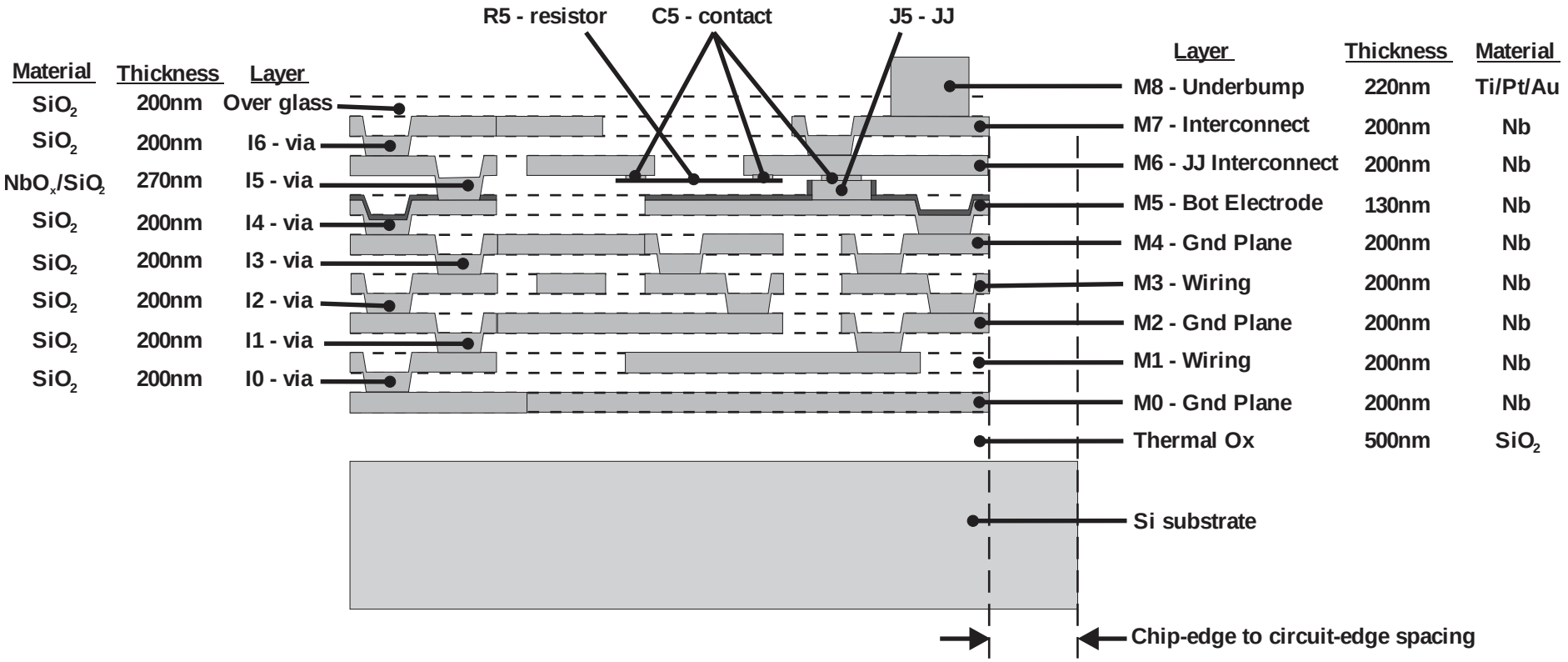
Fabrication Process Attribute	✓	✓	Process Node		
	SFQ3ee	SFQ4ee	SFQ5ee	SFQ6ee	SFQ7ee
Critical Current Density ($\mu A/\mu m^2$)	100	100	100	100	100
JJ diameter (surround) (nm)	700 (500)	700 (500)	700 (300)	500 (200)	500 (200)
Number of superconducting layers	4	8	10	10	10
Line width (space) (nm)	500 (1000)	500 (700)	350 (500)	250 (300)	180 (220)
Metal thickness (nm)	200	200	200	200	150
Dielectric thickness (nm)	200	200	200	200	180
Resistor width (space) (nm)	1000 (2000)	1000 (1000)	700 (700)	500 (500)	350 (350)
Resistor value (ohms per square)	2	2	2 and 0.002	2 and 0.002	2 and 0.002
Via diameter (surround) (nm)	700 (500)	700 (500)	500 (350)	350 (250)	350 (200)
Via type	Etched, Stacked Staggered	Etched, Stacked Staggered	Stud, Stacked	Stud, Stacked	Stud, Stacked
Process Development	Complete	Advanced	Underway	Underway	Underway
Early Access Availability	2013	Now	2015	2016	2017
Primary Process	Now	Sep. 2014	2016	2017	2018

4-Layer Process Node: SFQ3ee
Cross Section



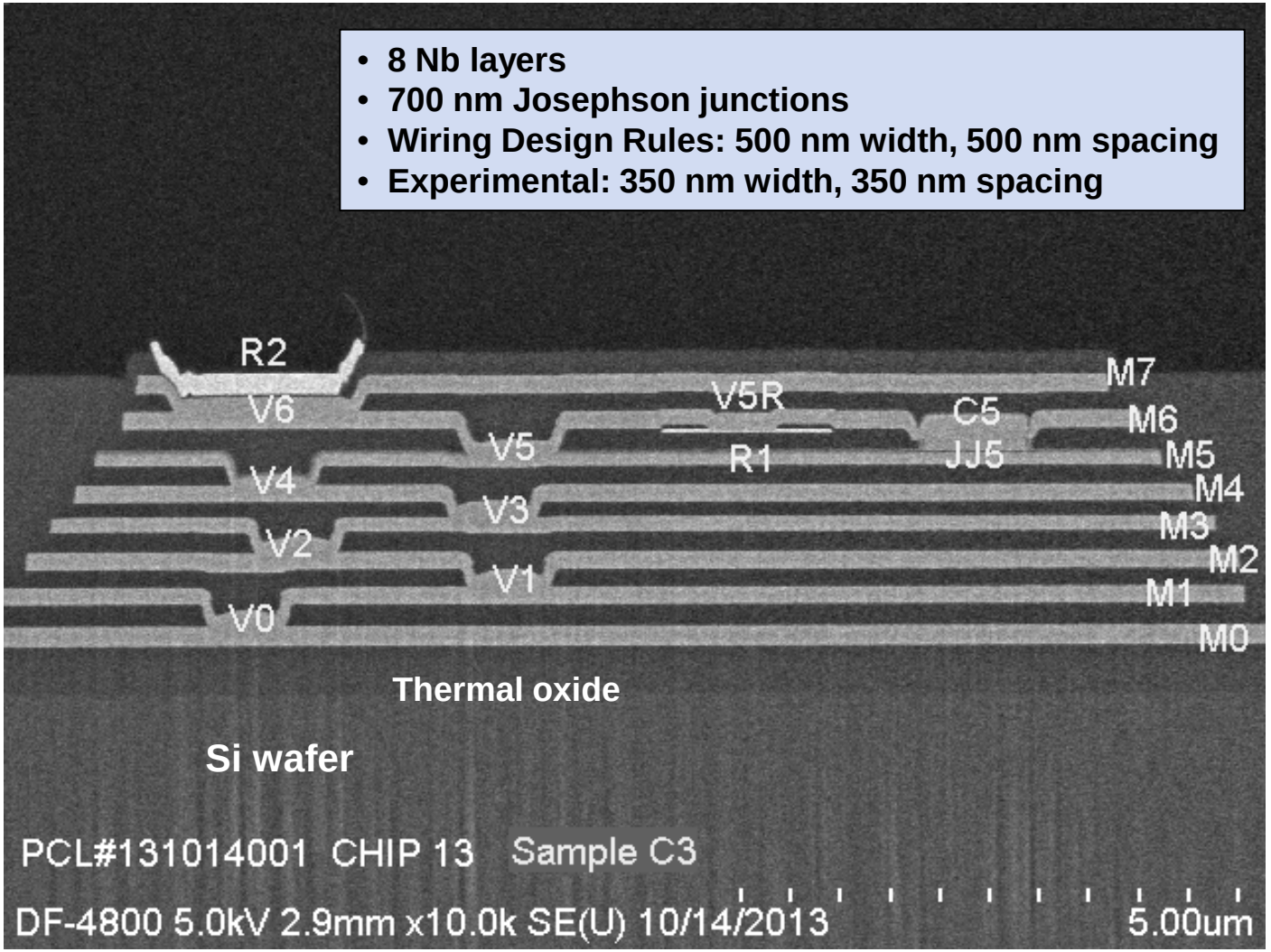
- 4 Nb layers
- 700 nm Josephson junctions
- Wiring: 500 nm width, 700 nm spacing

8-Nb Layers Process Node: SFQ4ee

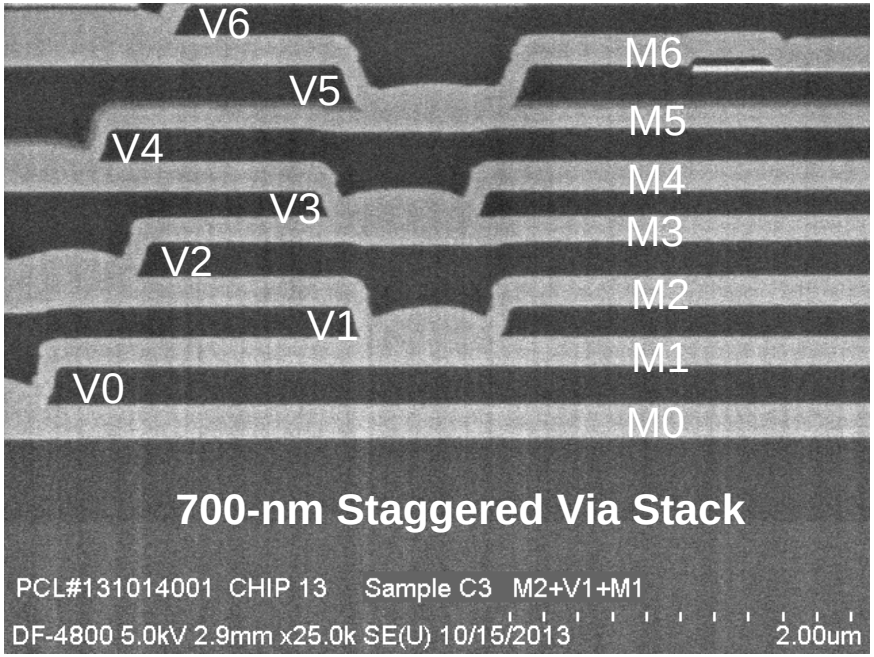


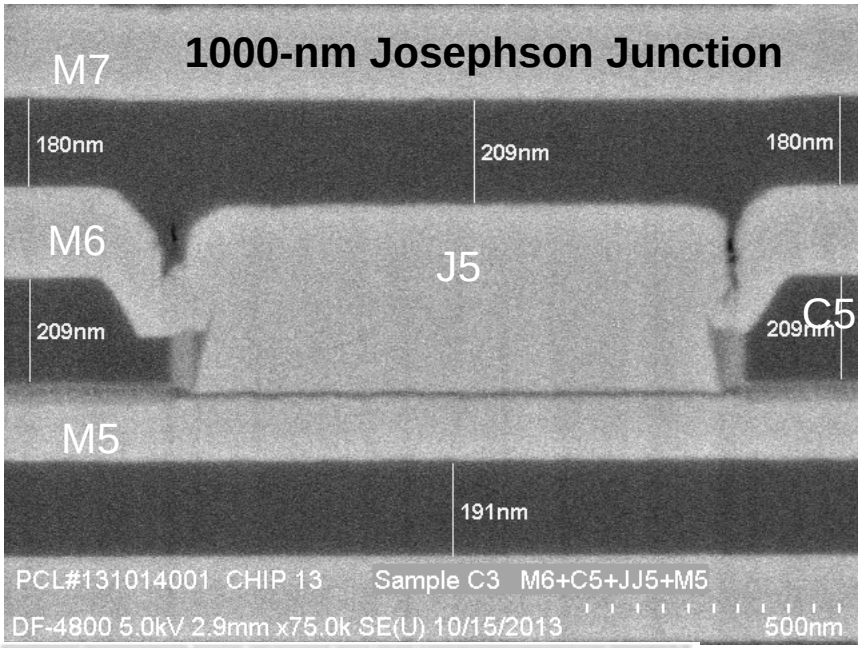
- 8 Nb layers
- 700 nm Josephson junctions
- Wiring: 500 nm width, 500 nm spacing

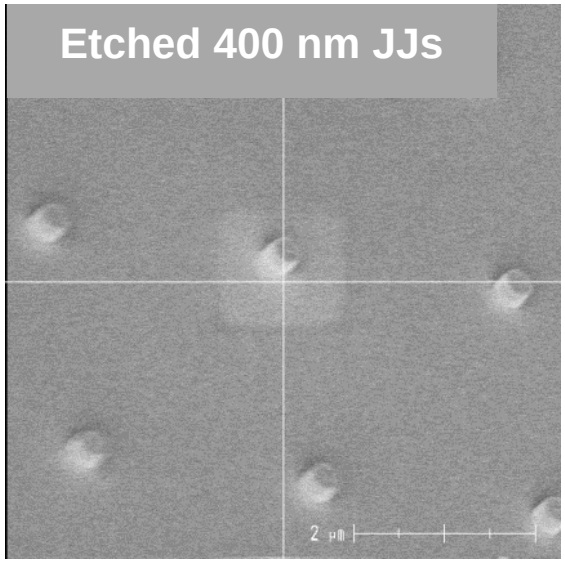
8-Nb Layer Process Cross Section SEM

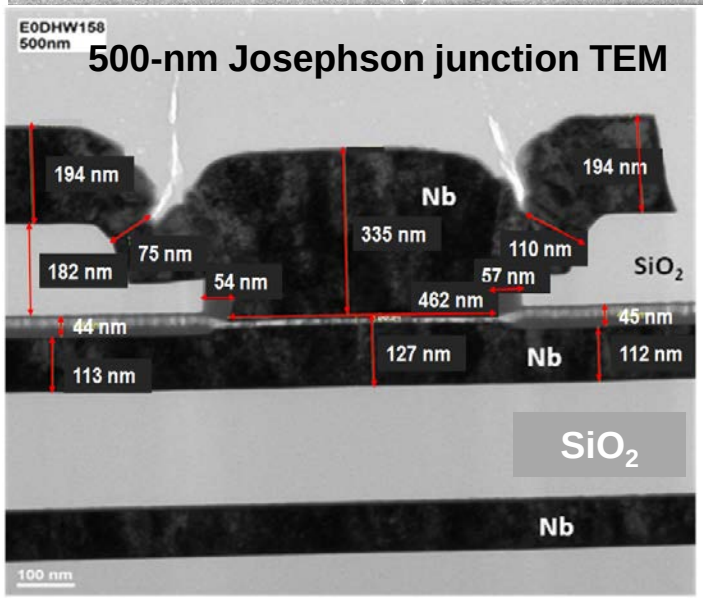


SEM Images of 8-Nb Layer Process

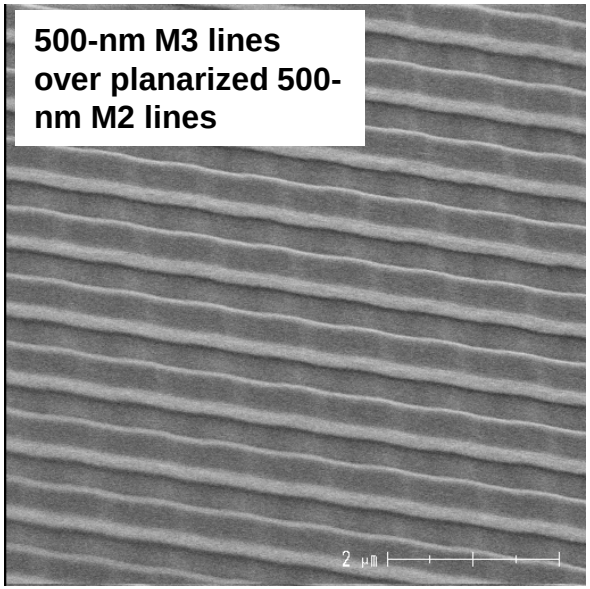


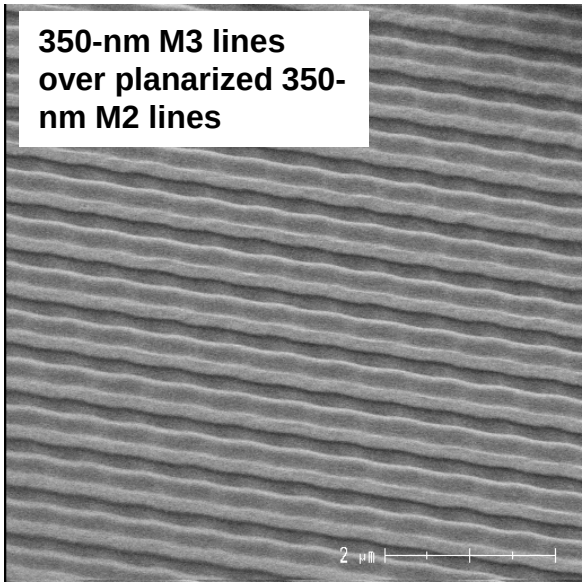


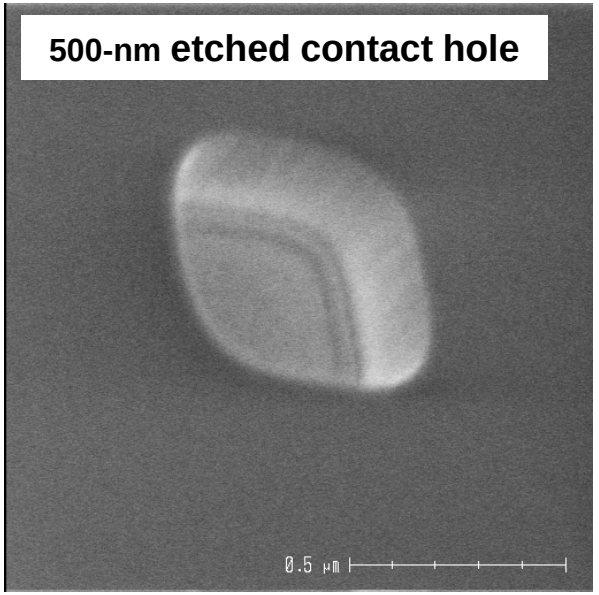


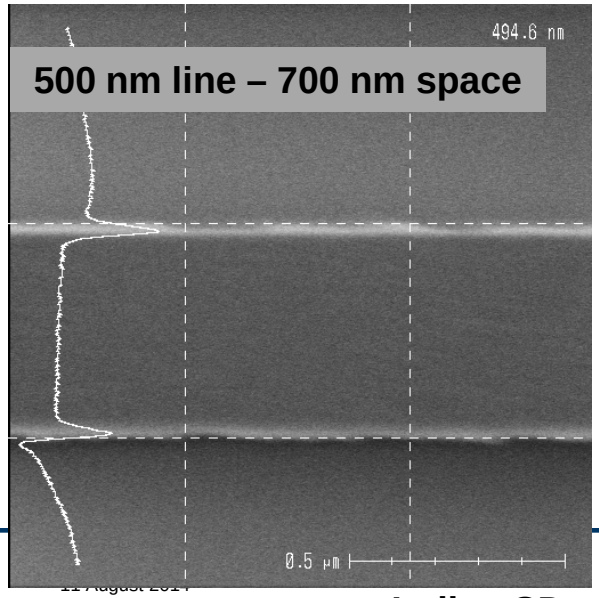


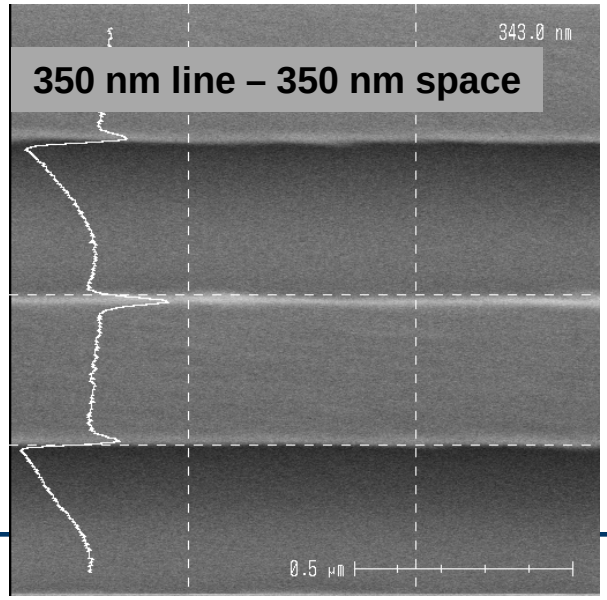
Process Pictures of Wires and Via Formation

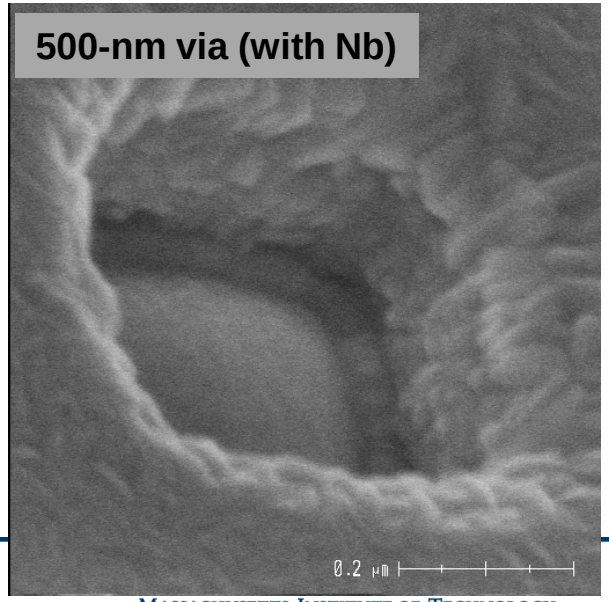






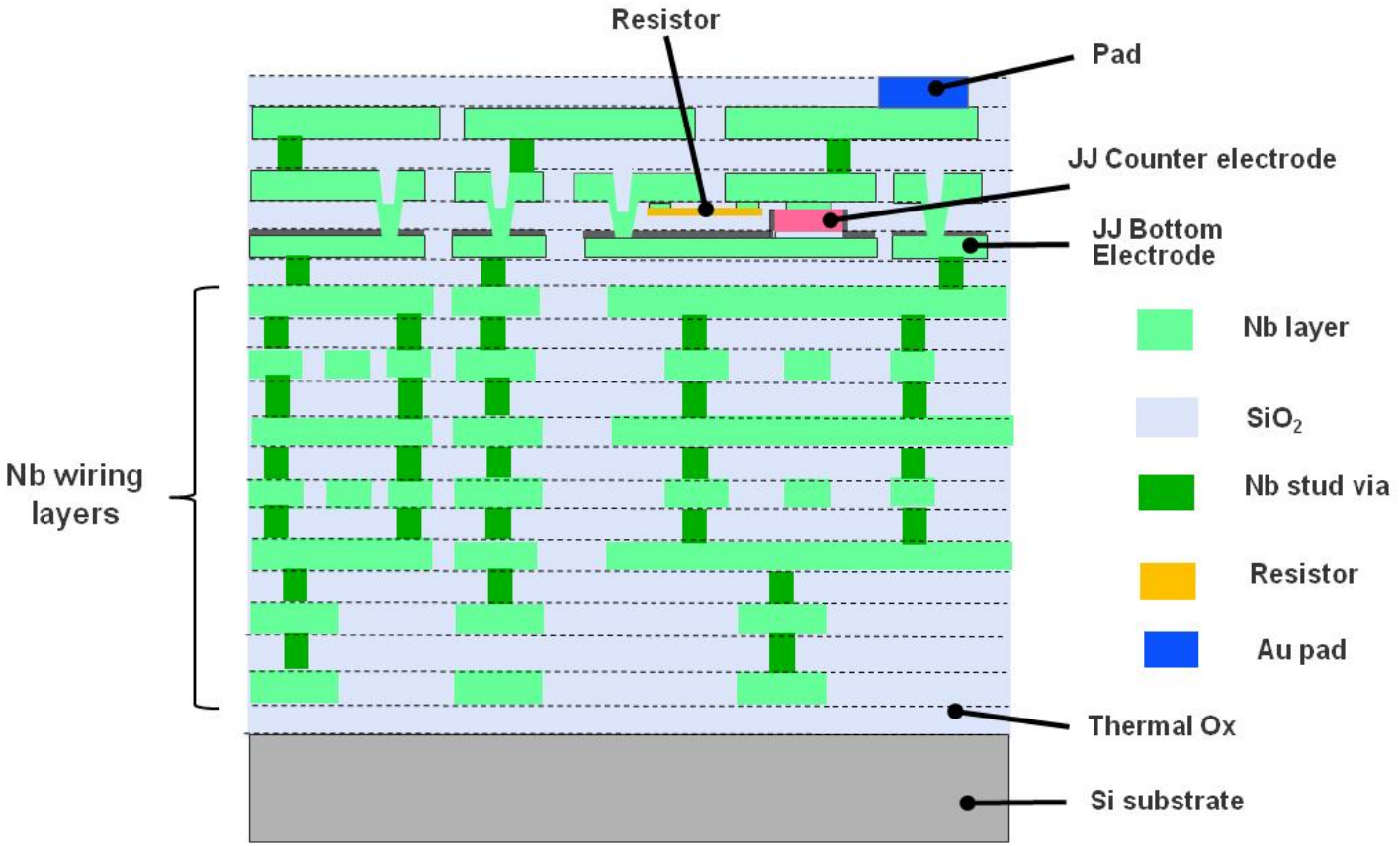






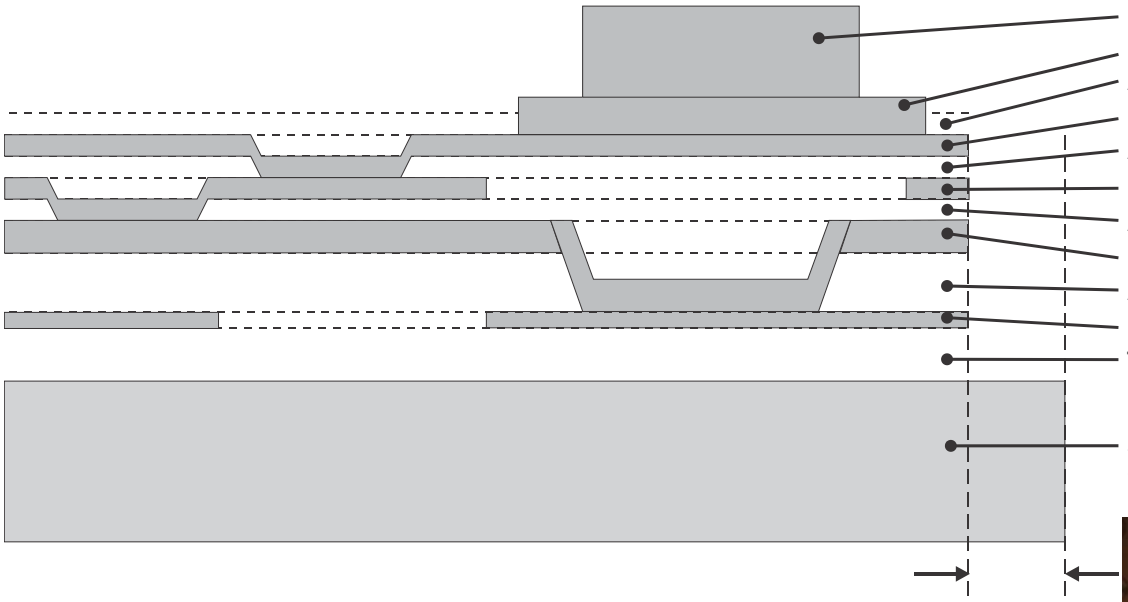
In-line CD measurements

Target 10-Nb Layer Node: SFQ5ee



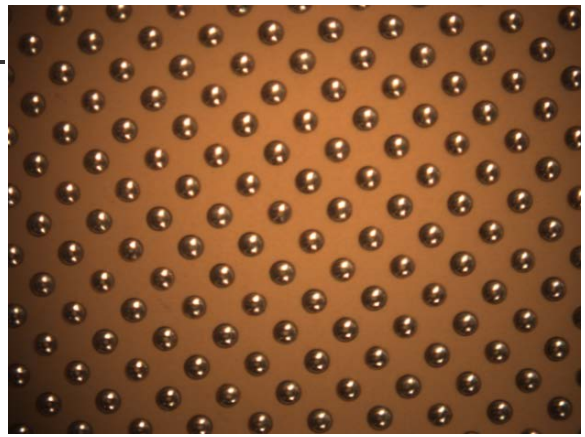
- 10 Nb layers
- 500 nm Josephson junctions
- Wiring: 180 nm width, 200 nm spacing
- Stud vias
- Two layers of resistors

Process for 4-Metal-Layer Superconducting MCM



Layer	Thickness	Material
M5 - Bump	8 um	In
M4 - Pad	220nm	Ti/Pt/Au
A3 - overglass	200nm	SiO_2
M3 - Gnd	200nm	Nb
A2/I2 - IMD/via	200nm	Nb/SiO_2
M2 - Data	200nm	Nb
A1/I1 - IMD/via	200nm	Nb/SiO_2
M1 - Gnd	250nm	Nb
A0/I0 - IMD/via	550nm	Nb/SiO_2
M0 - Clock	150nm	Nb
Thermal Ox	500nm	Thermal SiO_2
Si substrate (not high rho)		

- Dielectric thicknesses chosen to facilitate impedance targets
  - 50-ohm for 'clock' line, 15-ohm for 'data' line (subject to revision)
- In bumps: 8-15 μm diameter on 35 μm pitch
- Up to $6 \cdot 10^4$ bumps per chip in flip-chip MCMs demonstrated
- MCM size up to 5 cm by 5 cm



Reflowed Indium Bumps (Optical Image)
15 μm bump diameter on 35 μm pitch

Outline

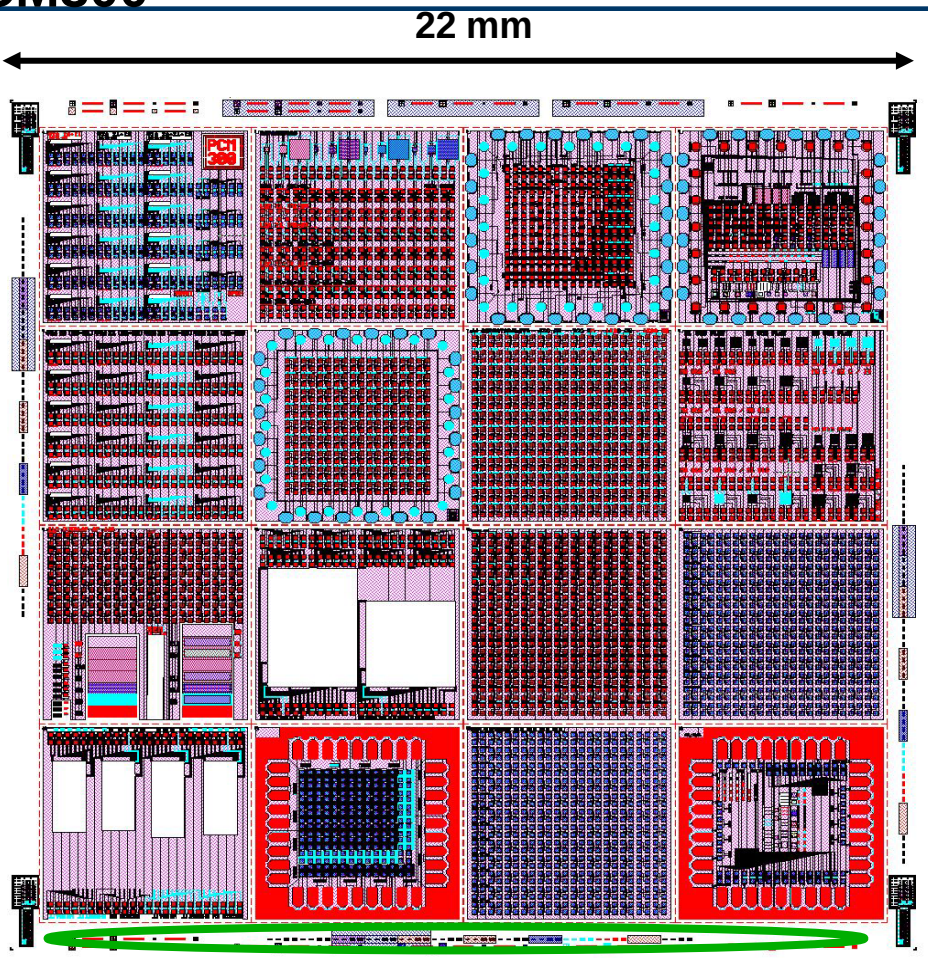
- **SFQ Process Overview**
  - **SFQ fabrication process nodes**
  - **General process description (4M, 8M, and 10M)**
  - **Multi-chip module process**
- **SFQ fabrication process highlights**
  - **Process Control Monitors and test examples**
  - **Junction properties and sizing, inductors, vias**
  - **SFQ5ee and beyond: shrinking feature size to 180 nm, stud vias**

  - **See also our poster presentations 2EPo1A-02 and 2EPo1A-03 on Tuesday morning for more info on JJs, inductances, etc.**

SFQ3ee Process Control Monitor

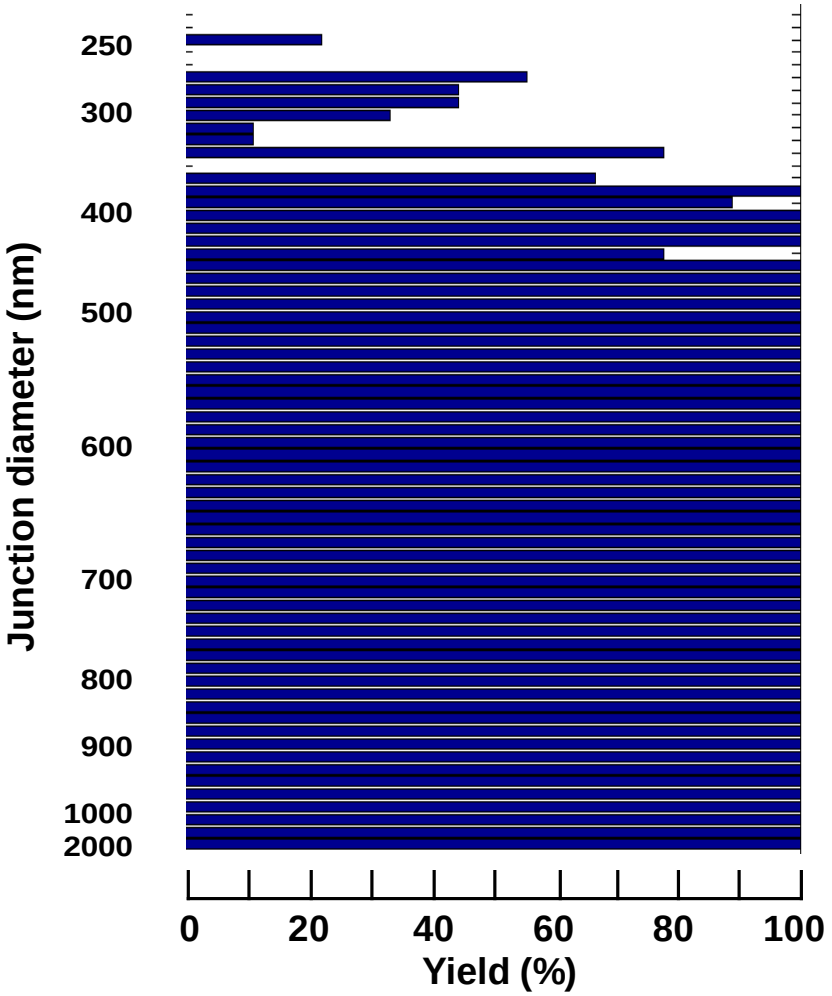
PCM300

Chip 1 Via Chains Staggered, Capacitors	**Chip 2** Capacitors and CBKR Via	**Chip 3** JJ Strings & Resistors	**Chip 4** In-line Process Monitor
Chip 5 Via Chains Individual	**Chip 6** JJs from 200 nm to 15 µm for J_c	**Chip 7** JJ statistics 500 nm 700 nm 1000 nm 1500 nm	**Chip 8** Metal Lines Snake& Combs
Chip 9 Layer Thick Measure SEM, I1R Array	**Chip 10** 400k Via Strings staggered	**Chip 11** JJs from 200 nm to 15 µm for J_c	**Chip 12** JJ statist. 500 nm 700 nm
Chip 13 Stacked 400k Via Strings JJ strings	**Chip 14** Snake & Combs CT, JJ shunted	**Chip 15** JJ statistics 300 nm 350 nm 400 nm 450 nm	**Chip 16** JJ chains Metrology CTT Structures



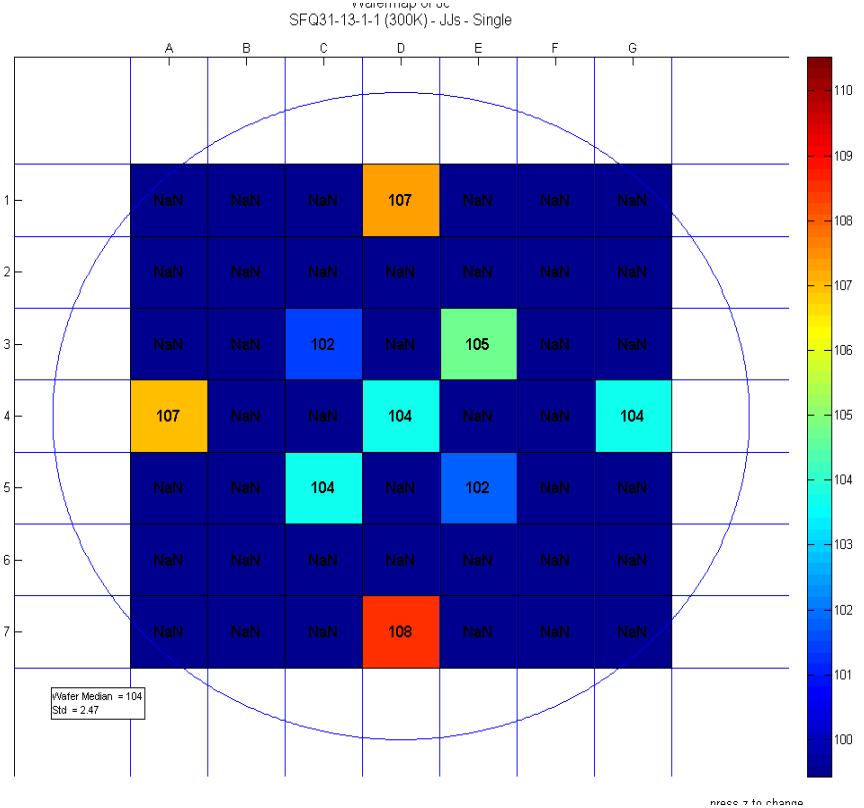
PCM300 includes process test structures for SFQ3ee and smaller-geometry test devices for later C3 process nodes down to 180 nm

Single JJ Yield By Size and J_c Wafer Map



Wafer Map

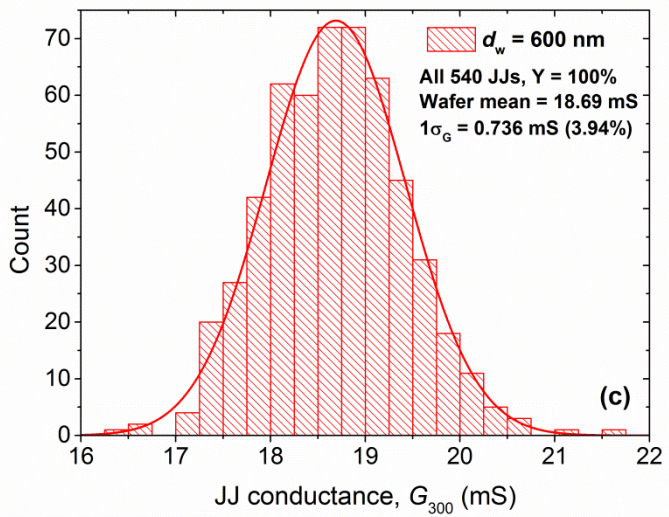
J_C (μA/μm²) at PCM exposure locations



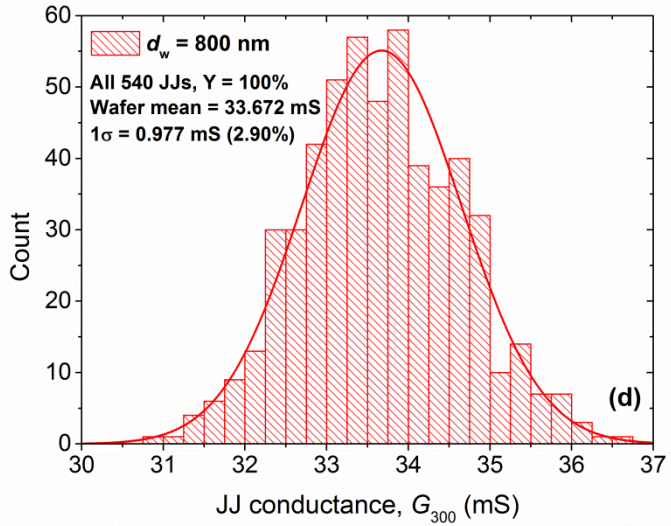
PCM data indicates excellent junction yield down to 450 nm drawn diameter

Josephson Junction PCM Prescreening

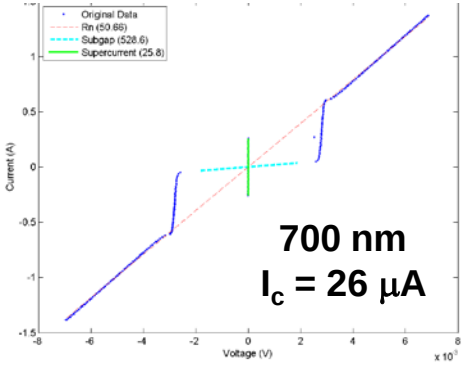
Room Temperature Histogram 600 nm JJs, full wafer, 1σ < 4%



Room Temperature Histogram 800 nm JJs, full wafer, 1σ < 3%



4 K Single-Junction Test



Key JJ testing prior to chip delivery

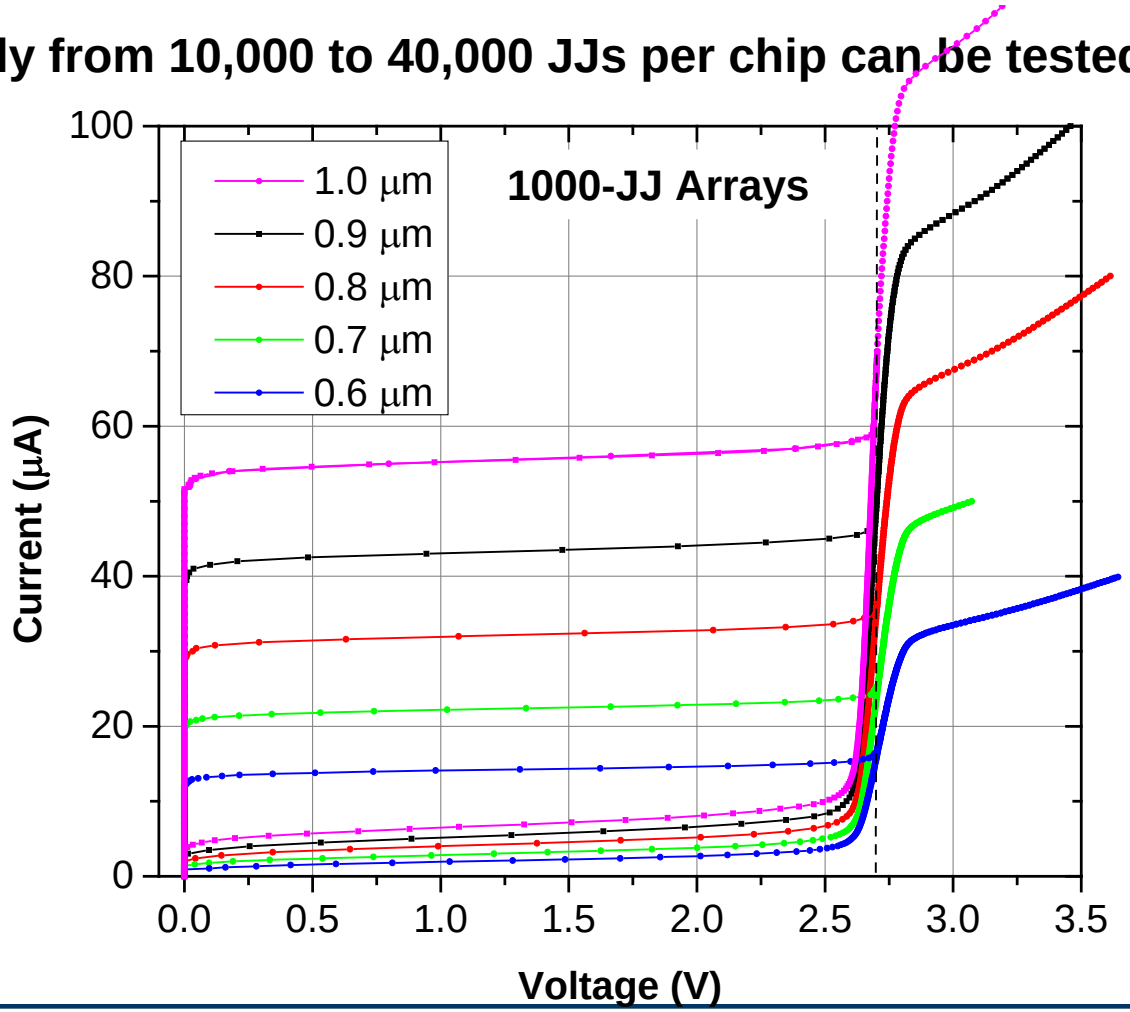
- RT conductance histograms indicating I_C spreads
- Single JJ and JJ arrays 4 K I-V characterization
- I_c of vias and wires

Extensive PCM testing continues at MIT-LL following initial chip delivery to circuit design teams

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

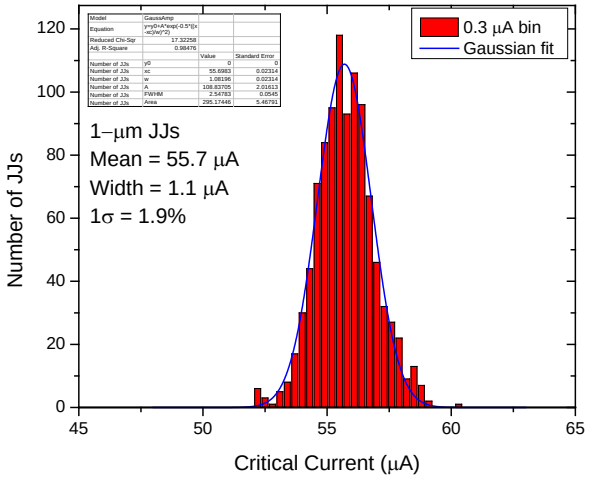
4.2 K Testing of 1000-JJ Arrays

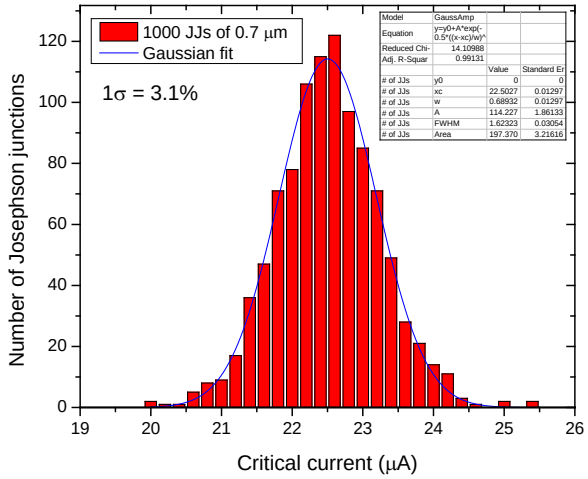
- **Testing of series arrays of 1000 JJs at 4.2 K is an efficient method for evaluating yield of JJs and uniformity of their critical currents**
- **Typically from 10,000 to 40,000 JJs per chip can be tested.**

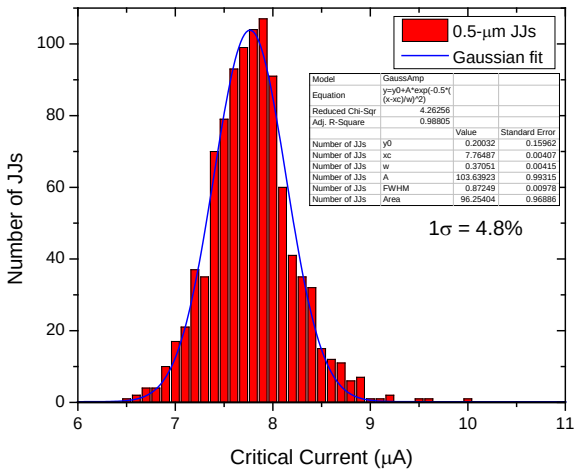


JJ Uniformity ("I_c Spreads") from 4.2 K Measurements and Correlation with RT Data

- **I_c distribution of JJ arrays from 4.2 K measurements**







- **From the I_cR_n = Const. relationship, measuring I_c of JJ arrays at 4.2 K gives similar distributions as the RT measurement of R_n distribution**

JJ drawn diameter (μm)	Critical Current, 1σ (%) @4.2 K	Resistance, 1σ (%) @300 K
0.5	4.8*	3.8
0.7	3.1	3.0
1.0	1.9	1.8

*** I_c of small JJs become affected by thermal and EM noise**

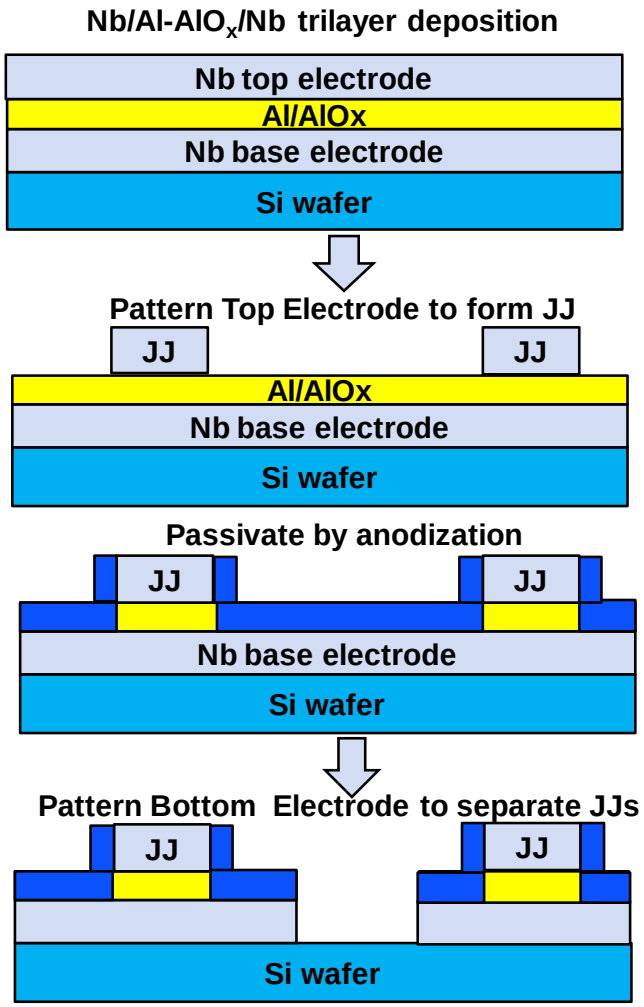
Outline

- **SFQ Process Overview**
  - **SFQ fabrication process nodes**
  - **General process description (4M, 8M, and 10M)**
  - **Multi-chip module process**
- **SFQ fabrication process highlights**
  - **Process Control Monitors and test examples**
  - **Junction properties and sizing, inductors, vias**
  - **SFQ5ee and beyond: shrinking feature size to 180 nm, stud vias**

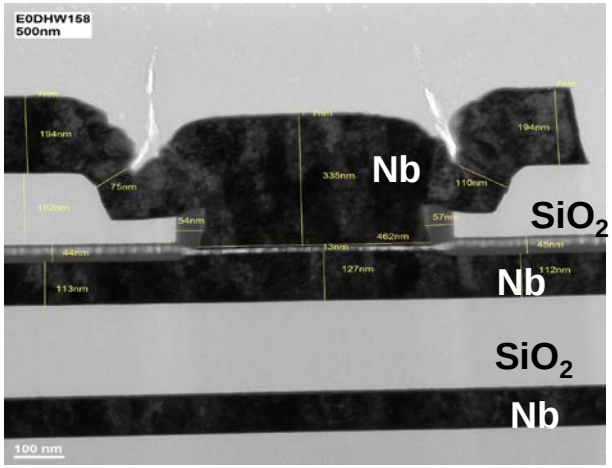
  - **See also our poster presentations 2EPo1A-02 and 2EPo1A-03 on Tuesday morning for more info on JJs, inductances, etc.**

SFQ Fabrication Flow

Josephson Junctions

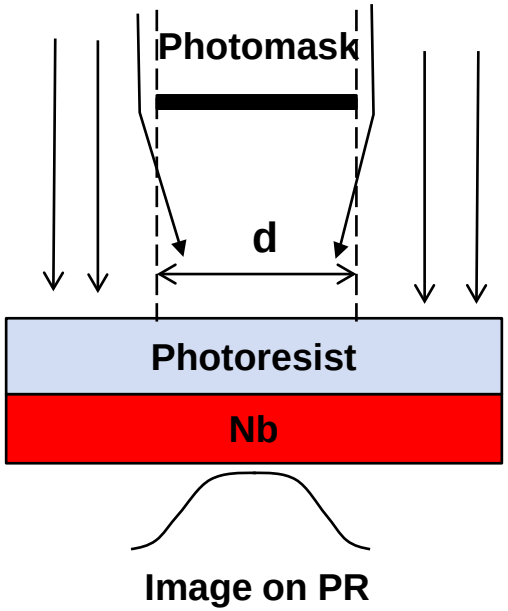


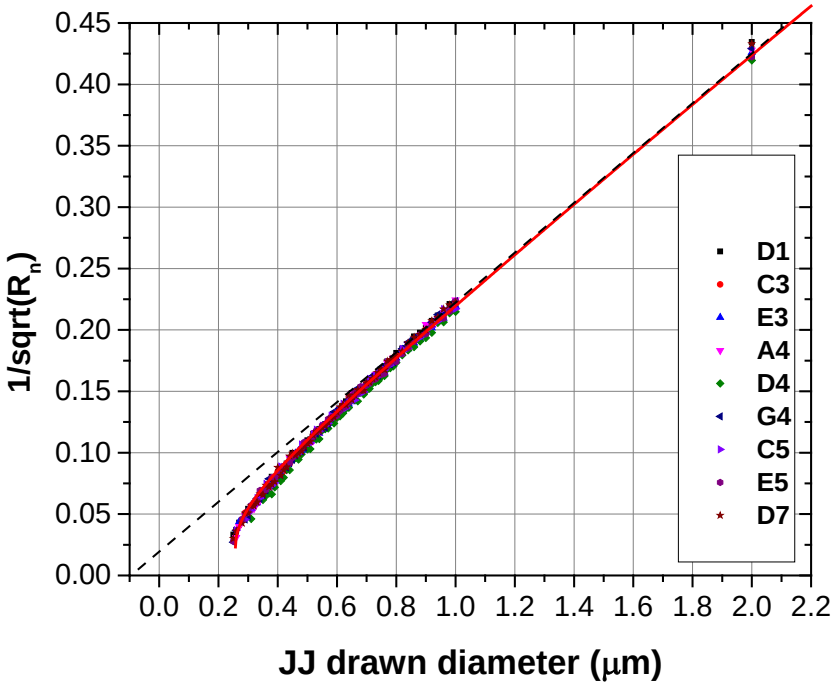
500 nm Josephson Junction TEM



- **Robust JJ fabrication process provides high yield and tight spreads**
- **I_C targeting depends on precision of photolithographic patterning**

JJ Fabrication Near Photolithography Diffraction-Limited Resolution





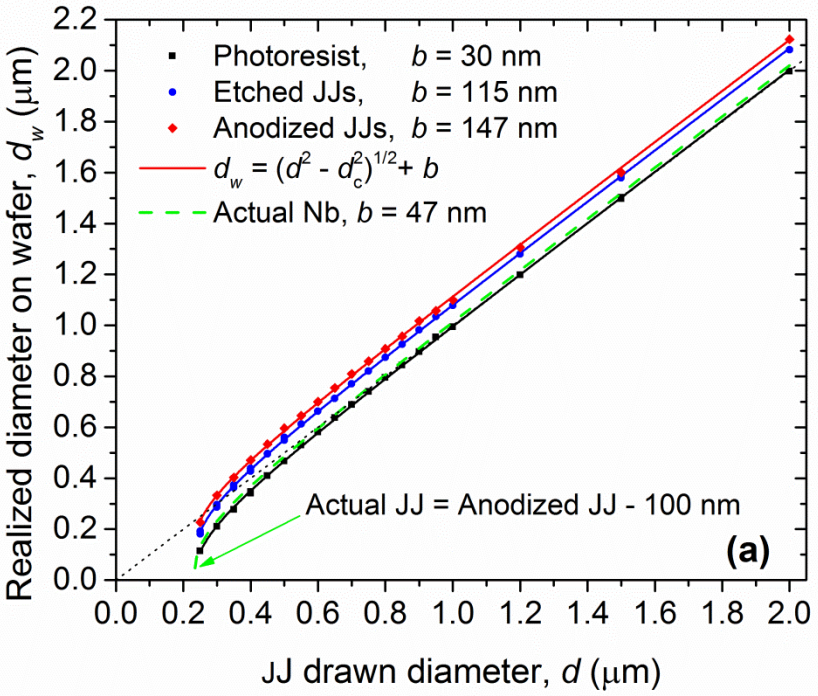
- Need to compensate for photolithography diffraction effects in mask layout to achieve desired JJ sizing
- SFQ3ee (&4ee) design rules provide relationship between 'drawn' JJ diameter d_d on mask and resulting JJ diameter d_w on wafer

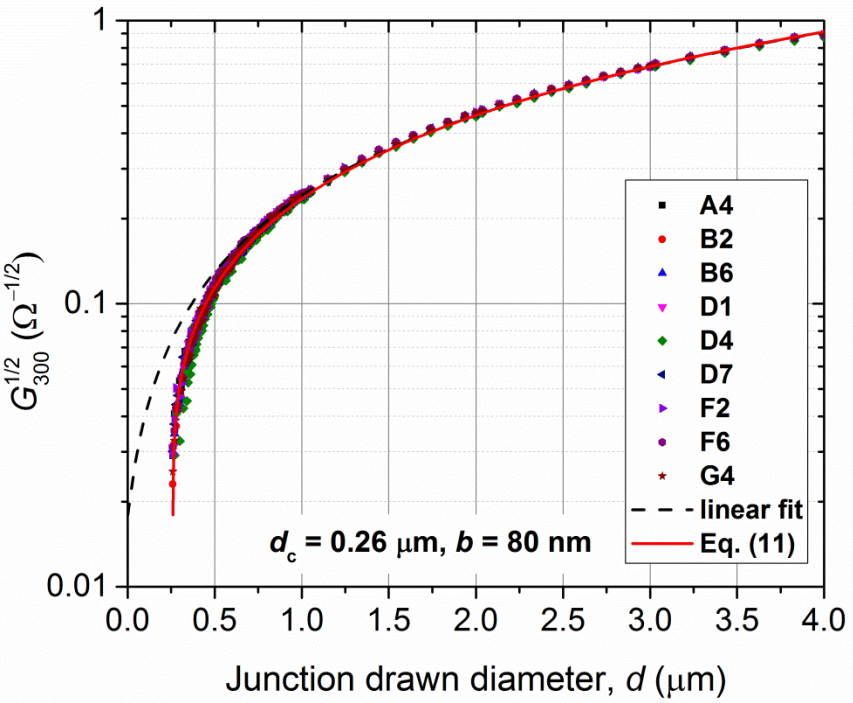
$$d_w = (d_d^2 - d_c^2)^{1/2} + b, \qquad \text{for design: } d_d = [(d_w - b)^2 + d_c^2]^{1/2}$$

- Parameters d_c and b are provided in the Design Rules

See our poster 2EPo1A-02 on Tuesday morning

JJ Size on Wafer vs JJ Size on Photomask



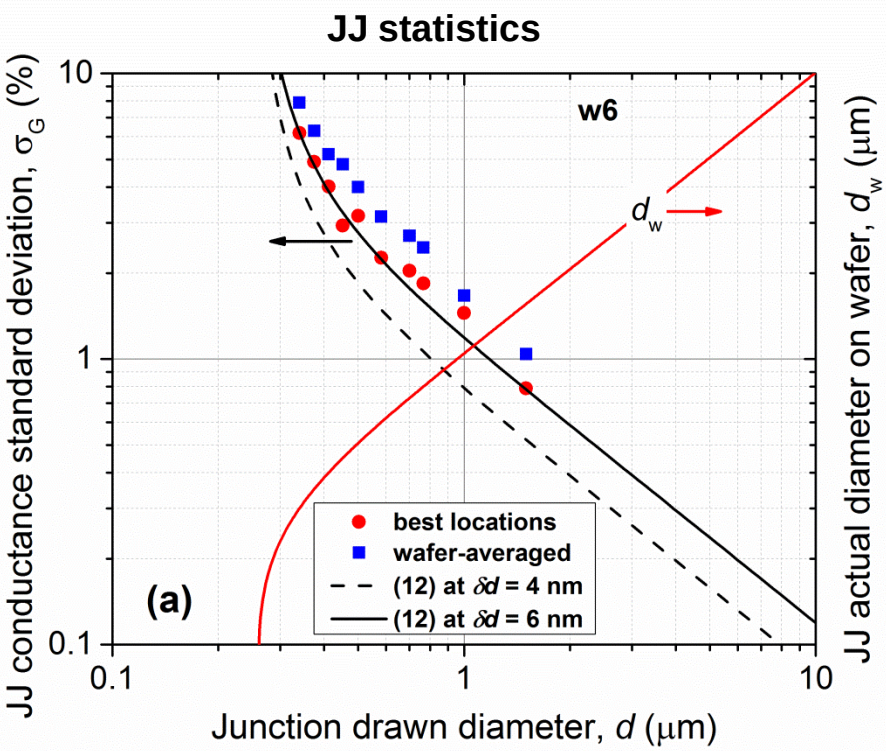


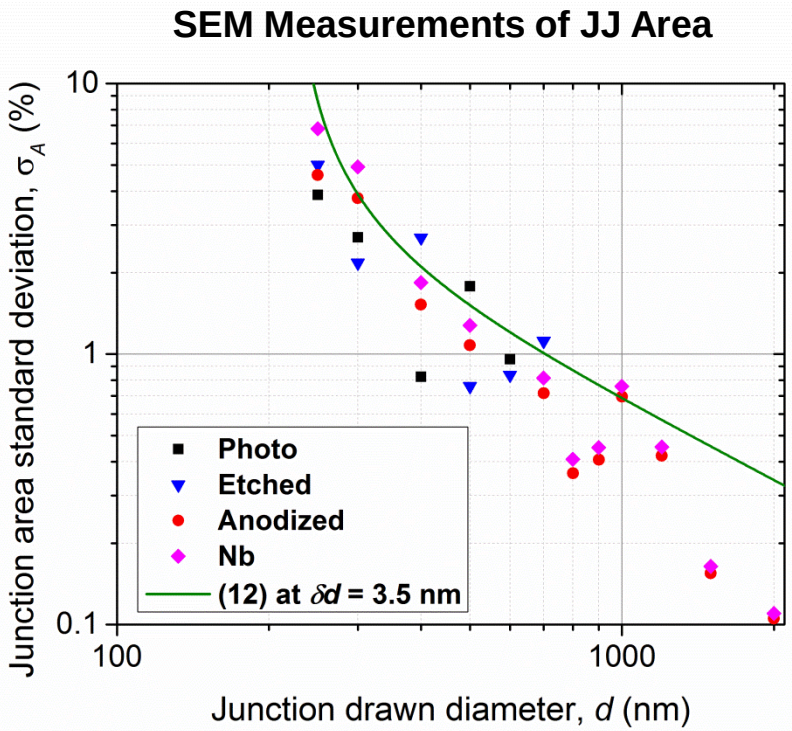
$$d_w = (d_d^2 - d_c^2)^{1/2} + b$$

$$G_N = G_0(\pi/4)d_w^2 \text{ and } I_c = J_c(\pi/4)d_w^2$$

The minimum printable size $d_c \approx 250$ nm for our 248-nm photolithography, and ~ 130 nm for our 193-nm photolithography

PCM300 Junction Characterization: 10 kA/cm² process

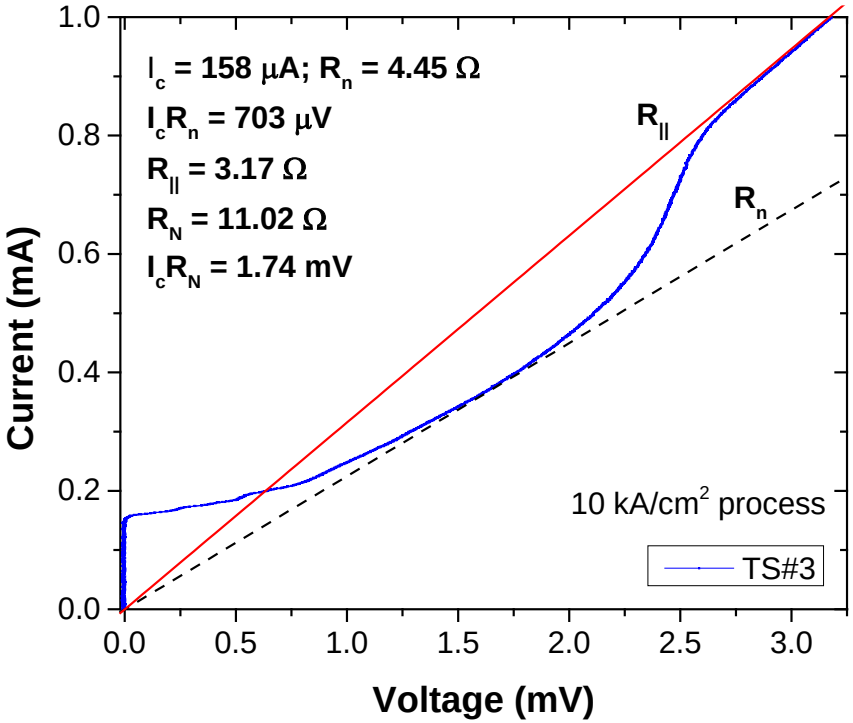


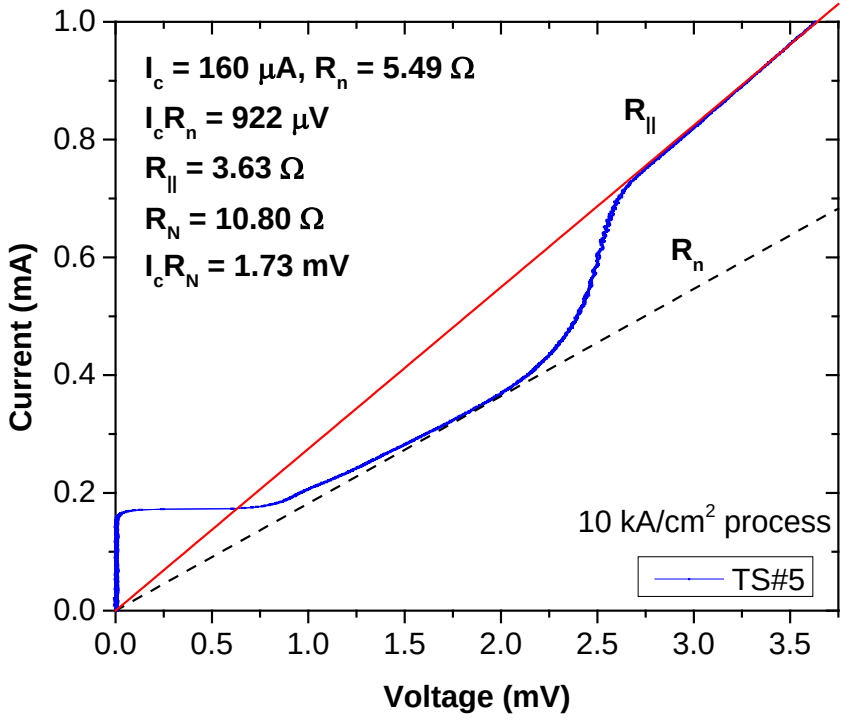


- **Dependence of JJ conductance spread (I_C spread) with JJ size down to 200 nm**
- **Characterized baseline 248 nm photolithography prior to transition to 193 nm**
- **Full runs for J_C and I_c spreads @ 100, 200 & 500 μA/μm² to characterize trilayer process**
- **Solid and dash lines – theory based on mask error enhancement, see our poster 2EPo1A-02 on Tuesday morning**

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

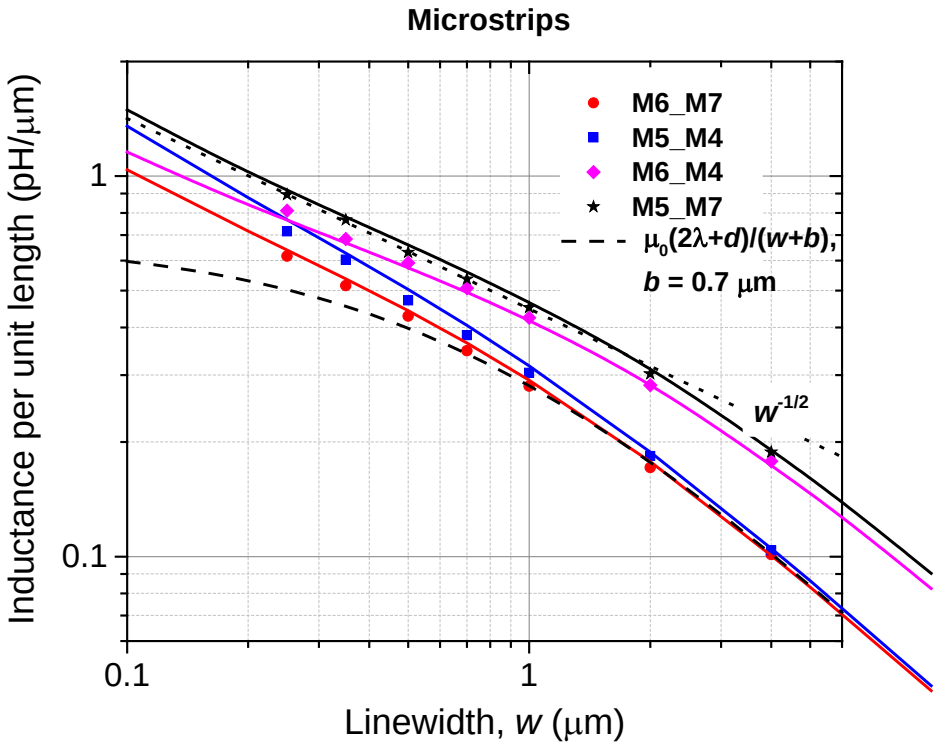
Shunted Junction Characteristics

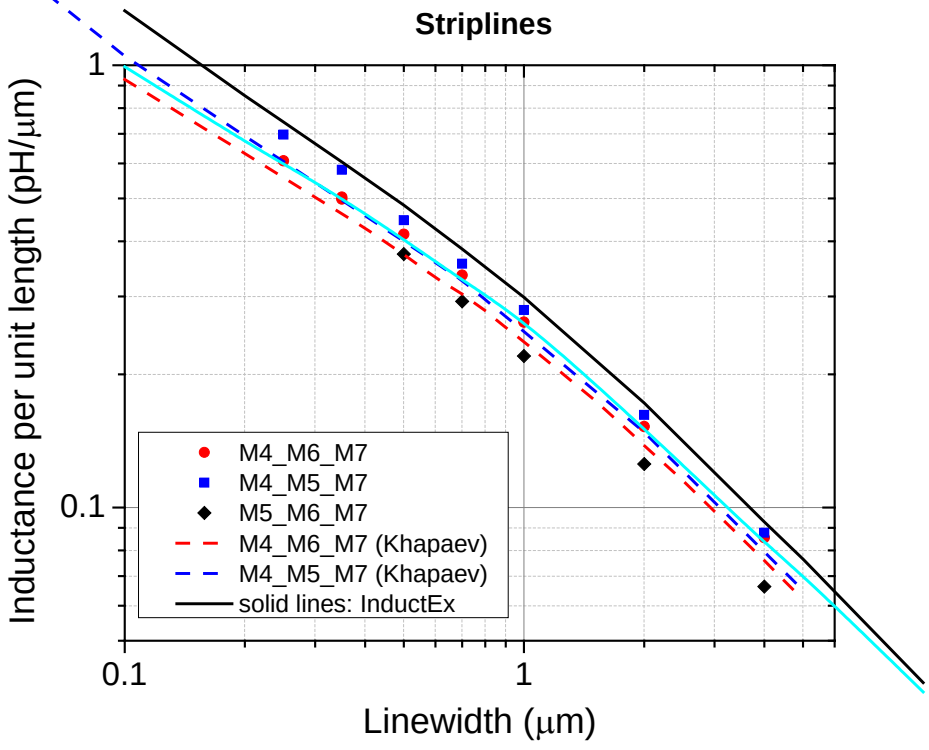




- **JJs are externally shunted for $\beta_c \sim 1$**
- **No hysteresis of I-V**
- **I_cR_n range 700 – 900 μV**
- **R_n: shunt resistance; R_N: JJ normal-state resistance**

Layer Inductances and Inductance Uniformity in SFQ4ee (8M) Process





- **Below ~ 1 μm, inductances increase as ~ $w^{-1/2}$ with line width decreasing**
- **Simulations using different software packages generally agree within a few percent**
- **Simulated inductances are very close to the experimental data, within a few percent**

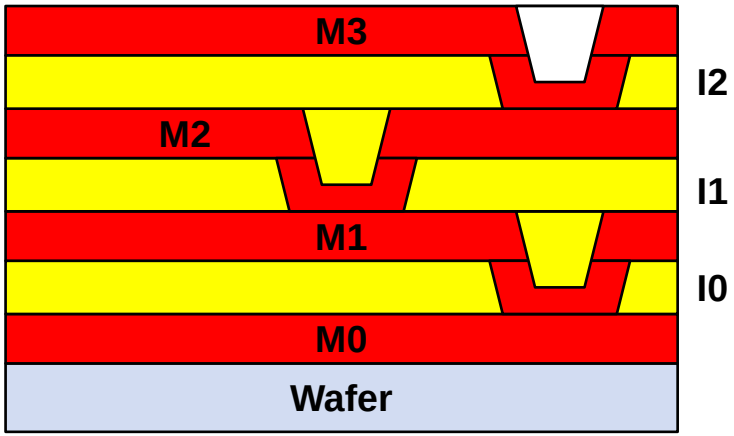
Inductance on-Wafer Uniformity

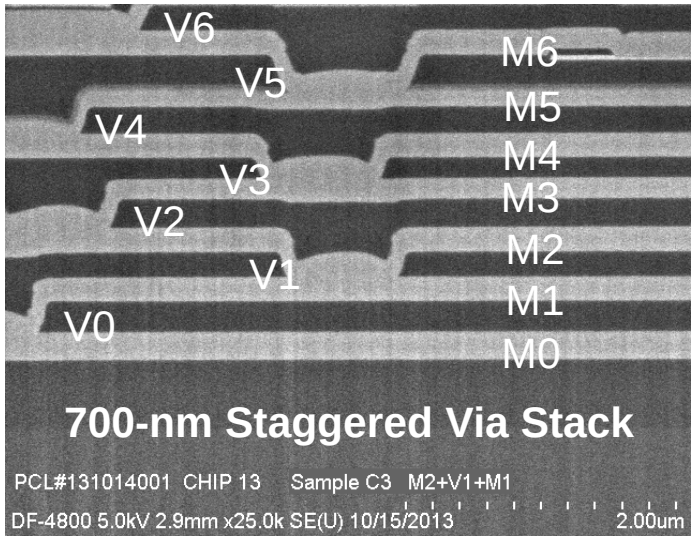
- **w = 0.5 μm, 1σ = 1.5%**
- **w = 1.0 μm, 1σ = 1.2%**
- **w = 2.0 μm, 1σ = 0.7%**
- **w = 4.0 μm, 1σ = 0.5%**

See our poster 2EPo1-03 on Tuesday morning

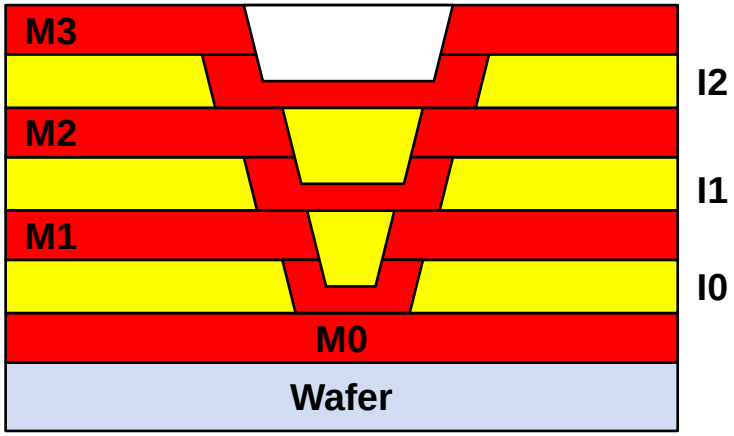
Stacked Vias vs Staggered Vias

Staggered I0_I1_I2 Via (from M0 to M3)



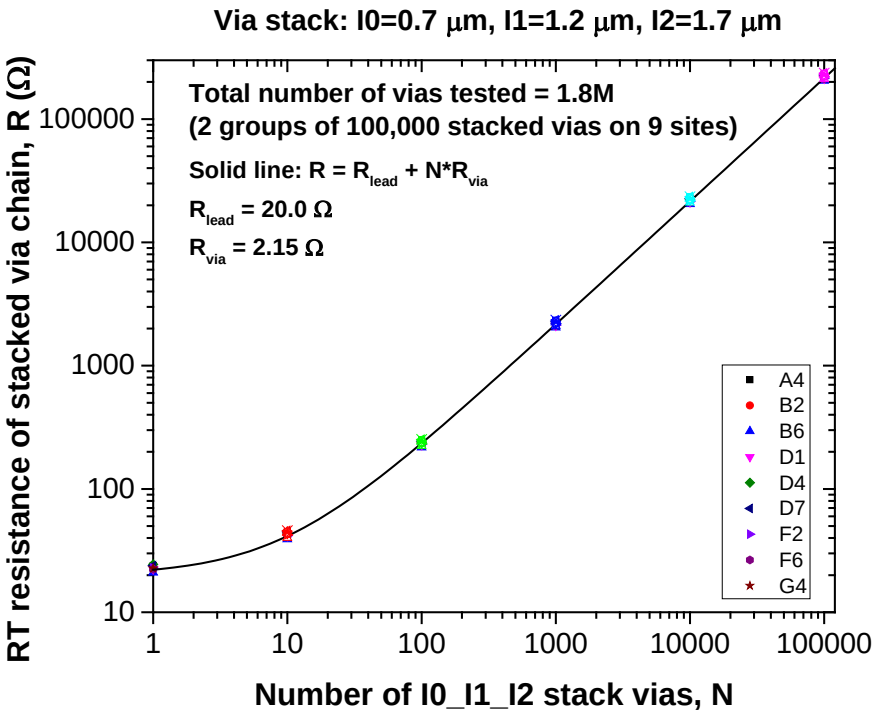


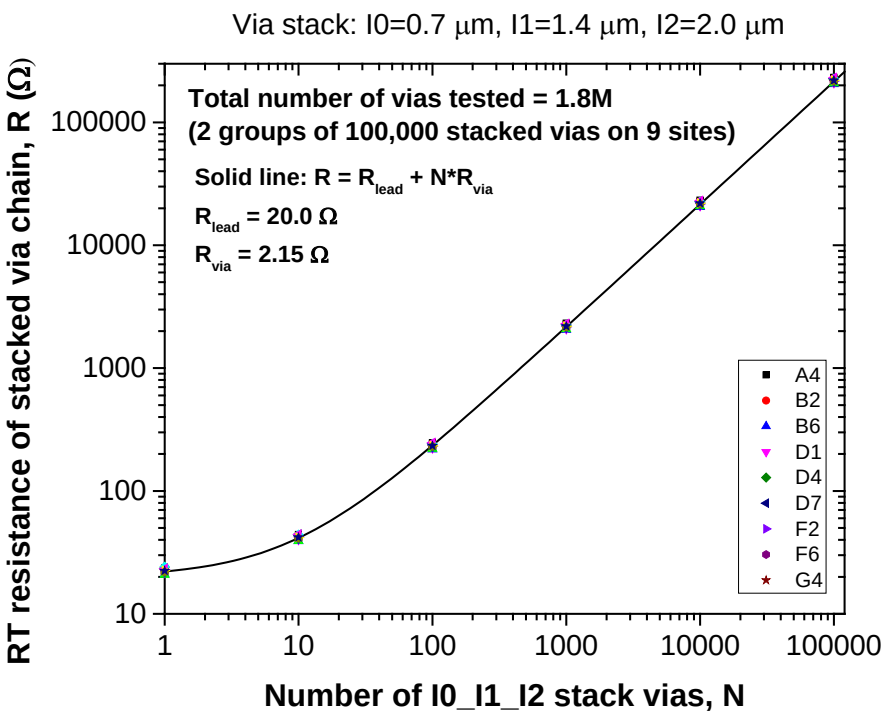
Stacked Via I0_I1_I2 (from M0 to M3)



- **Design rules for SFQ3ee (&4ee) currently require *staggered* vias**
- **Stacked vias may have smaller inductance, and possibly occupy less area in circuits**
- **Both have been tested on a 2M-via scale, using PCM300 via test structures**

Testing Stacked Vias





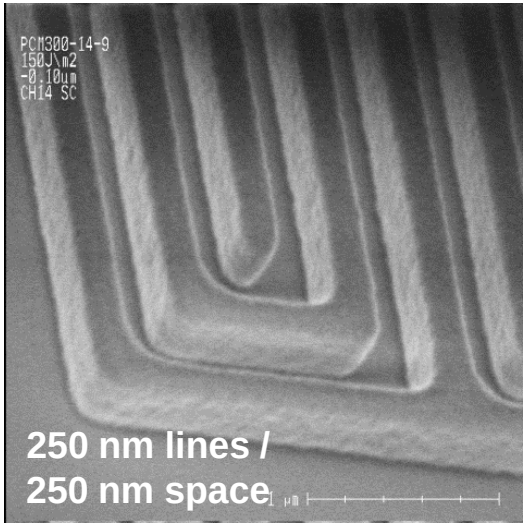
- **Stacked vias I0_I1_I2 (from M0 to M3 layers) with 400k vias per chip were fabricated and tested at RT**
  - **Excellent yield and reproducibility across the wafers were found**
- **I_c measurement at 4.2 K have shown that all 1.8M stacked vias are superconducting with I_c ~ 35 mA. This is an excellent result!**

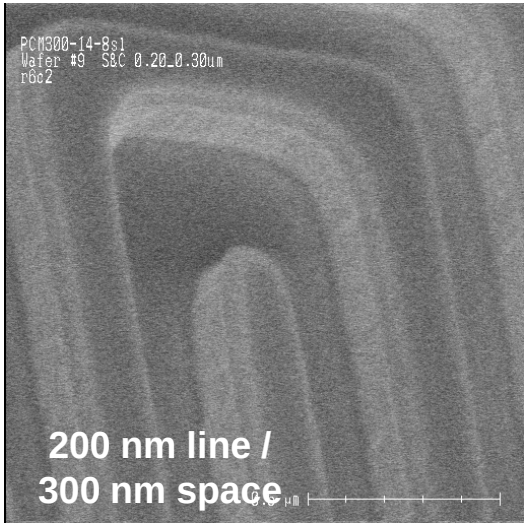
Outline

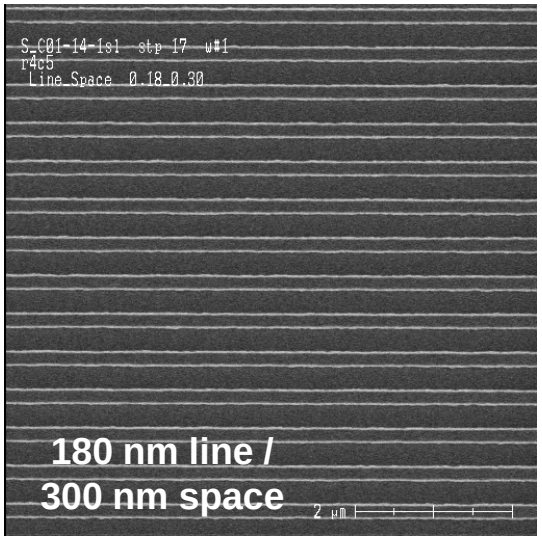
- **SFQ Process Overview**
  - **SFQ fabrication process nodes**
  - **General process description (4M, 8M, and 10M)**
  - **Multi-chip module process**
- **SFQ fabrication process highlights**
  - **Process Control Monitors and test examples**
  - **Junction properties and sizing, inductors, vias**
  - **SFQ5ee and beyond: shrinking feature size to 180 nm, stud vias**

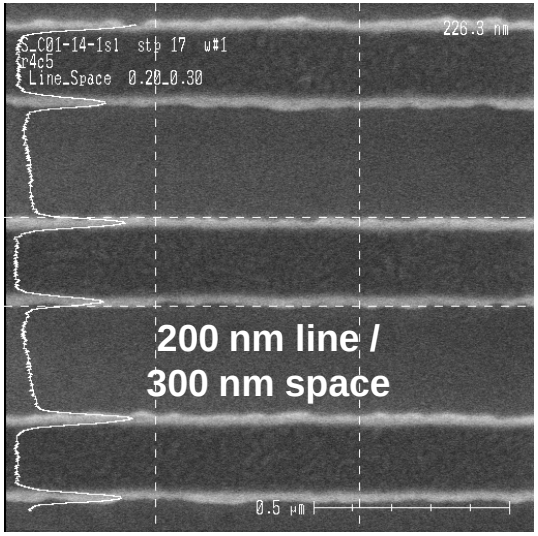
  - **See also our poster presentations 2EPo1A-02 and 2EPo1A-03 on Tuesday morning for more info on JJs, inductances, etc.**

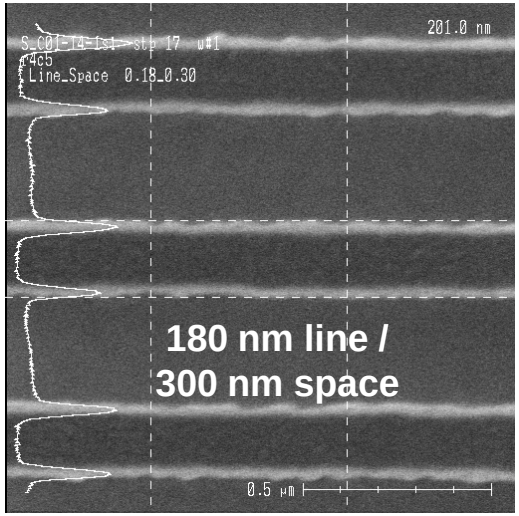
Etched Nb Lines for Advanced Nodes

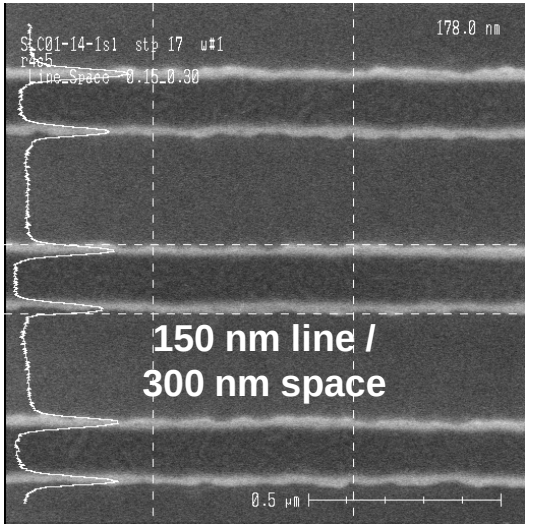






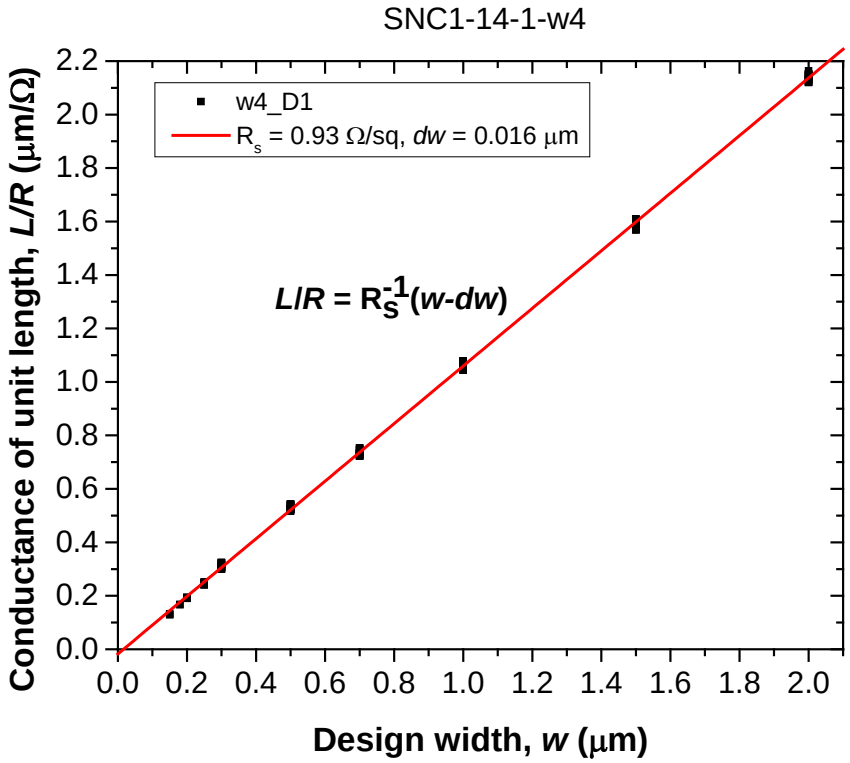


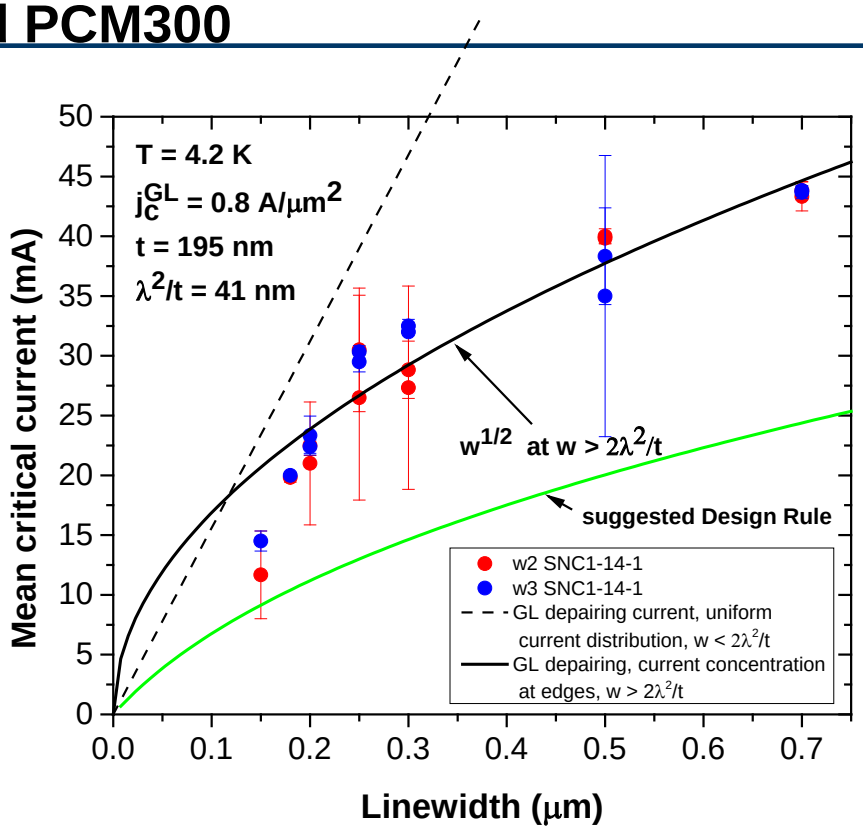




Min pitch, $p = w + s$, is 420 nm for our 248-nm photolithography

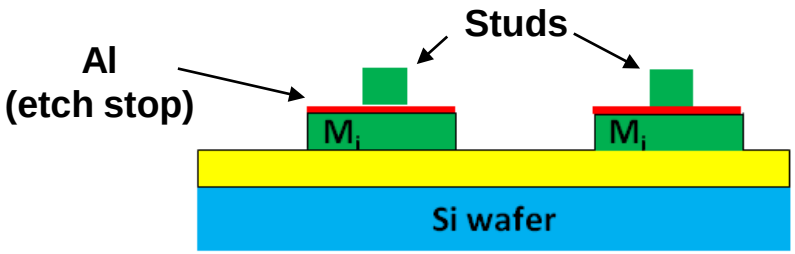
Critical Current of Narrow Nb Lines SNC1 and PCM300



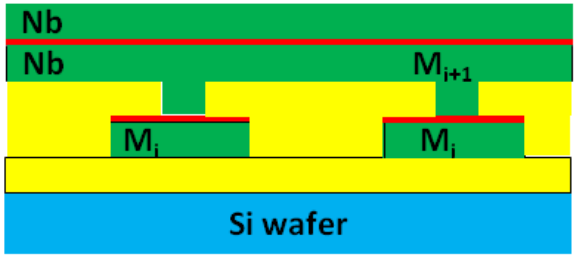


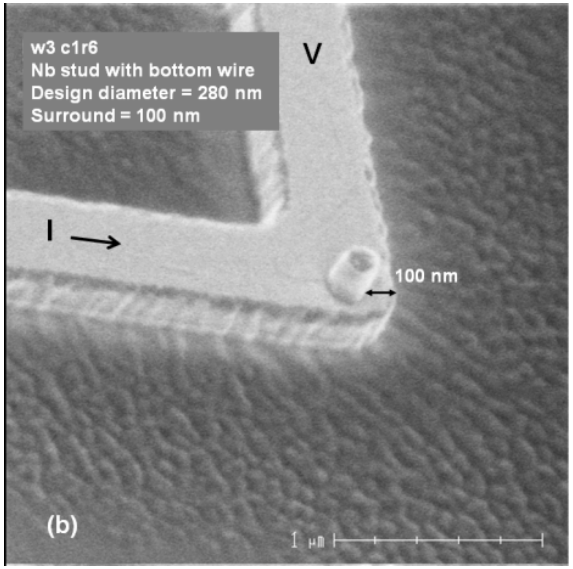
- **Nb lines with length L ~ 1 m - 2 m and different widths, *w*, down to 0.15 μm were fabricated. Six test structures of the same type (width and length) per chip**
- **Critical currents of Nb lines were found to be close to the theoretical limit – Ginzburg-Landau depairing current for wide films $w > \lambda^2/t$, where λ is magnetic field penetration depth, *t* is film thickness**
- **Allows setting the Design Rule for the future process nodes up to 7ee (0.18 μm)**

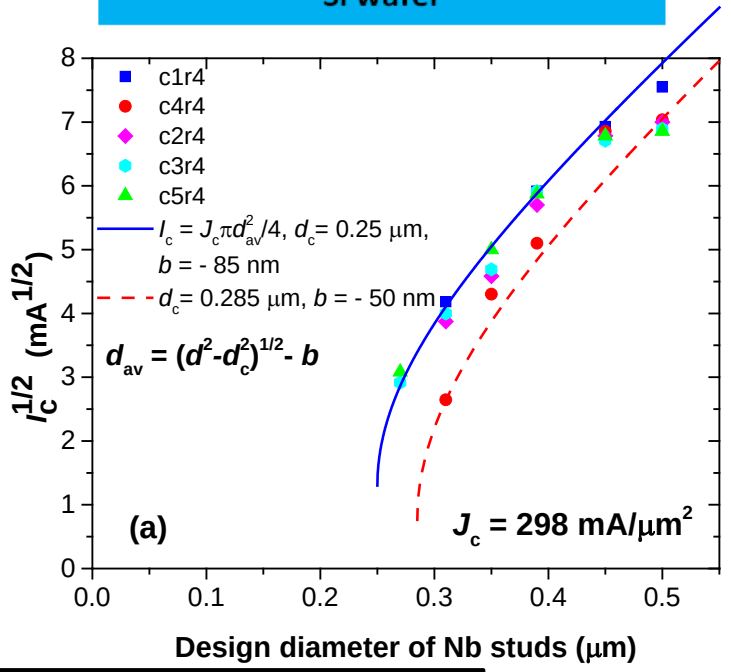
SFQ5ee Stud Via Development



Double Etch and Planarization Process



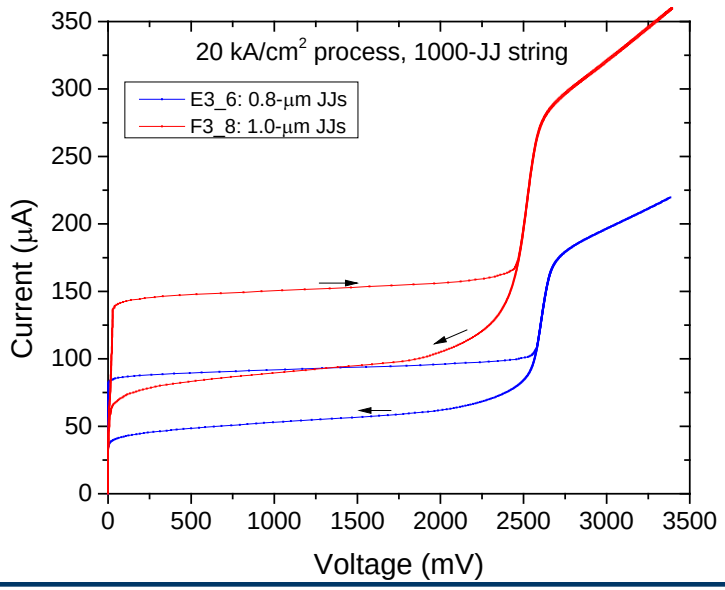


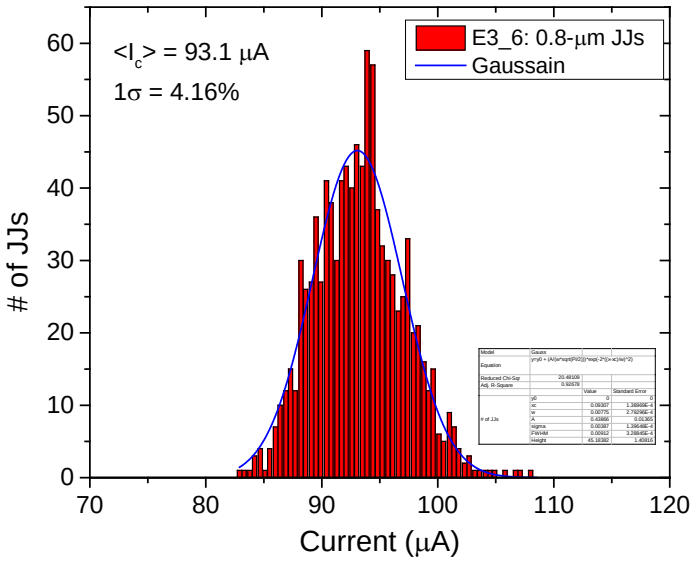


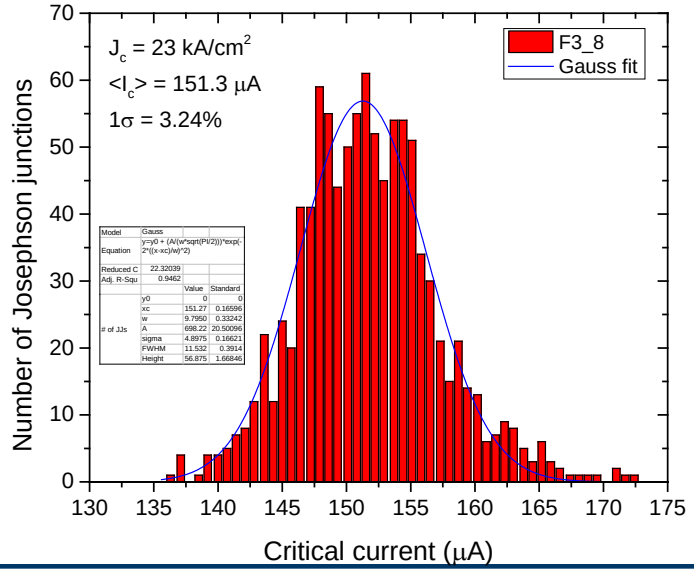
Demonstrated >5 mA I_c's for 300-nm stud vias, meeting SFQ5ee requirement

Higher J_c Junctions: 20-kA/cm^2

- J_c = 20 kA/cm^2 (200 μA/μm^2) process
  - JJs sizes: 0.7 μm to 1.6 μm
  - I_c range: 77 μA to 400 μA
- I_c spreads (1σ) nearly match 10 kA/cm^2 process

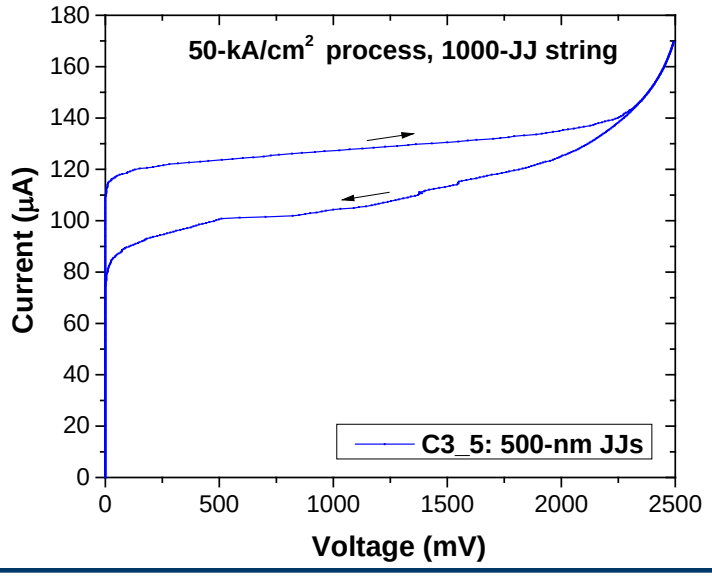


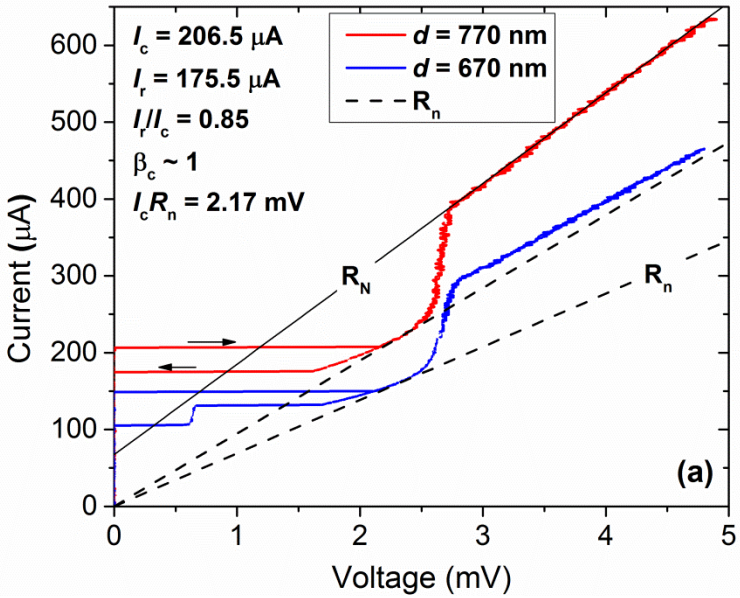


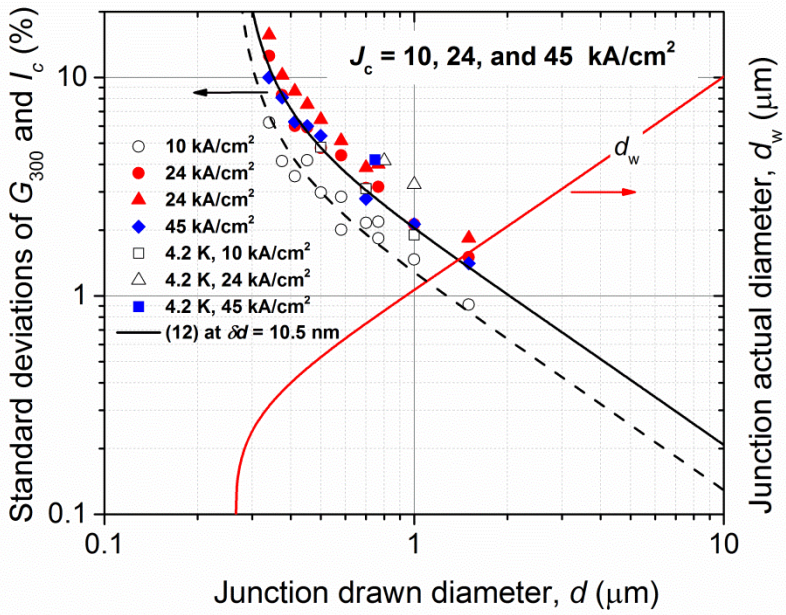


Higher J_c Junctions: 50-kA/cm²

- J_c = 50 kA/cm² (500 μA/μm²)
  - Self-shunted junctions
  - $\beta_c \sim 1$
  - JJs sizes: 0.5 μm to 1.2 μm
  - I_c range: 90 μA to 500 μA
- I_c spreads (1σ) nearly match 10 kA/cm² process
- $I_cR_n \sim 2.2$ mV!
- V_g = 2.65 mV – no excess heating!







Conclusion

- **We have developed a fully planarized 8-Nb layer fabrication process (SFQ4ee) for superconductor electronics on a tool set typical for a CMOS foundry with 248-nm photolithography**
- **The process and its truncated 4-Nb layer version (SFQ3ee) are high yielding processes based on extensive PCM measurements and high yield of operational circuits with tens of thousands of JJs**
- **We have demonstrated high uniformity and reproducibility of JJ with sizes down to 500 nm and below, sufficiently high to enable VLSI superconducting circuits with over 10^6 JJ/cm^2 at 10 kA/cm^2, 20 kA/cm^2, and 50 kA/cm^2 current densities**
- **We have developed a fully planarized process for stacked stud-vias with 300 nm diameter for replacing etched vias**
- **We have demonstrated high-critical-current superconducting Nb lines with linewidth to down to 150 nm at 450 nm pitch**
- **We are proceeding along our roadmap toward a 10-Nb layer fully planarized process with 180 nm linewidth at 380 nm pitch.**

Thank you very much for your attention

Questions?