IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), September 2019.
Contributed presentation 2-ME-C-1 given at ISEC, 28 July-1 August 2019, Riverside, USA.

Optical pulse-drive and on-chip power splitter for the pulse-driven AC Josephson voltage standard

(Josephson Arbitrary Waveform Synthesizer : JAWS)

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4: National Physical Laboratory NPL, Teddington, United Kingdom

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Outline

1. JAWS basics

2. JAWS at PTB : status quo

3. 5-stacked Josephson junctions arrays

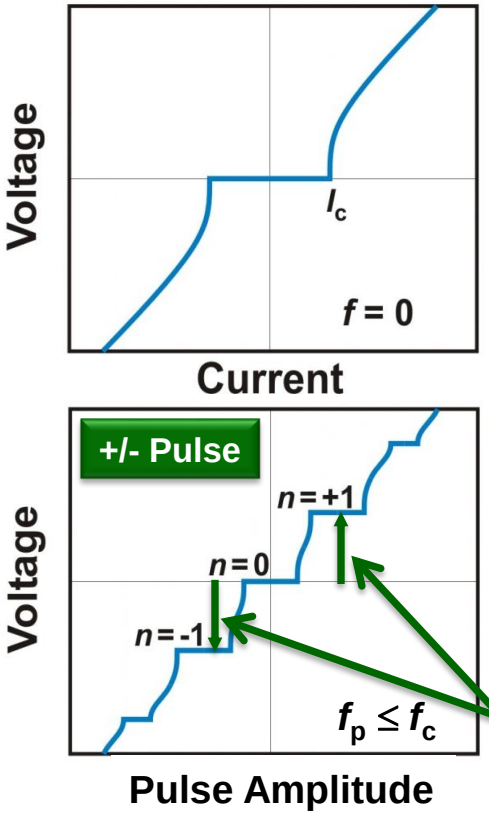
4. optical pulse-drive

5. on-chip power splitter

JAWS : basics (I)

SNS junctions : non-hysteretic IVC

S: Superconductor / N: normal metal



Shapiro-step : selected by pulse amplitude

f_{clock} = 15 GHz
RTZ pulses (30 Gbit/s)

a current pulse (pulse repetition frequency f_p)
transfers N flux-quanta $\Phi_0 = h/2e$
through M Josephson junctions.

signal voltage

Josephson equation in pulse-mode operation :

$$V_{signal}(t) = M \cdot N \cdot \Phi_0 \cdot f_p(t)$$

(Shapiro steps for $f_p \leq f_c$)

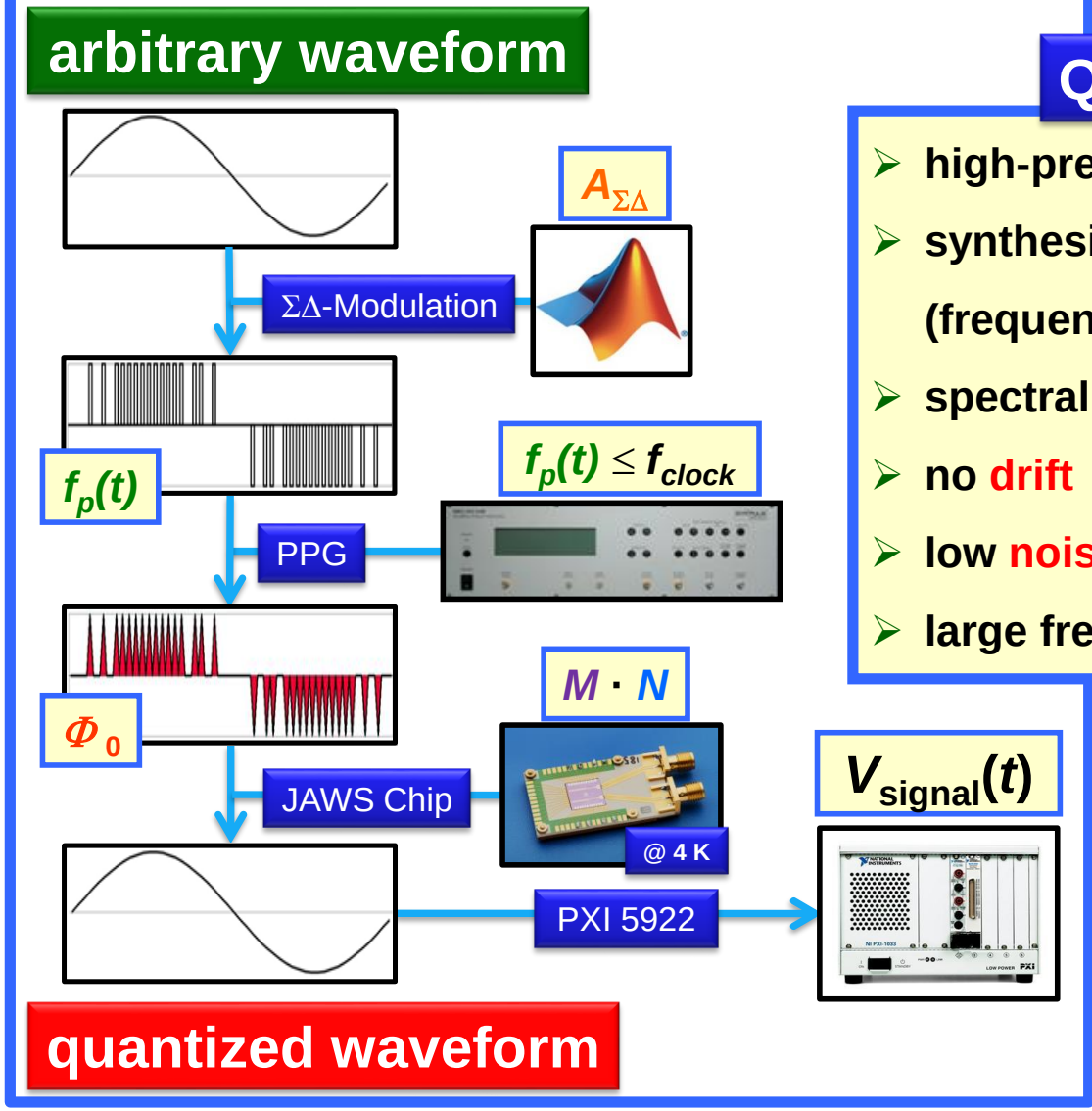
signal frequency

$$f_{signal} = T_{\Sigma\Delta} \cdot f_{clock} / L_{\Sigma\Delta}$$

$A_{\Sigma\Delta}$: code amplitude
$T_{\Sigma\Delta}$: number of periods
$L_{\Sigma\Delta}$: code length
$\Phi_0 \approx 2$ µV/GHz

JAWS principle : S.P. Benz and C.A. Hamilton, *APL* 68 (1996) 3171

JAWS : basics (II)

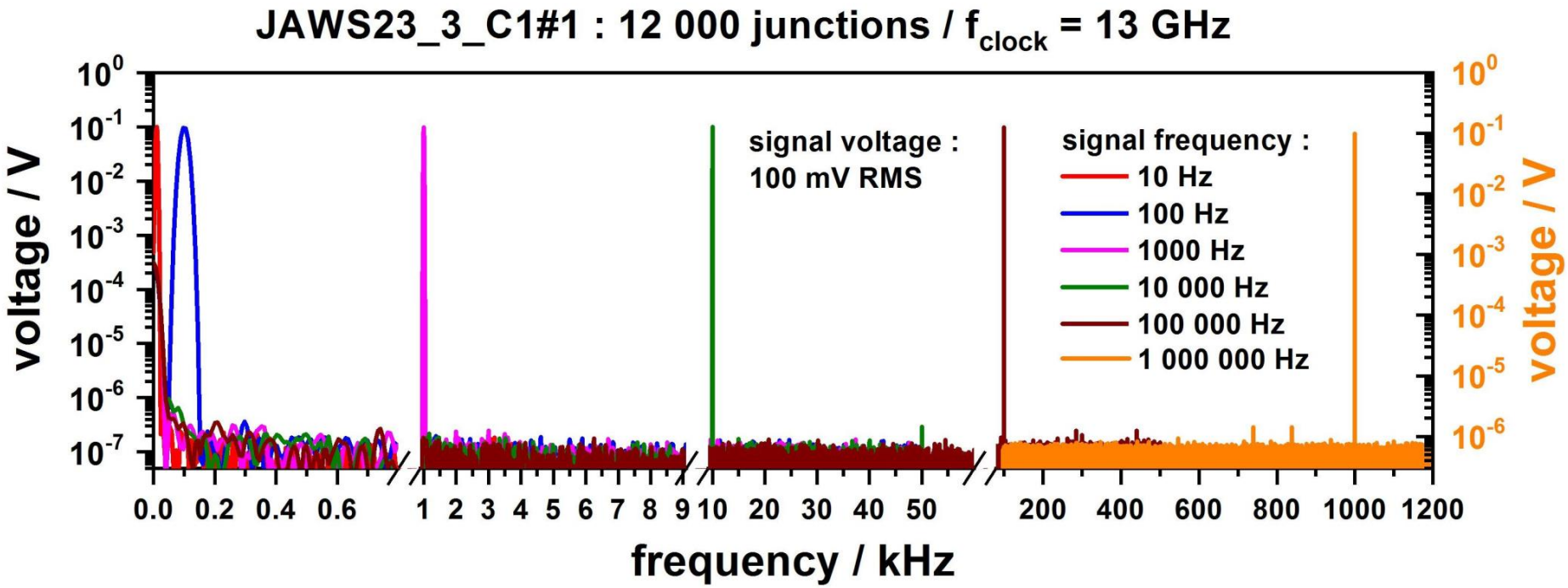


Quantum - Standard

- high-precision quantized AC voltage source
- synthesis of arbitrary waveforms (frequency or time domain)
- spectrally pure waveforms (SNR > 130 dBc)
- no drift
- low noise
- large frequency bandwidth (DC … MHz)

bandwidth / arbitrary / precision

large frequency bandwidth : 1 Hz…1 MHz

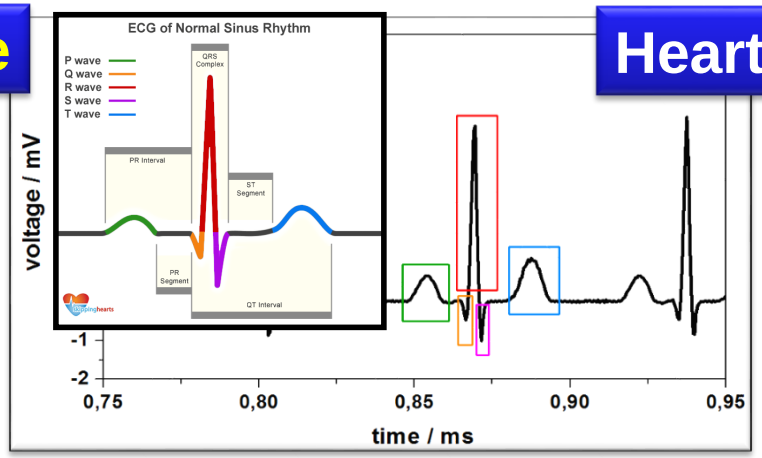


waveform : sinus
amplitude : 100 mV RMS

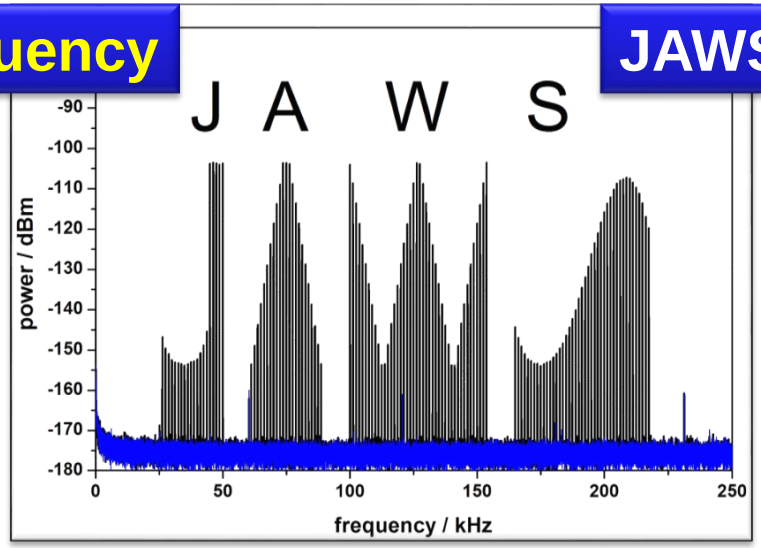
bandwidth / arbitrary / precision

arbitrary frequency and time domain

time — **Heartbeat**



frequency — **JAWS**



Quantum precision

1 V RMS comparison:

$V_{JAWS} - V_{QVM} =$

(+3.5 ± 12) nV @ 250 Hz

Behr et al., *Metrologia* 2015

Highlight paper of *Metrologia* in 2015 !

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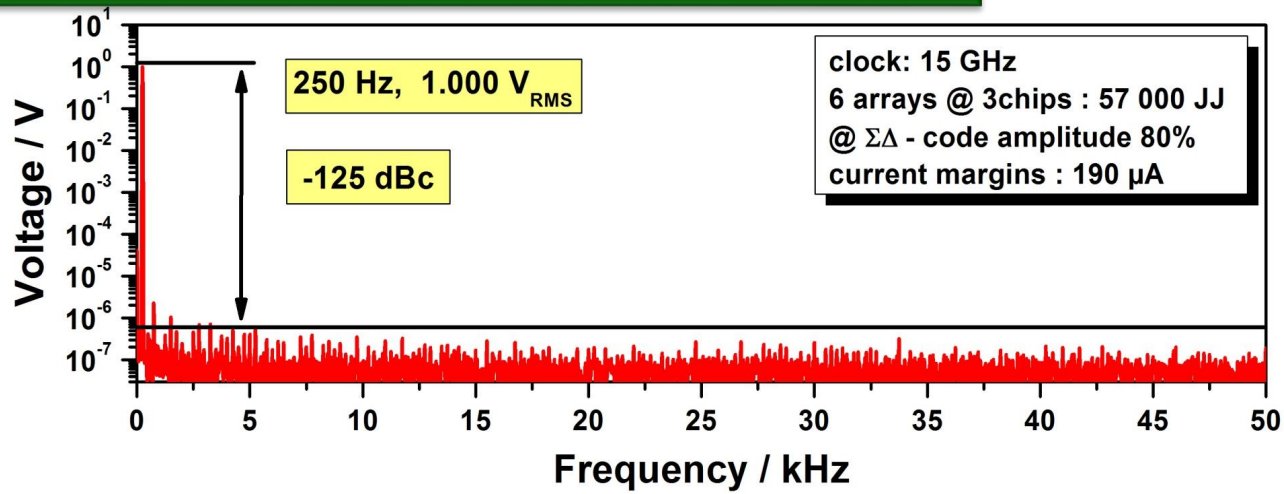
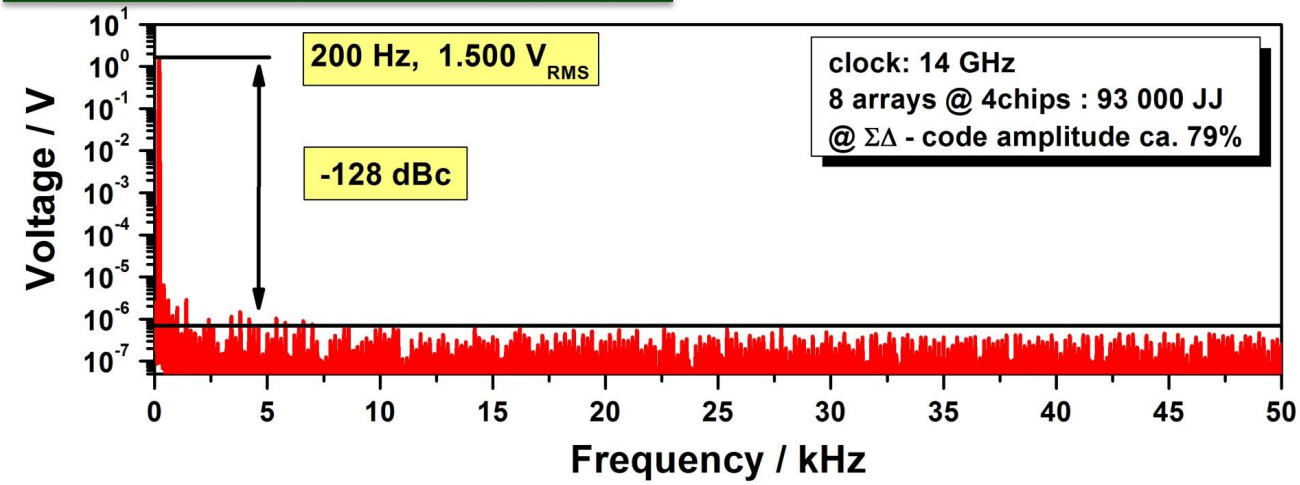
Recently : higher integration density

57 000 junctions @ 3 chips (instead of 4)



93 000 junctions @ 4 chips

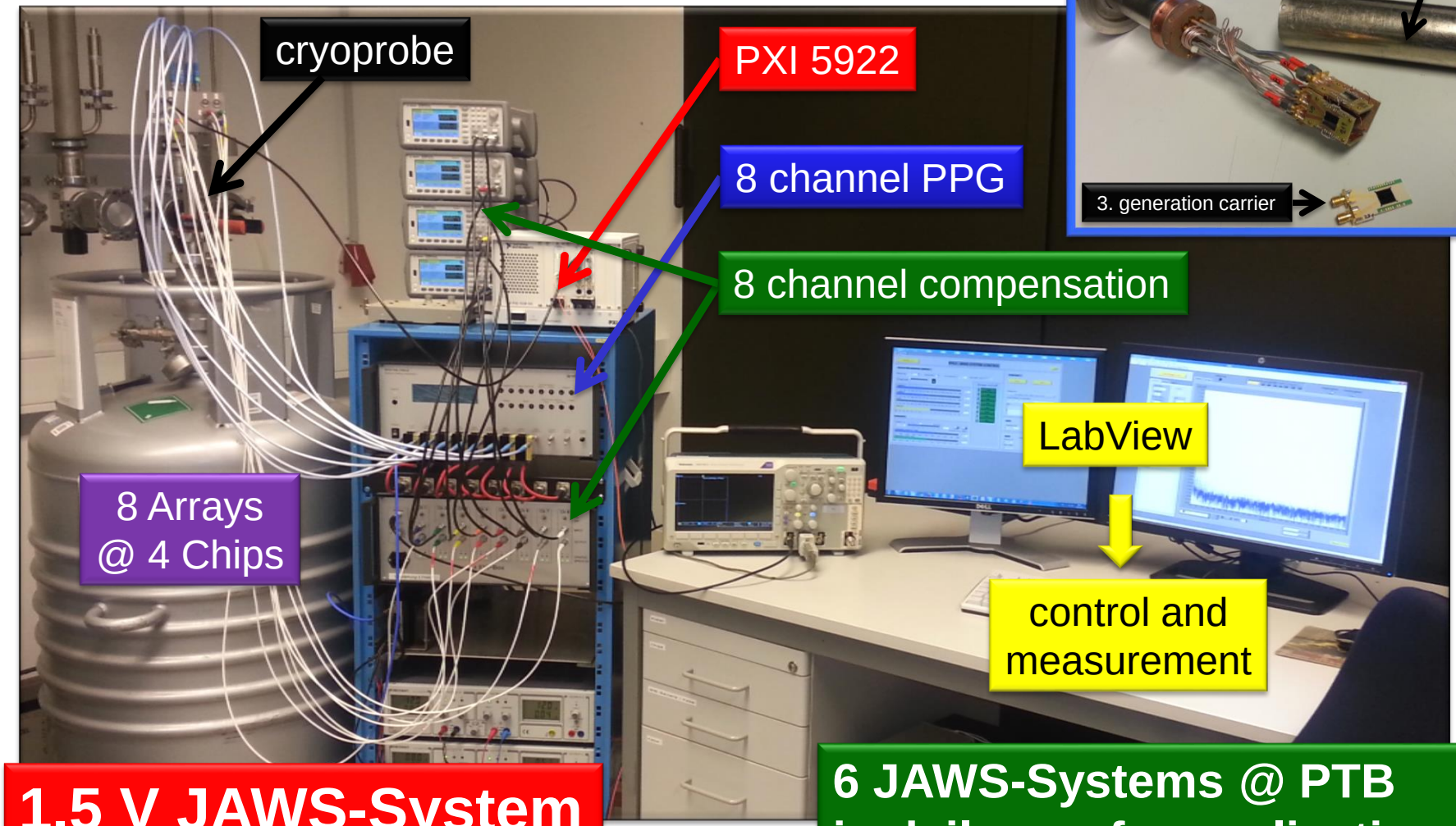


1 V RMS

established (high yield) :
- 4-stacked junctions
- 24 000 junctions / chip

1.5 V RMS

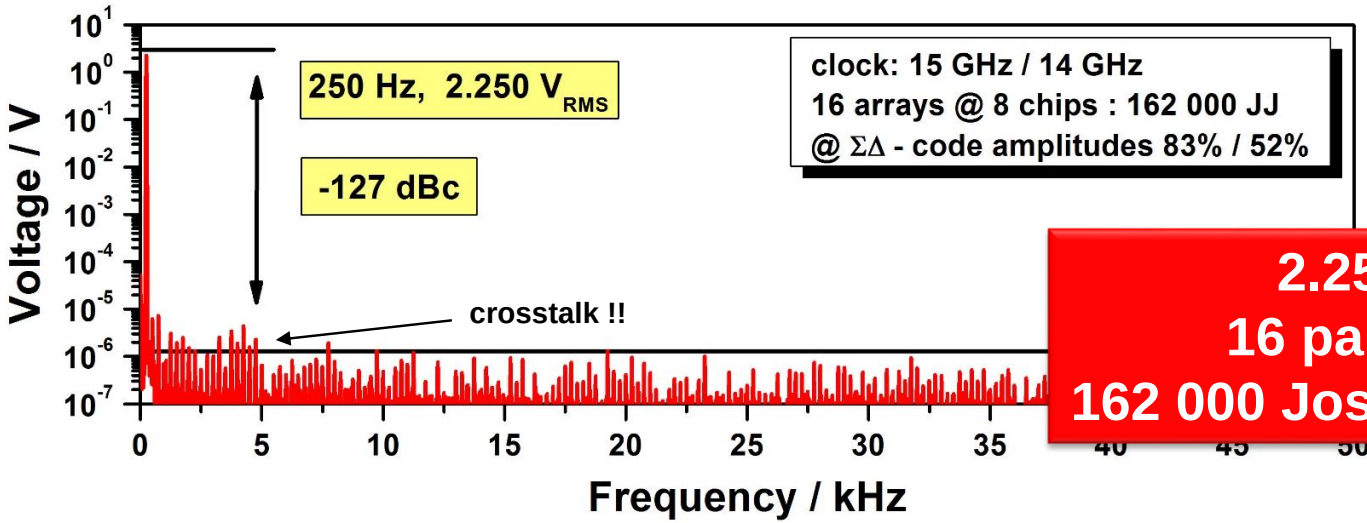
1.5 V JAWS-System : 93 000 junctions



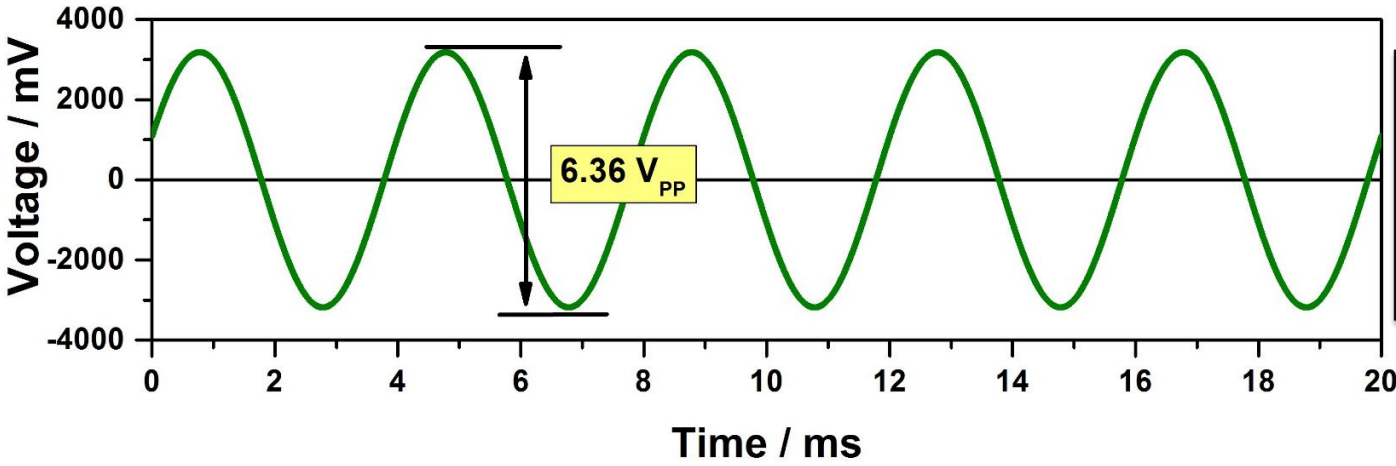
1.5 V JAWS-System

6 JAWS-Systems @ PTB in daily use for applications

2017 : 2.25 V RMS demonstrated



2.25 V RMS :
16 parallel arrays
162 000 Josephson junctions



NIST @ CPEM 2018 :
4 V RMS
16 parallel arrays
204 960 junctions
(4 HF channels)

2.25 V RMS →
ca. 1 088 000 000 000 000 Φ_0 per second

Kieler, et al., EUCAS 2017

Impact 2018 : JAWS applications

12 x CPEM 2018 - contributions with JAWS → coauthor

Conference on
Precision
Electrical
Measurement

most important
Metrology
conference

PTB	with external partners
1. Bauer	7. de Aguilar
2. Behr	8. Ireland
3. Herick	9. Lapuh
4. Kohlmann	10. Nissilä
5. Kraus	11. Sira
6. Palafox	12. Sosso

most measurements made @ PTB

ACQ XXXXXXXXX

QUADC

JNT - JAWS

6 other contributions (2xASC 2018, etc.)

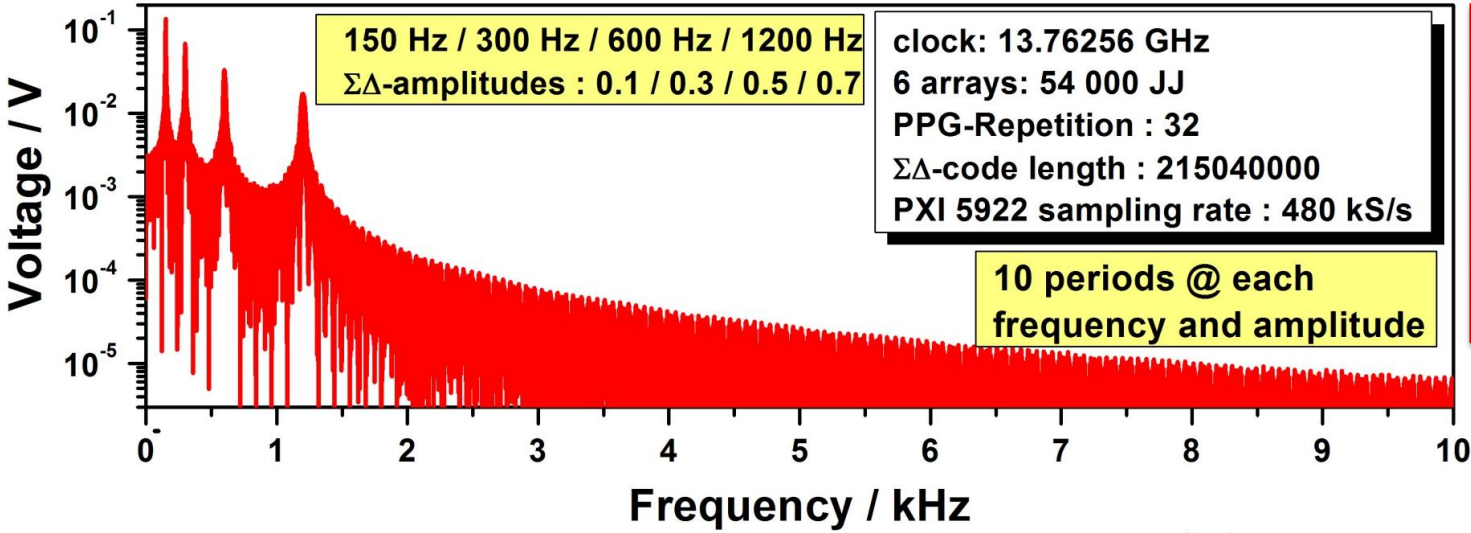
Examples of Activities (@ PTB)

1. 1 V JAWS : AC-DC transfer measurements with trans-conductance amplifier (NMIA)
2. 1 V JAWS : characterization of Keysight 3458A (SIQ, CEM)
3. AC-DC transfer (up to 1 MHz) with Fluke792A in mini-cryostat (VSL)
4. Characterization of ADC's (CMI)
5. Systematic error analysis (Tubitak)
6. Impedance/quadrature bridge (vs. AC-QHE, cryocooler)
7. JAWS based µV-Synthesizer (pV/junction)
8. JAWS with optical pulse-drive (NPL, JV, VTT)
9. JAWS JNT (with PTB Berlin)
10. JAWS in cryocooler (INRIM)
11. Characterization of Voltage Divider

EU projects:
EMRP „Q-WAVE"
EMPIR „ACQ-PRO"
EMPIR „QuADC"

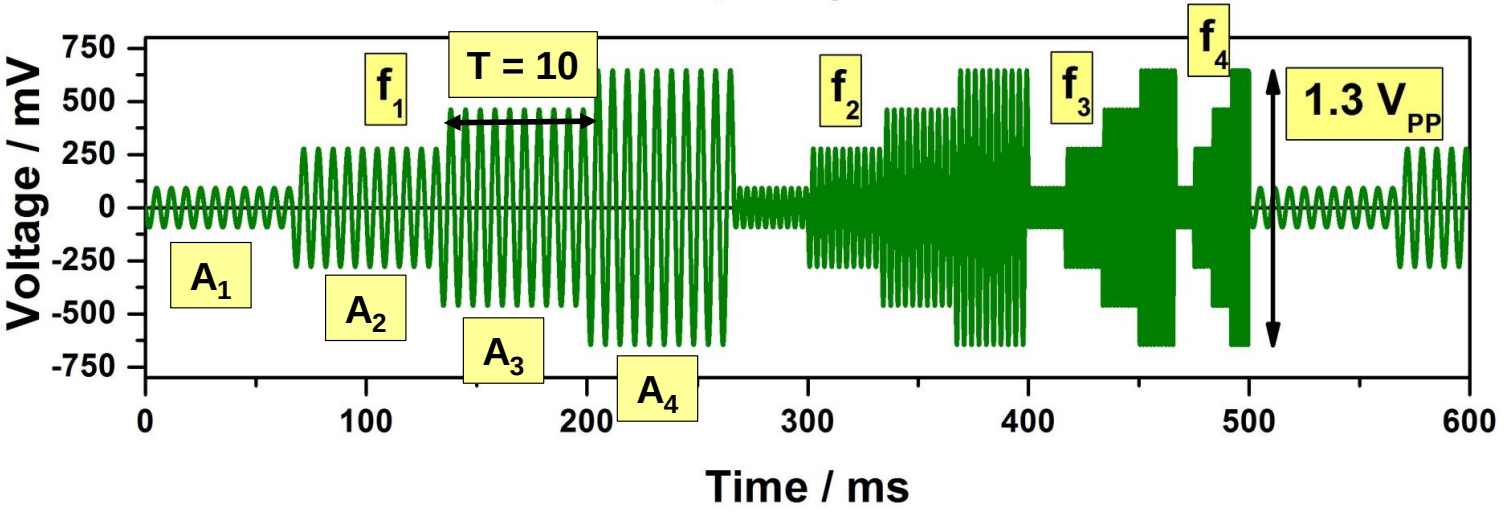
Application : characterization ADC (I)

"Martin Sira" 4x4x10-Waveform : 4 x f, 4 x A, 10 x T



special waveform :
- 4 frequencies
- 4 amplitudes
- 10 periods each

„simultaneously" analyzed :
- gain (amplitude)
- frequency response
- time stability



M. Sira et al. @ CPEM 2018

PTB JAWS Chips @ 8 countries

distributed within international research projects

JOSY

ACQ

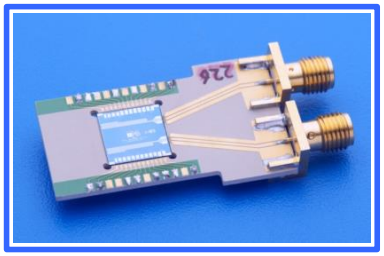
JAWS

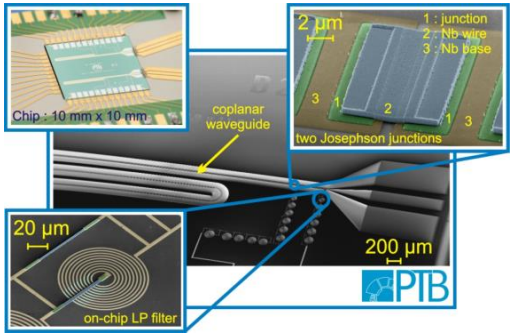
Q-WAE

QUADC

National Metrology Institutes

1. Netherland
2. United Kingdom
3. Norway
4. Italy
5. Finland
6. Turkey
7. Russia
8. China





Odyssey goes on…

…JAWS

AND BEYOND…

http://www.listal.com/viewimage/5873313

overview : recent projects / goals

JAWS with higher voltage : 7…10 V RMS

- more Josephson junctions @ chip
- less chips → less HF-channels @ 300 K
- less HF-crosstalk
- parallel-operation on-chip :
  - optical pulse → photodiodes @ 4.2 K
  - power-splitter on-chip @ 4.2 K

→ **JAWS system:**
- less complex
- less expensive
- more user-friendly

↓

AIST and NIST : pioneer work !

- Urano, et al., SUST, 2009

↓

few junctions, work stopped

- Flowers-Jacobs, et al., IEEE TAS, 2016
- Yamamori et al., IEEE TAS, 2016

UNIVEX 450C – Cluster - Sputter - System

PTB

SNS junctions : Nb_xSi_{1-x}

Nb_xSi_{1-x} parameter for
70 GHz and 15 GHz

6 chambers

fully automatic

2xNb, Si, AuPd,
HfTi, Al, Al_2O_3
rf-cleaning

SNS / SIS / SINIS

2 parameter to optimize :
JAWS : x ≈ 20%, d_{NbSi} ≈ 30 nm @ 15 GHz

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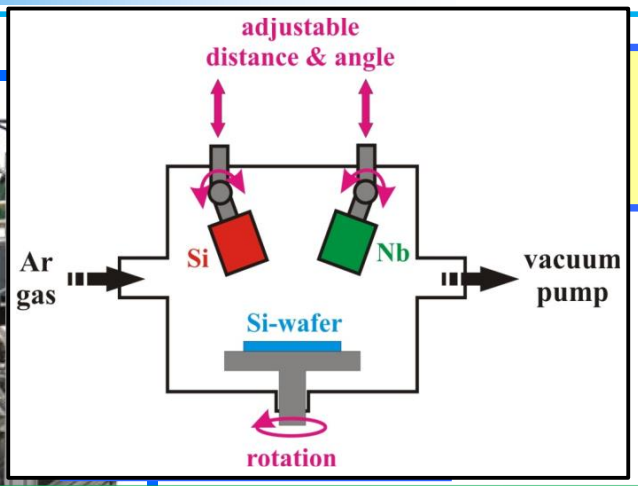
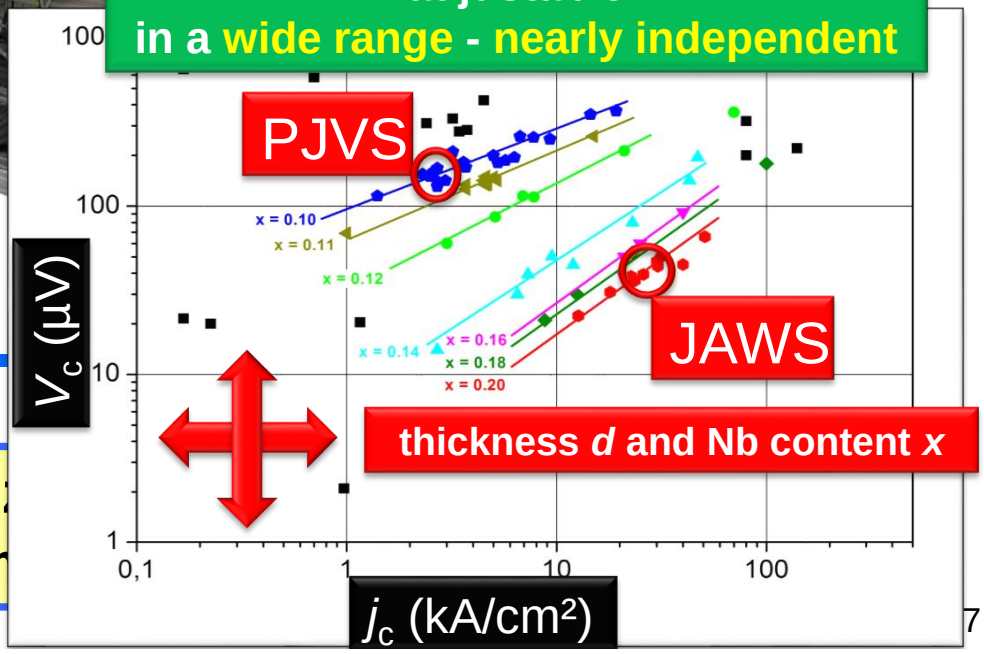
UNIVEX 450C – Cluster - Sputter - System

SNS junctions : Nb_xSi_{1-x}



adjustable
in a wide range - nearly independent



thickness *d* and Nb content *x*

2 parameter to optimi

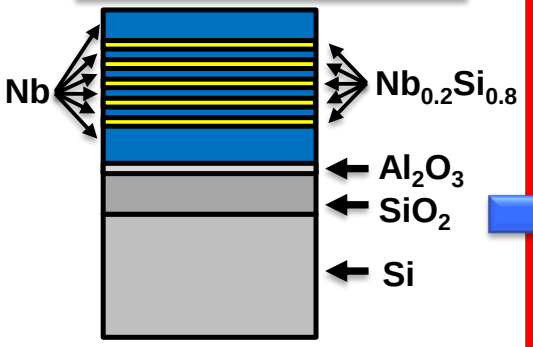
JAWS : x ≈ 20%, d_{NbSi} ≈ 30 nm

Technology: 5-stacked Jos. junctions

PTB

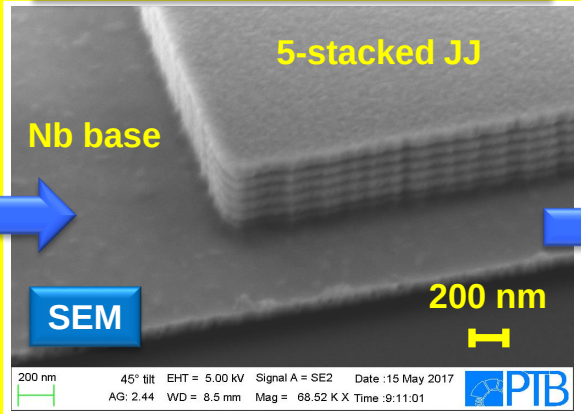
12 layer in-situ, 15 layer total → **stacks : „high“ integration density**

1) layer sequence

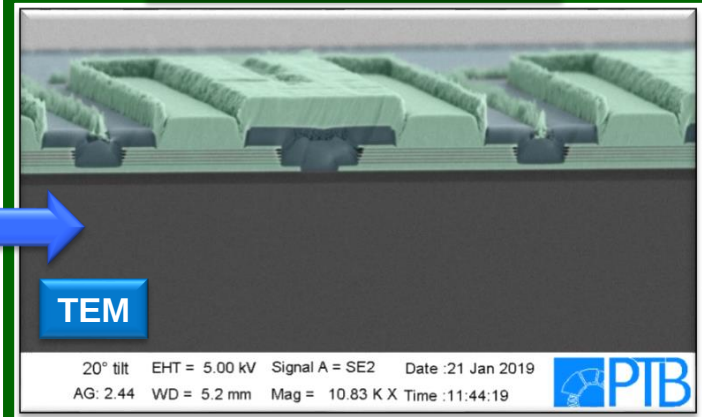


not shown : 1) Nb wire,
2) AuPd resistors, 3) SiO_2 isolation

2) after two fabrication steps



3) fabrication finished



JJ parameter :

- chain length : 3000…4000 JJ
- $Nb_{0.2}Si_{0.8}$: deposited by co-sputtering
- critical current density : $j_c \approx 5$ kA/cm²
- normal resistance : $R_n \approx 3$ mΩ
- characteristic voltage : $V_c \approx 10$ µV

modified fabrication of 5-stacked JJ :

- “window” process adjusted for stacks :
  - resist thickness
  - e-beam dose and proximity correction
  - development times
  - SiO_2 and Nb-Wiring layer thickness
  - implementation of CMP for SiO_2
- RIE-ICP : JJ stacks with steep edges
- PECVD : thick SiO_2 isolation layer
- window etch : in 2 steps !

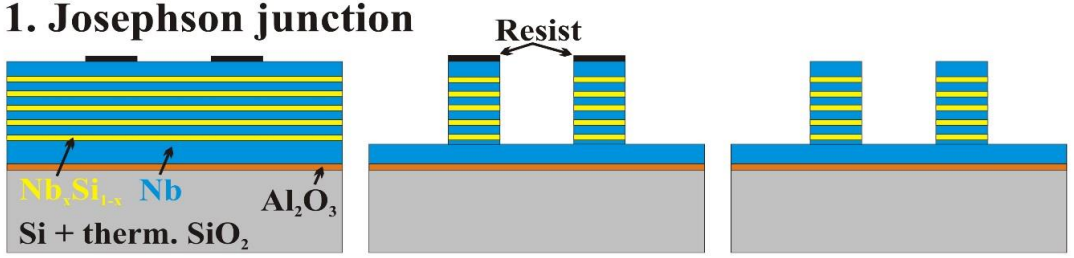
summary of process :

- 5 x deposition
- 7 x etching
- 7 x e-beam
- 1 x UV-lithography
- 1 x lift off
- 6 main fabrication steps
  → next slide

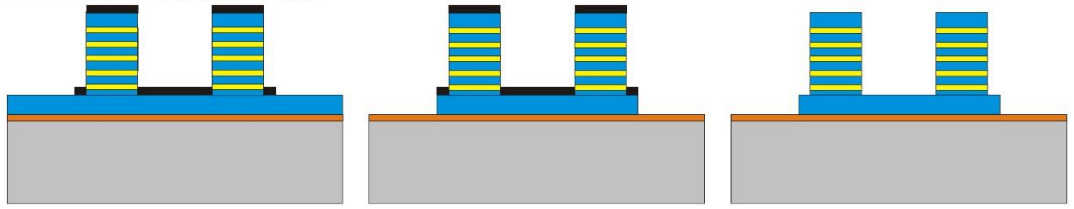
Technology : SNSNSNSNSNS

PTB

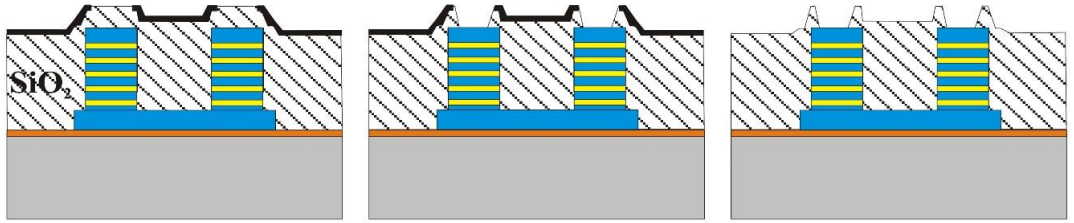
1. Josephson junction



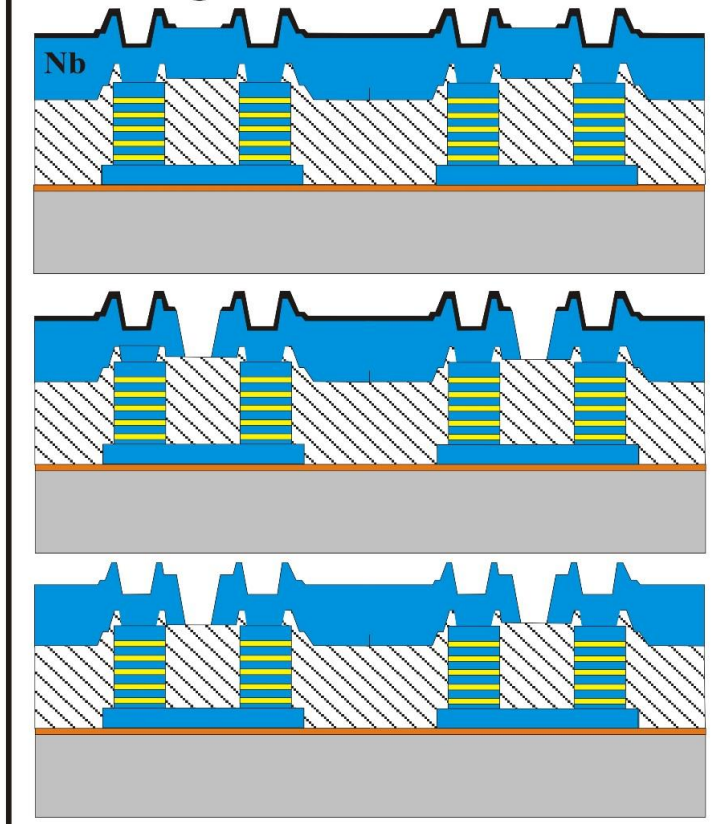
2. Base electrode



3. Isolation and window



4. Wiring electrode



5. Load : AuPd resistors by “lift-off”

6. Pads : SiO_2 by ICP-RIE

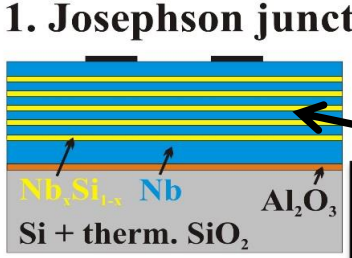
→ detailed process : ca. 40 fabrication steps
→ clean-room cycle-time 2 wafer : ca. 3 weeks

→ only for 5-stacked JJ : Improvement of yield !

Technology : SNSNSNSNSNS

PTB

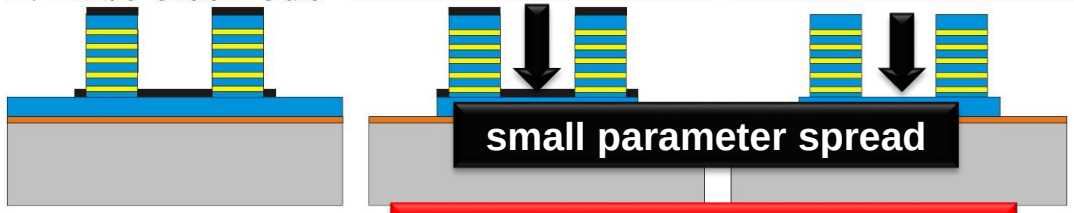
1. Josephson junction



homogeneous & reproducible !! (NbSi deposition)

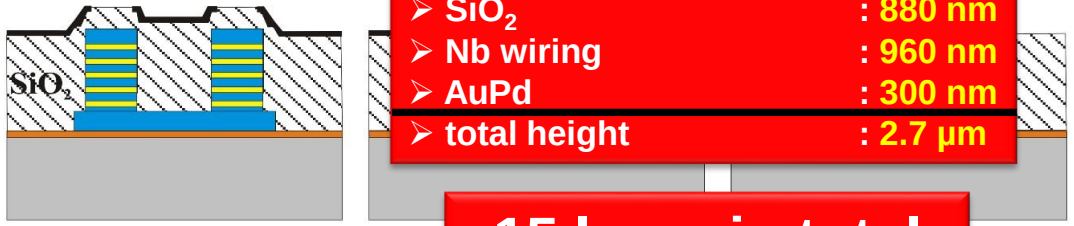
homogeneous & steep edges !! (ICP-RIE)

2. Base electrode



small parameter spread

3. Isolation and wir

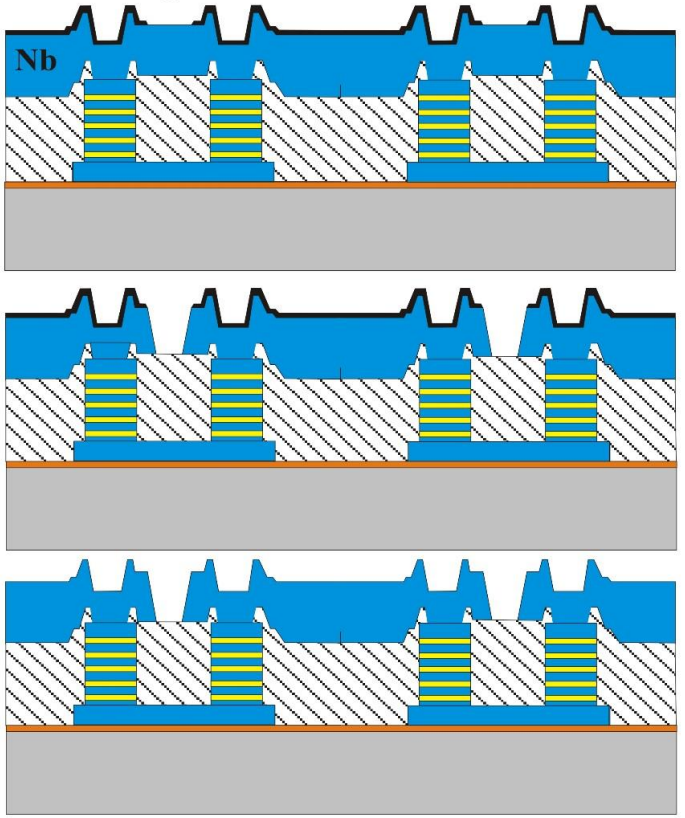


3D fabrication :

- junction multilayer : 780 nm
- SiO_2 : 880 nm
- Nb wiring : 960 nm
- AuPd : 300 nm
- total height : 2.7 µm

15 layer in total

4. Wiring electrode



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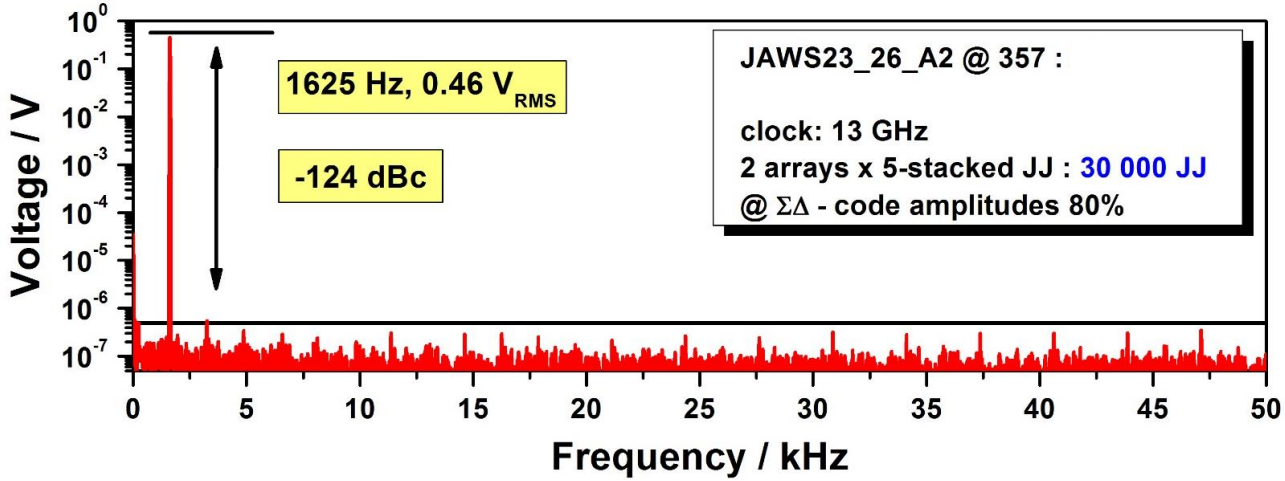
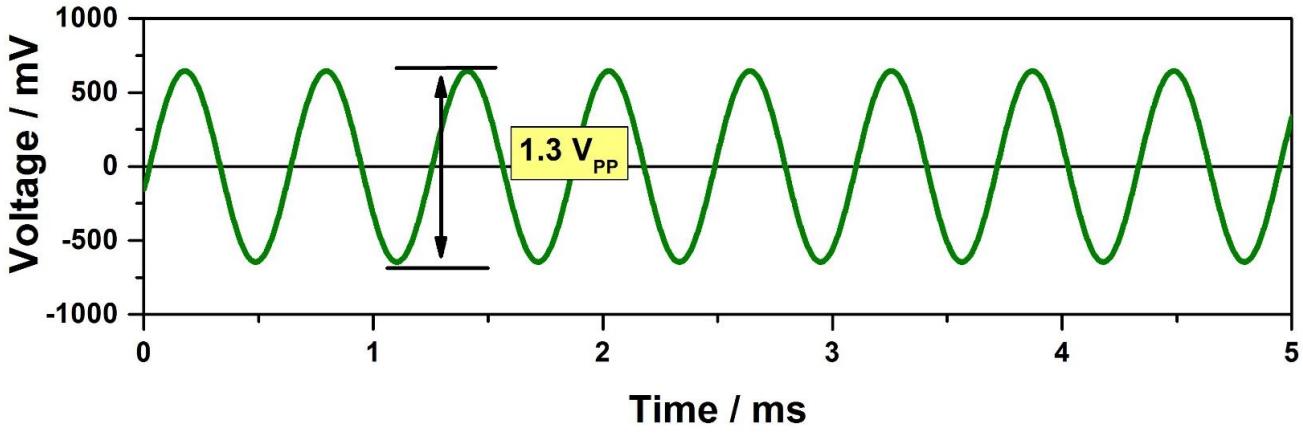
→ only for 5-stacked JJ : Improvement of yield !

5-stacked Josephson junctions

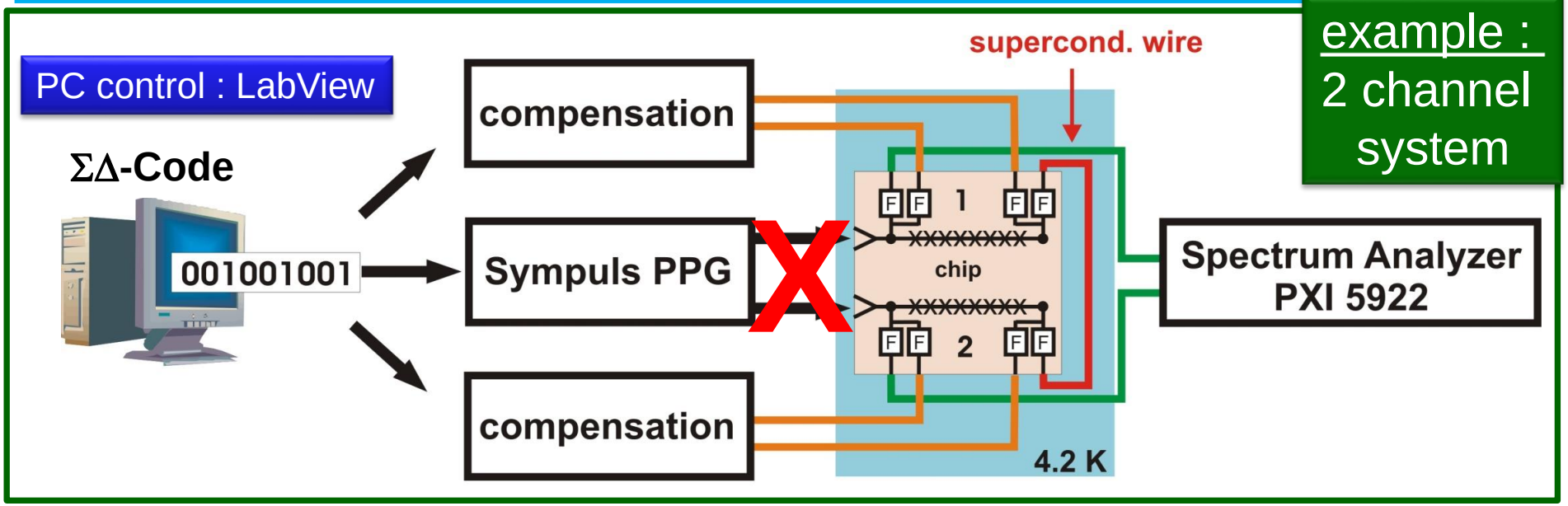
30 000 junctions per chip : ca. 0.5 V RMS / 1.3 V_{PP}





2 arrays @ 1 chips with 30 000 junctions

JAWS setup : electrical pulses

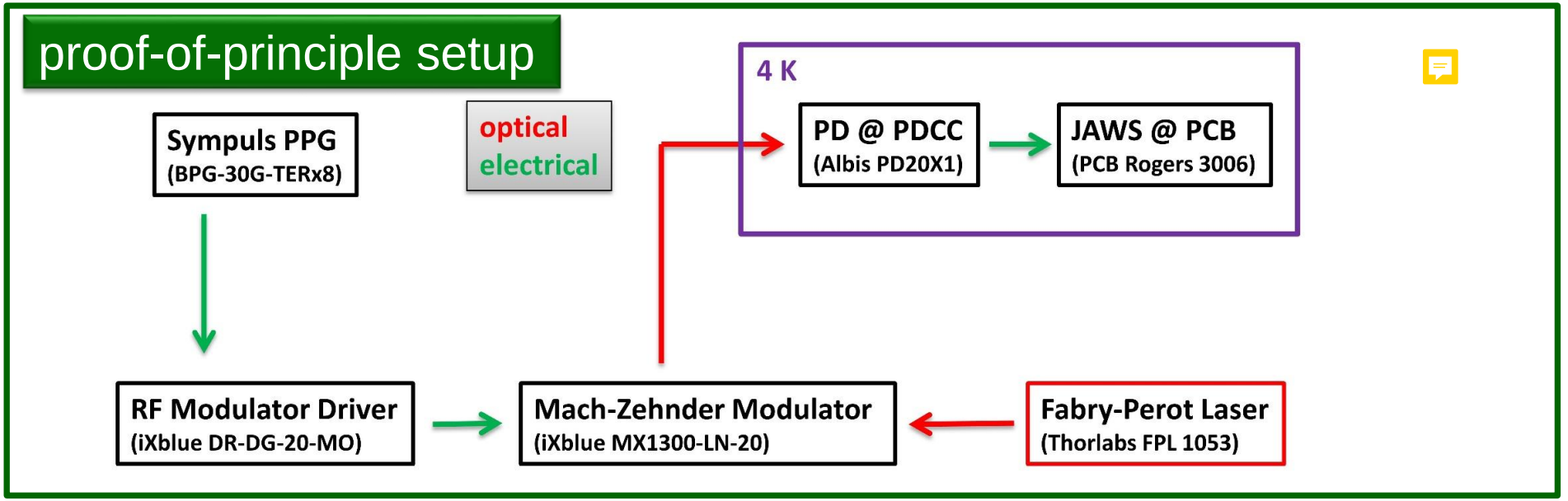


no electrical pulses anymore

- optical pulses : photodiodes @ 4.2 K “direct” (hybrid) on-chip
- use of optical fibers → less noise @ MHz-range
- easy parallel optical HF-channels → low cost solution

JAWS setup : optical pulses

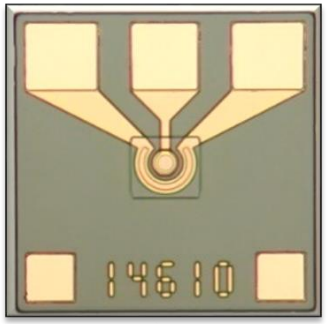
proof-of-principle setup



high-speed lensed photodiode (PD)

- PDCS24L (InGaAs/InP) chip with a tapered CPW
- integrated backside lens (bottom illuminated)
- up to 28 Gb/s, laser 1310 nm
- easy and efficient optical coupling
- pad layout allowing flip-chip mounting

ALBIS



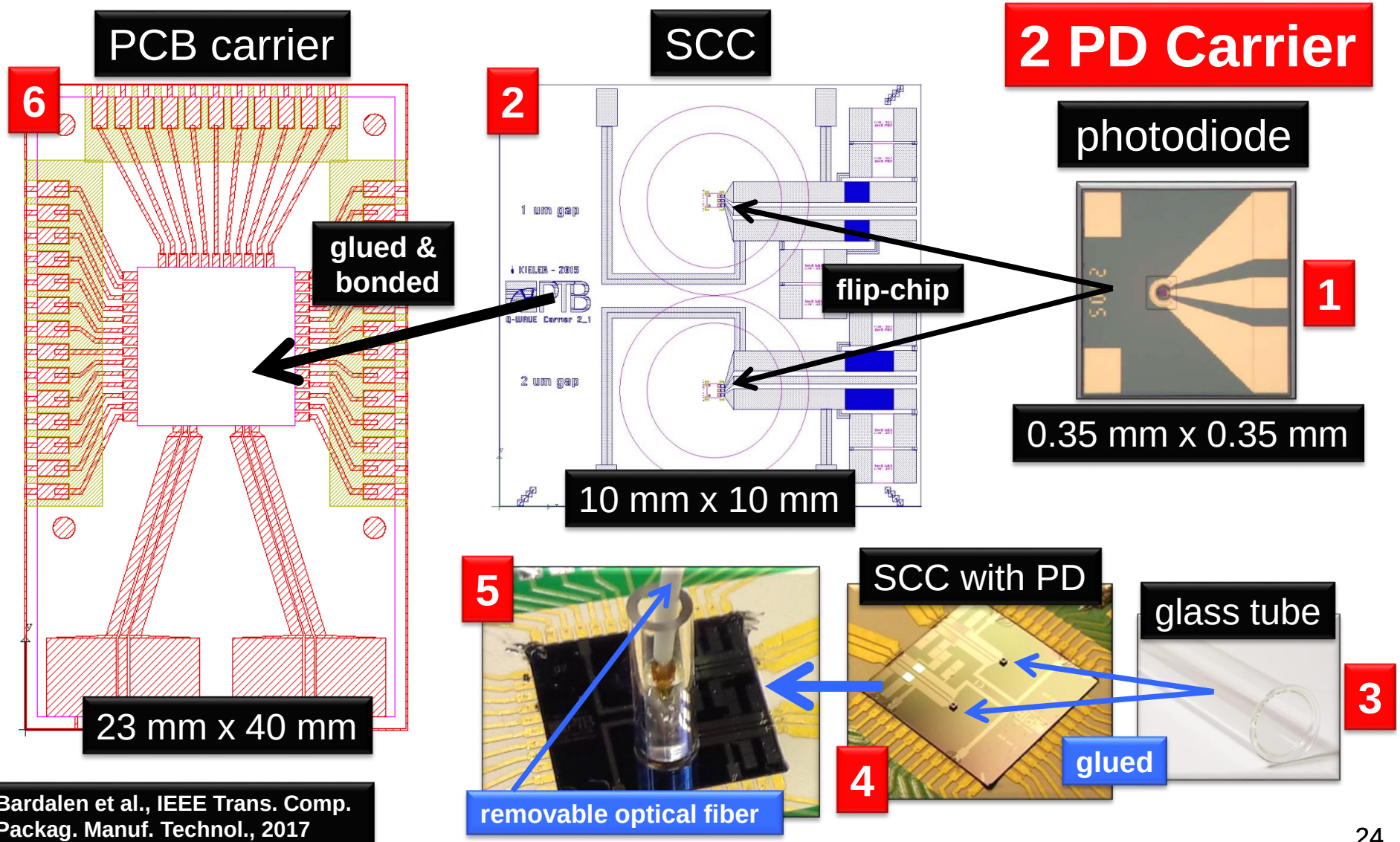
http://www.albisopto.com

University of South-Eastern Norway

Justervesenet

NPL National Physical Laboratory

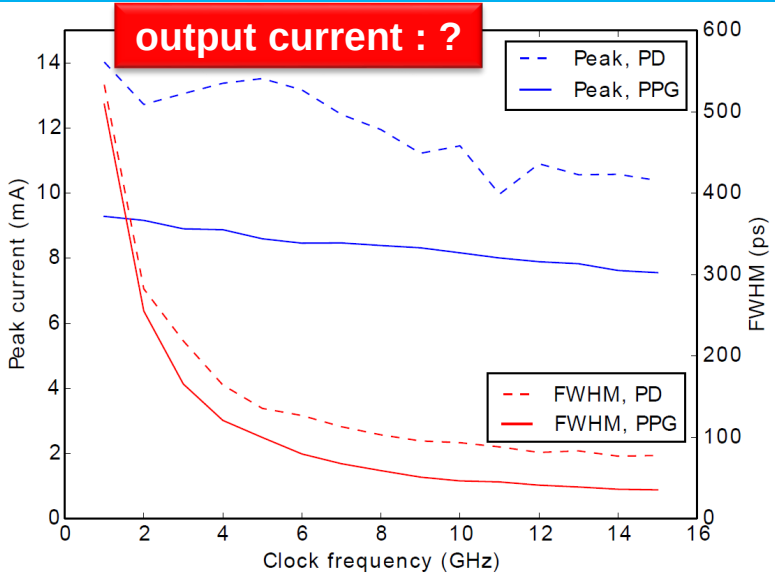
Mounting of PD's and tube @ USN, JV



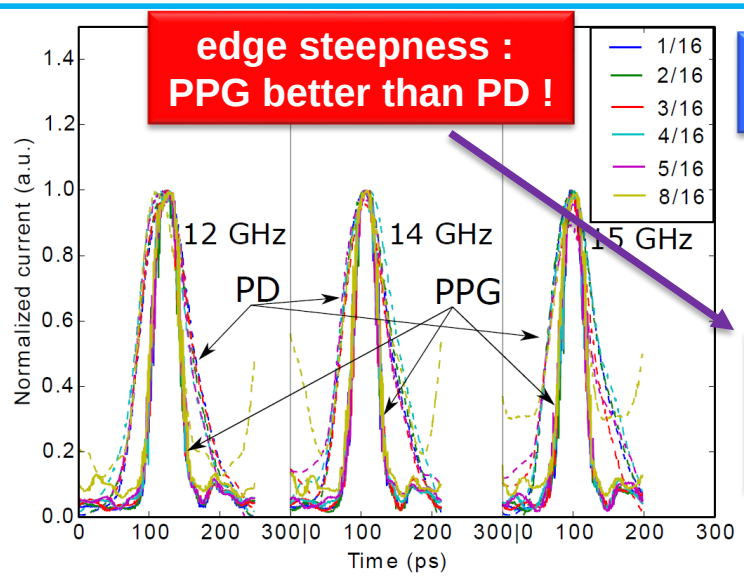
Bardalen et al., IEEE Trans. Comp. Packag. Manuf. Technol., 2017

PD's @ 4 K: HF-characterization

output current : ?

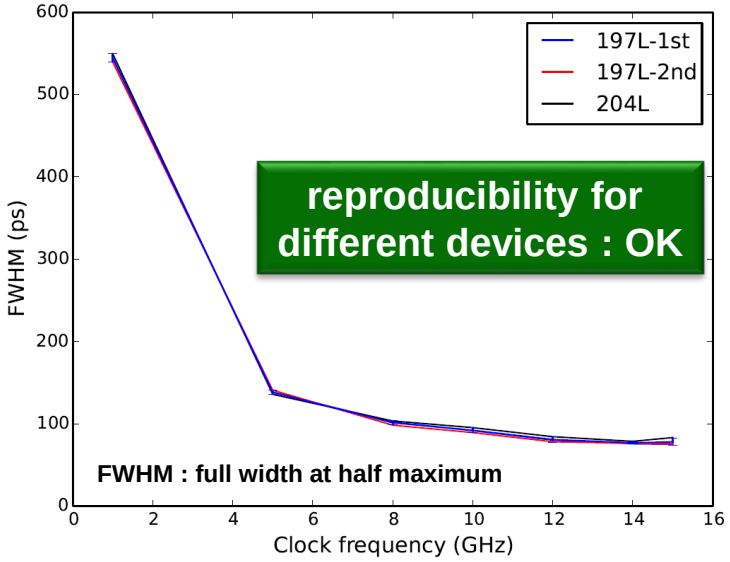


edge steepness : PPG better than PD !



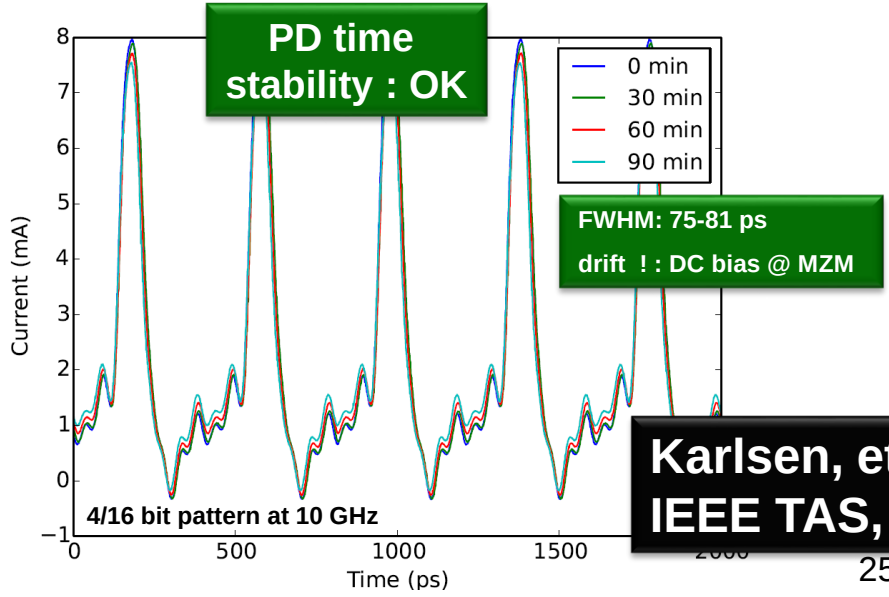
measurements made @ PTB

problem for maximum pulse rate !?



reproducibility for different devices : OK

PD time stability : OK

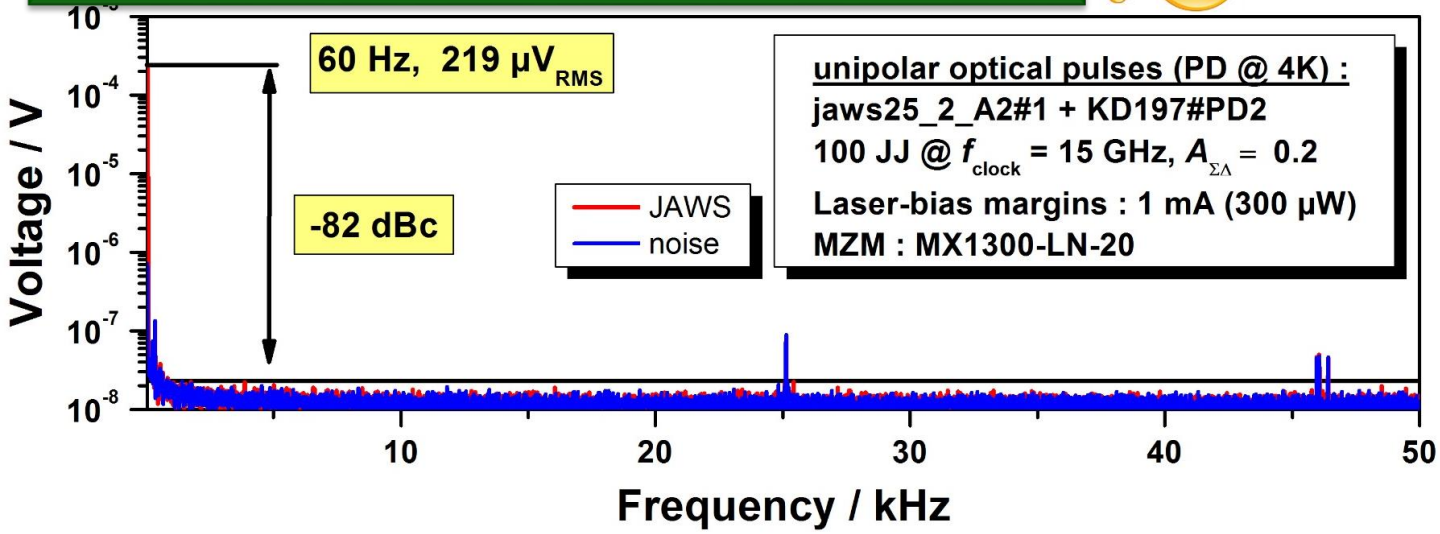


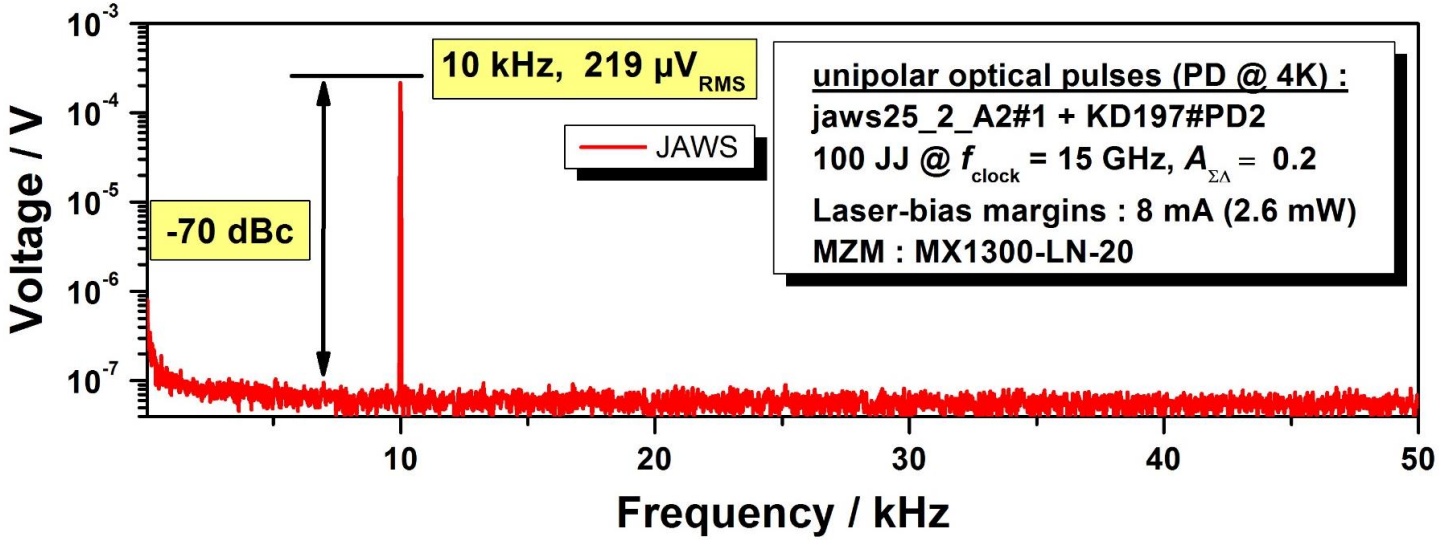
FWHM: 75-81 ps
drift ! : DC bias @ MZM

Karlsen, et al. : IEEE TAS, 2019

optical JAWS: signal frequency

spectrally pure waveforms synthesized



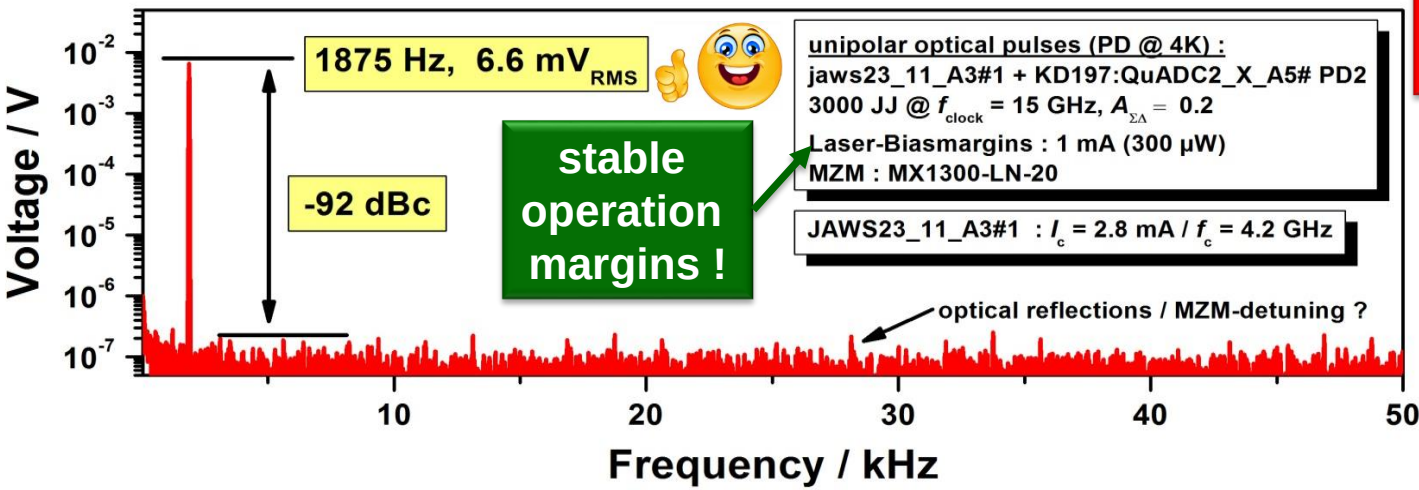


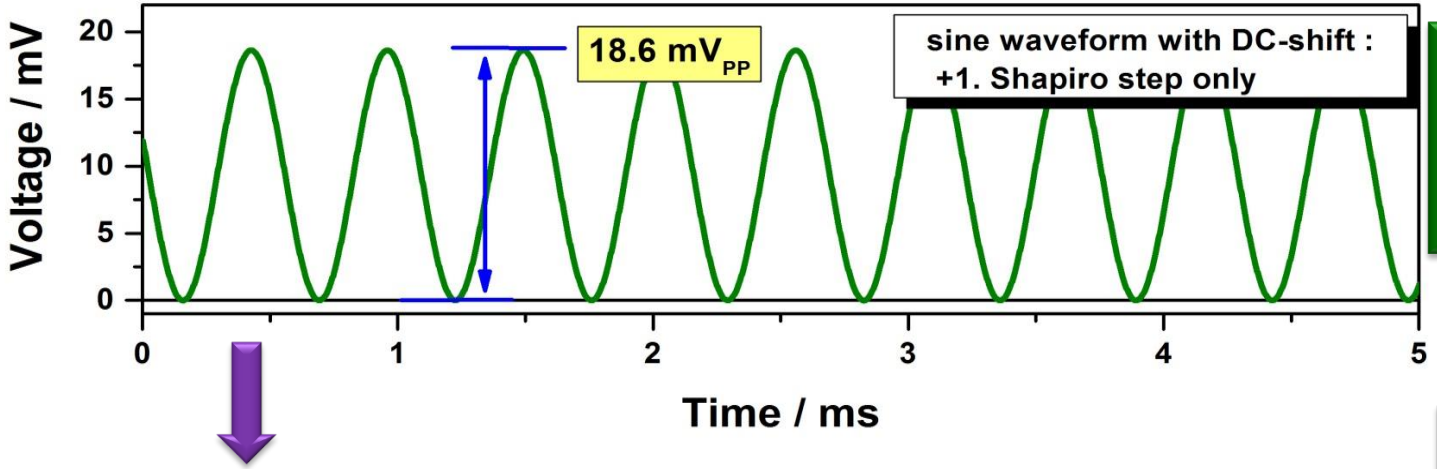
signal frequencies 60 Hz & 10 kHz

f_{clock} = 15 GHz

„full speed“

optical JAWS : number of junctions





JAWS with 3000 junctions

signal frequency 1875 Hz

f_{clock} = 15 GHz & $A_{\Sigma\Delta}$ = 20%

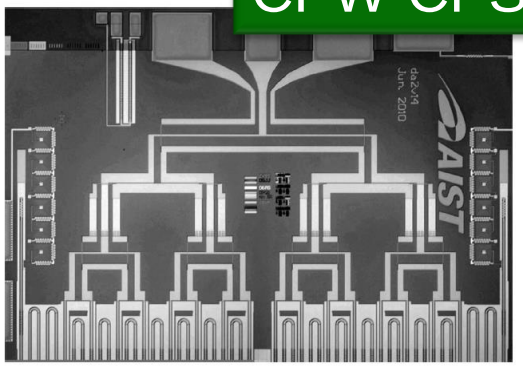
„full speed“

1 PD → unipolar operation → +1.SS only : DC-shift

Kieler, et al. : IEEE TAS, 2019

On-chip power splitter

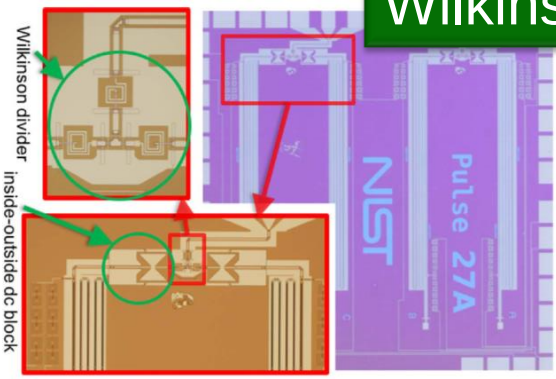
CPW-CPS



AIST

H. Yamamori and S. Kohjiro, *IEEE Trans. Appl. Supercond.*, Dec. 2016

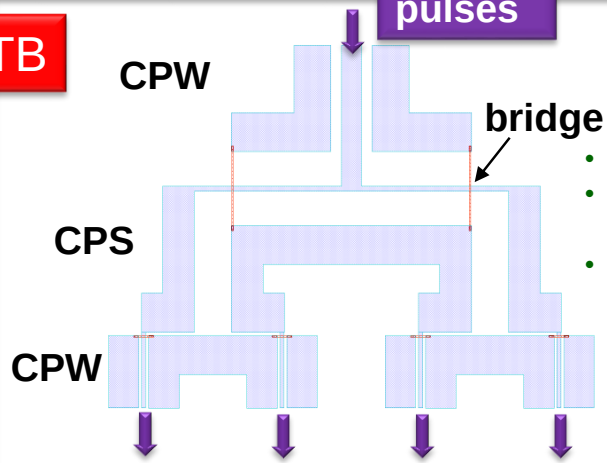
Wilkinson



NIST

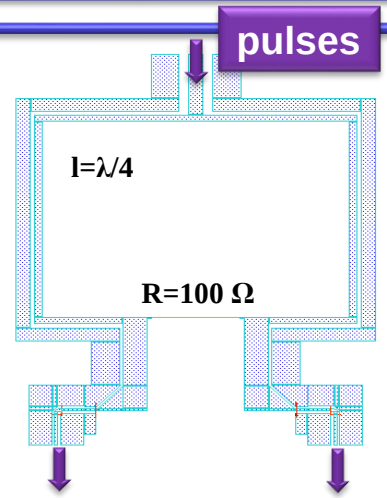
N. E. Flowers-Jacobs, et al., *IEEE Trans. Appl. Supercond.*, Sep. 2016

PTB



2-stage :

- Insertion loss: ca. 6 dB
- Return loss: > 20 dB (up to 30 GHz)
- Amplitude balance < 0.3 dB



1-stage :

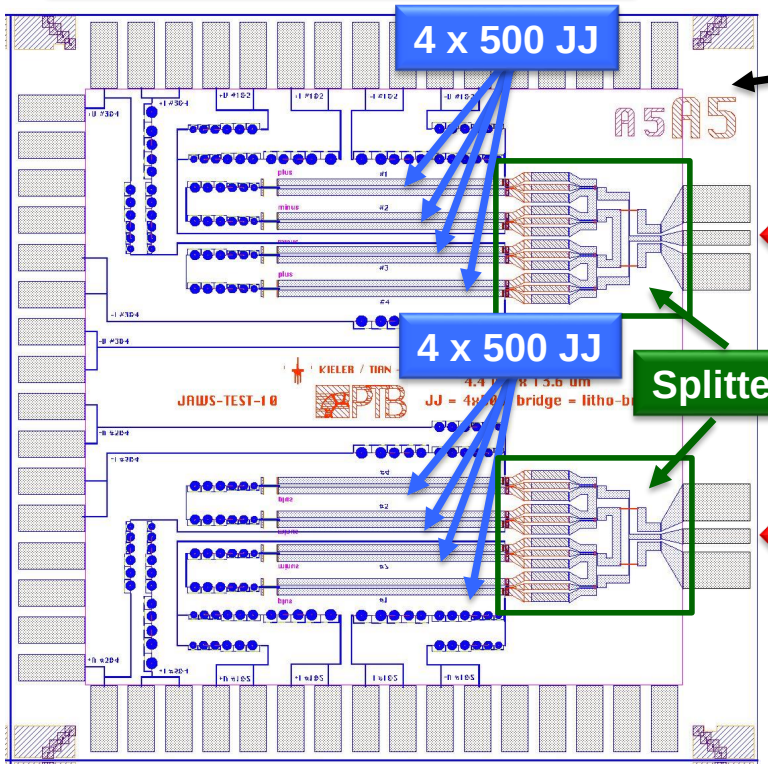
- Insertion loss: ca. 3 dB
- Return loss: > 10 dB (up to 25 GHz)
- Amplitude balance < 0.3 dB

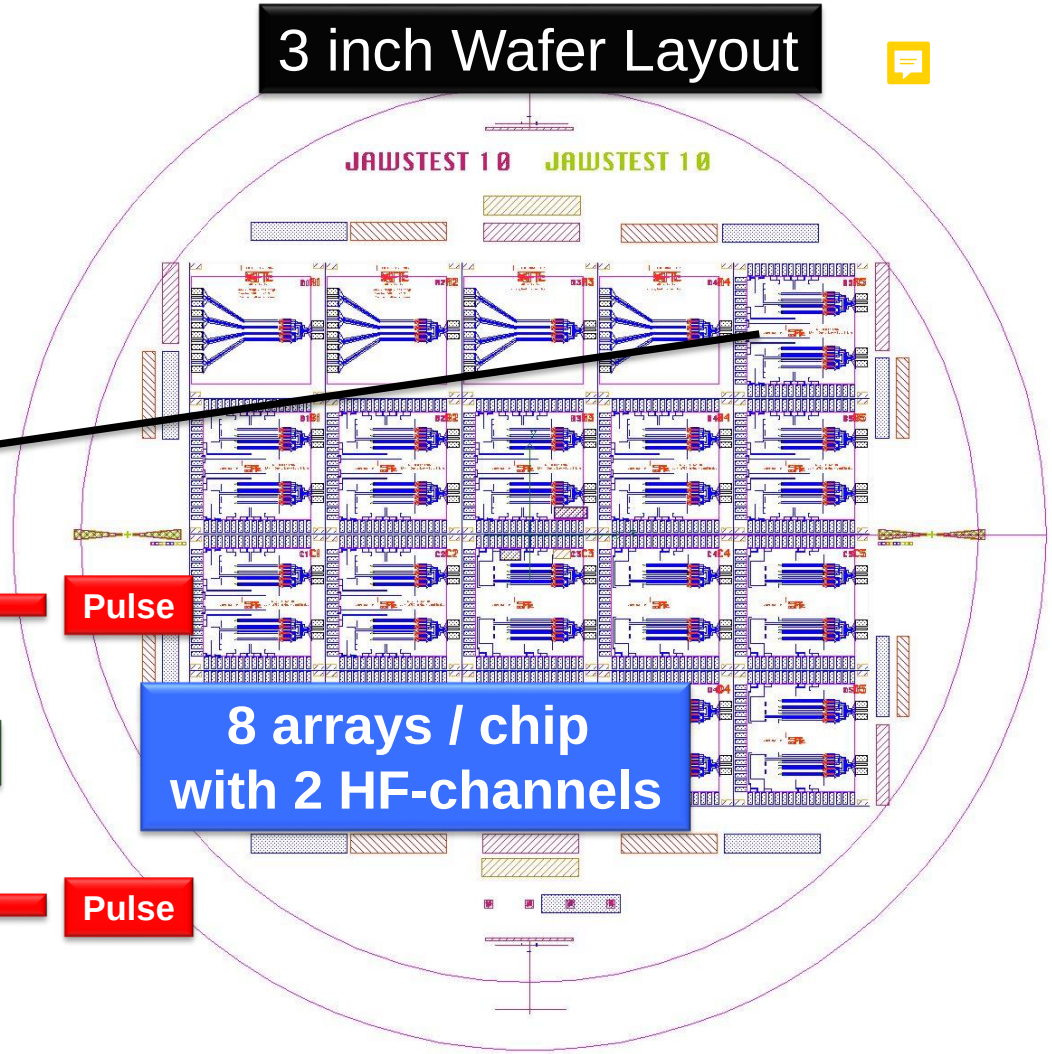
CST optimization

CPW-CPS splitter : layout

Design „JAWSTEST 10“ :

- chip size: 10 mm × 10 mm
- 2 arrays @ chip
- 4 chains @ array
- 500 JJs @ chain
- CPW: 50 Ohm
- CPW taper





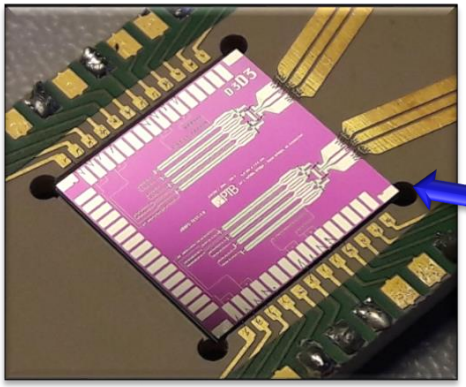
CPW-CPS splitter : fabrication

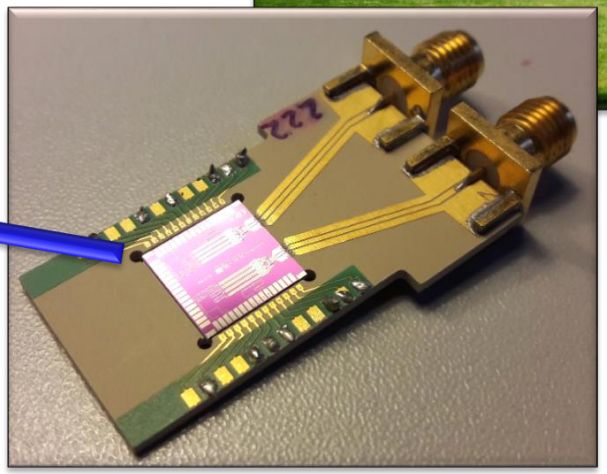
Design „JAWSTEST 10“ :

- chip size: 10 mm × 10 mm
- 2 arrays @ chip
- 4 chains @ array
- 500 JJs @ chain
- CPW: 50 Ohm
- CPW taper

PTB clean room

JAWS Chip





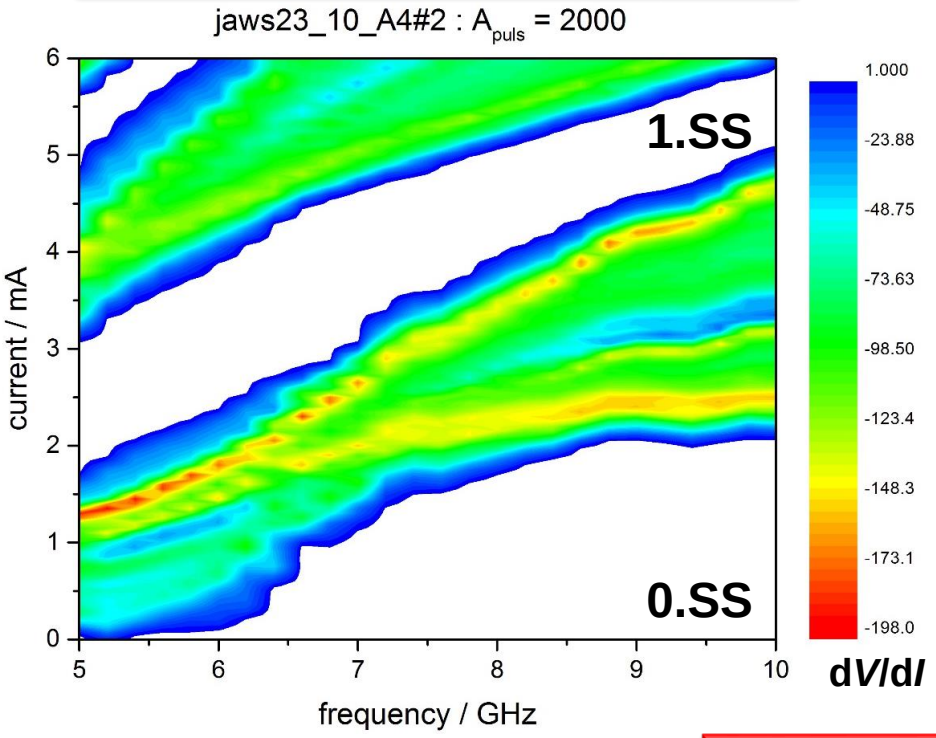
- SNS junctions: Nb_xSi_{1-x}
- standard window process

CPW-CPS splitter : IVC comparison

3) IVC vs. pulse frequency

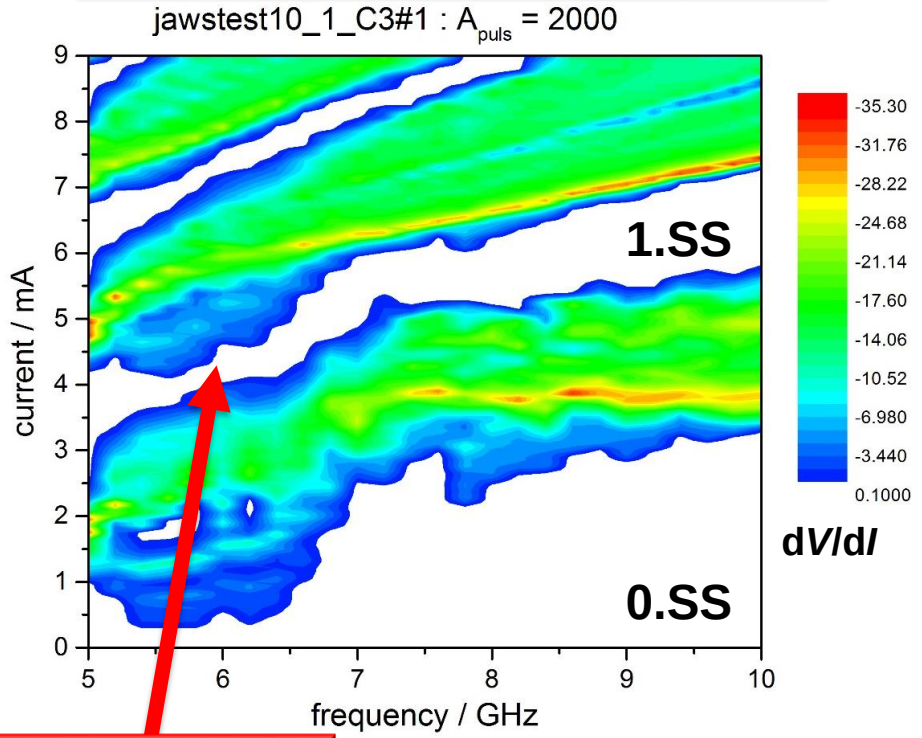
"standard" JAWS Array

12 000 junctions (4-stacked)



4 parallel JAWS Arrays

2 000 junctions (non-stacked)



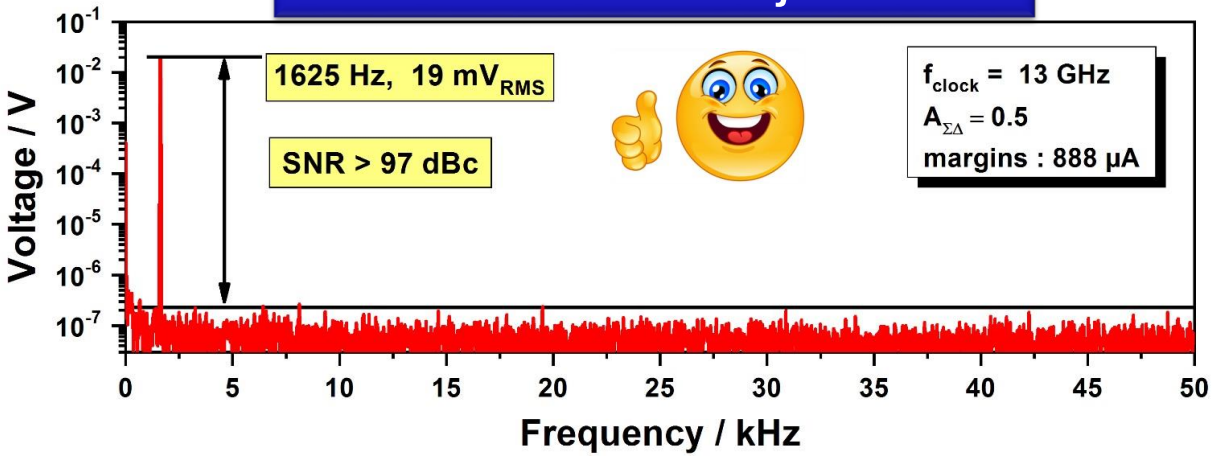
Shapiro step reduzed

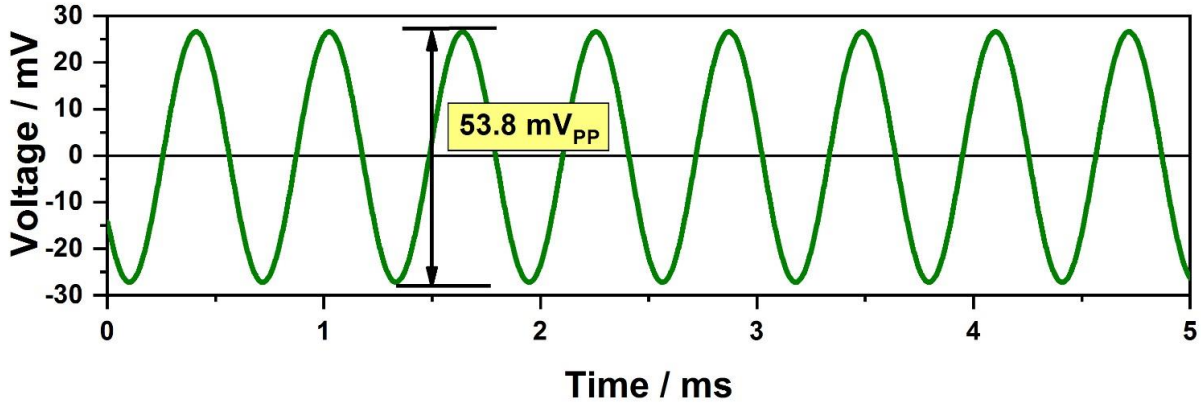
CPW-CPS splitter : waveform synthesis

PTB

4) synthesis sinus-waveform

2000 non-stacked junctions





pulse amplitude not sufficient

max. clock frequency 13 GHz (not 15 GHz !)

spectrum OK, and $A_{\Sigma\Delta}$ = 0.6

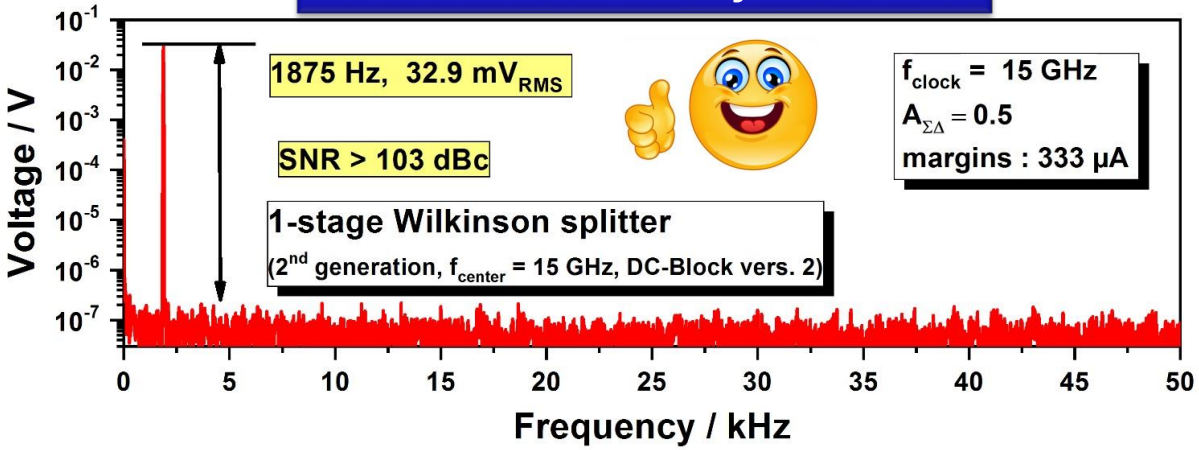
4 parallel arrays

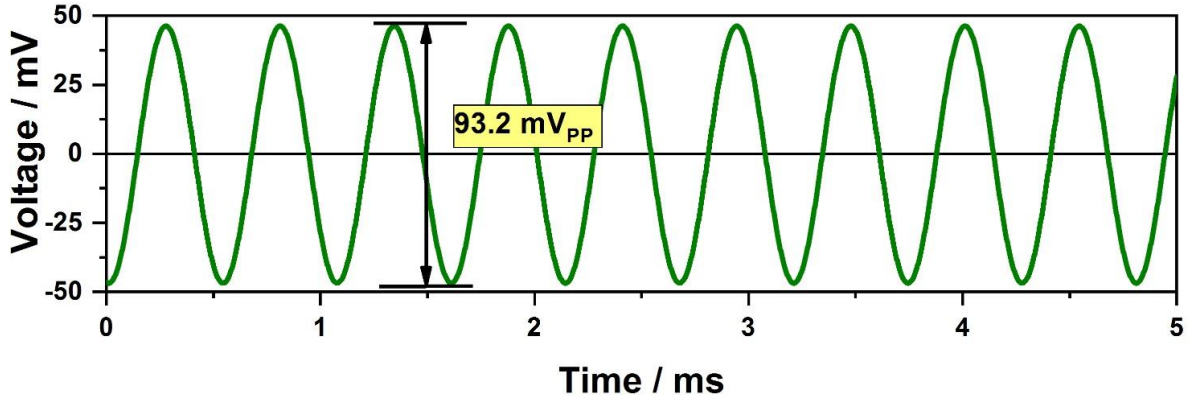
Design : 3rd generation

Wilkinson splitter : waveform synthesis

4) synthesis sinus-waveform

3000 3-stacked junctions





max. clock frequency 15 GHz

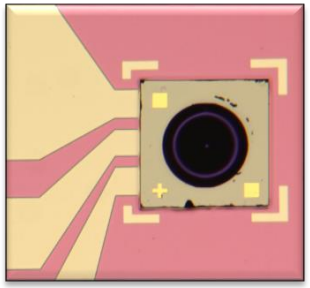
spectrum OK and $A_{\Sigma\Delta}$ = 0.5

2 parallel arrays

Design : 2nd generation

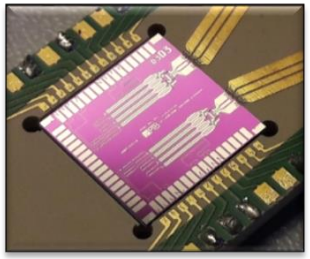
Tian, et al. : subm. to IEEE TAS, 2019

Summary and outlook



optical pulse drive

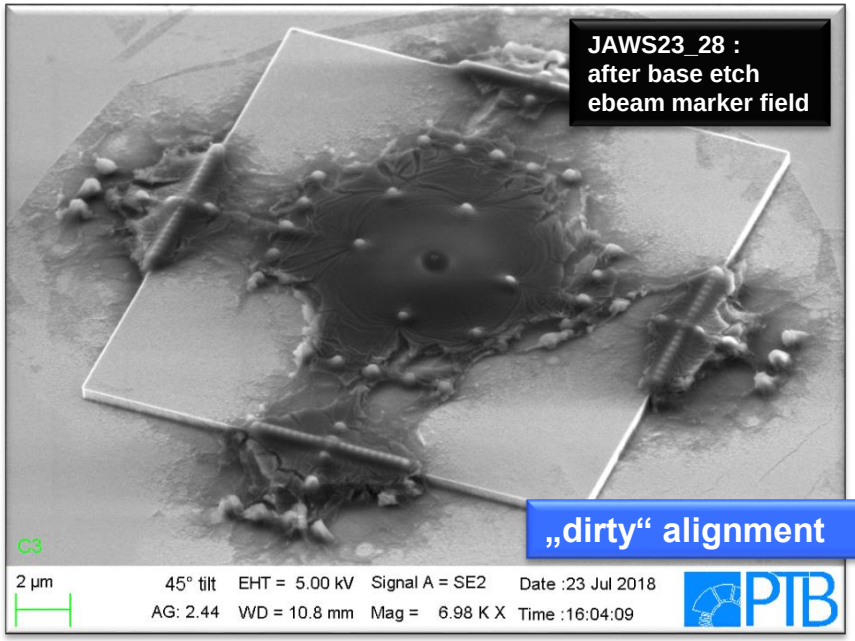
- Si-carrier chip (SCC) for photodiodes (PD) developed and fabricated
- PD @ SCC by flip-chip established
- easy-mount for optical fiber by glass tube developed
- operation of PD @ SCC and JAWS-chip @ 4.2 K
- spectrally pure unipolar waveforms synthesized
- next step : bipolar operation and higher integration density of PD's



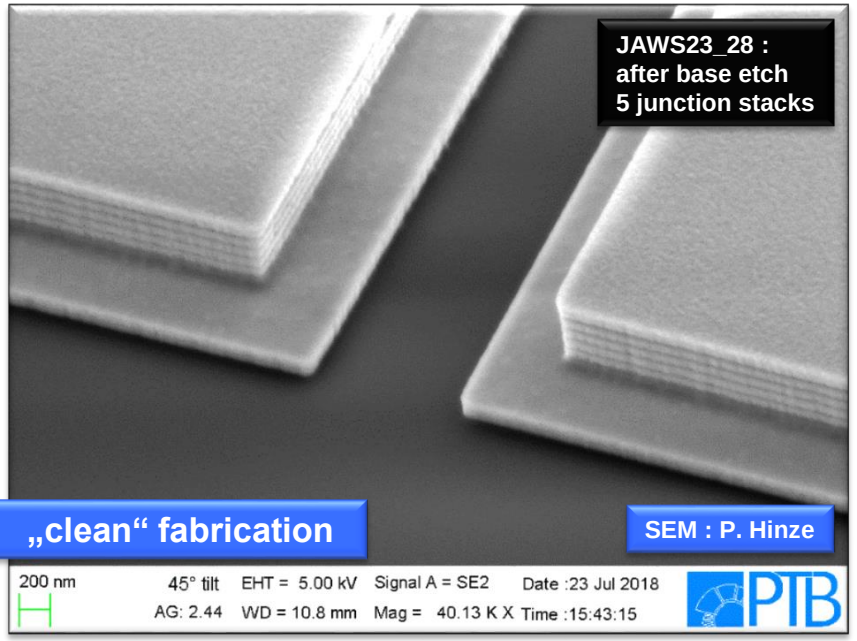
power splitter

- on-chip CPW-CPS- and Wilkinson-splitter optimized by simulations
- fabrication of JAWS circuits with up to 3000 3-stacked junctions
- spectrally pure bipolar waveforms with both splitter types
- next step : more junctions and 2-stage Wilkinson-splitter

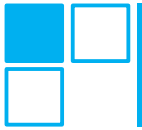
Thank you very much for your attention !



„dirty“ alignment → „clean“ fabrication



IEEE CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), September 2019.
Contributed presentation 2-ME-C-1 given at ISEC, 28 July-1 August 2019, Riverside, USA.



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