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Institute of Advanced Sciences

Yokohama National University YNU

15th Workshop on Low Temperature Electronics (WOLTE15)
Matera, Italy, June 6-9, 2022

Extremely energy-efficient superconductive logic circuits based on adiabatic flux quantum devices

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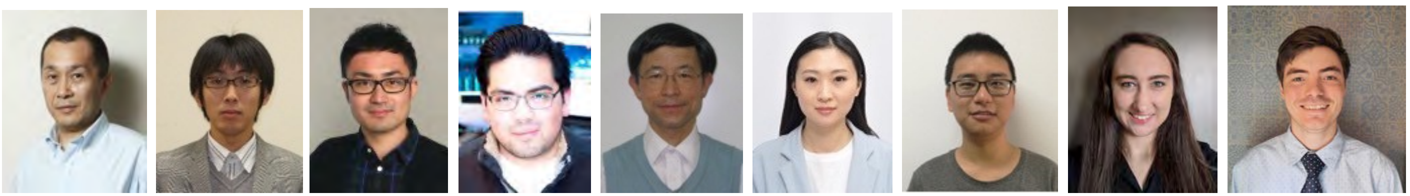
Members in the research unit on "Extremely Energy-Efficient Processors"



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Now in Tokyo City University

Now in Southwest Jiaotong University

Institute of Advanced Sciences
Yokohama National University

Overseas members

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CiS, Managing Director,
Germany

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Outline

- Background and motivation
- The minimum energy in computation?
  - Laudauer's principle
  - Adiabatic and reversible computing
- Adiabatic quantum flux parametron (AQFP)
- Present research activities of AQFP logic
  - High-performance computing
  - Readout circuit for a superconductor sensor array
  - Interface circuit for a quantum computer
- Reversible quantum flux parametron (RQFP)
- Summary

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Background

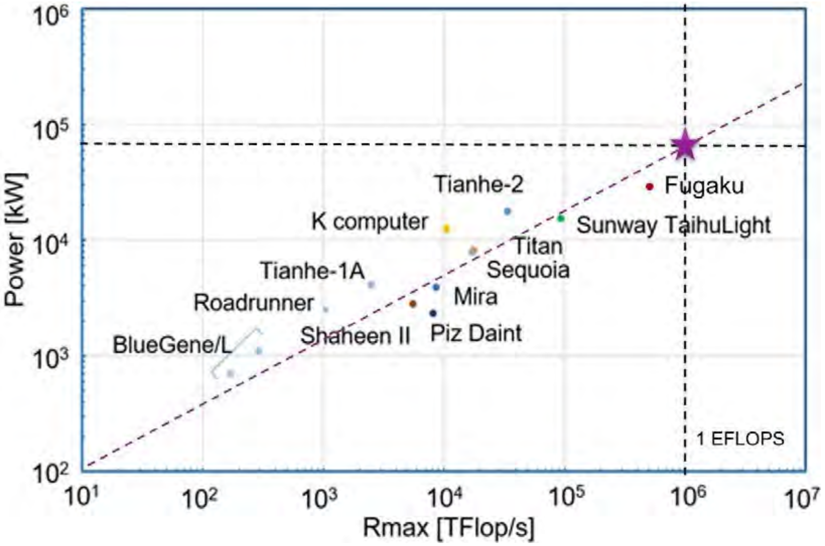
Estimated power consumption to achieve exa-scale computing

~ 100 MW ~ $100 million per year

Fugaku (Japan)

Peak performance: 513 PFLOPS
Power consumption: 28.3 MW

1st-ranked computers in recent TOP500



http://www.top500.org/

Low-Power Logic Devices is highly demanded.

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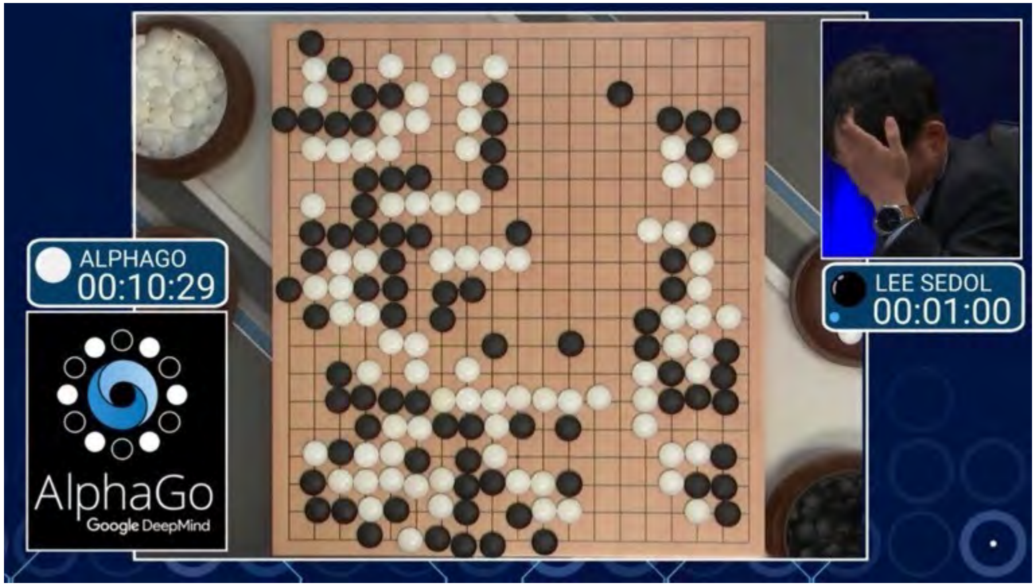
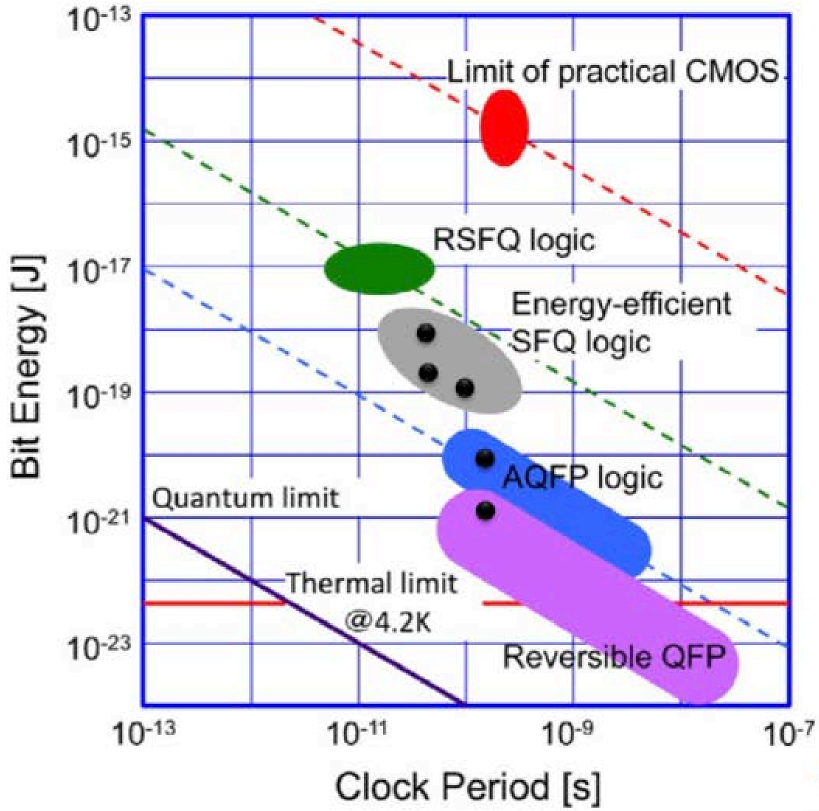
AI is Power Hungry



In 2016 AlphaGo program beat a human professional "Go" player.

AlphaGo	vs	Lee Sedol
1202 CPUs, 176 GPUs	vs	1 human brain
1 Mega Watt	vs	20 Watt, 1 coffee

Energy and Delay of Superconductor Logic



Quantum limit

$$\Delta E \Delta \tau \sim h$$

Thermal limit

$$E \sim k_B T \ln 2$$

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Minimum Energy in Computation?

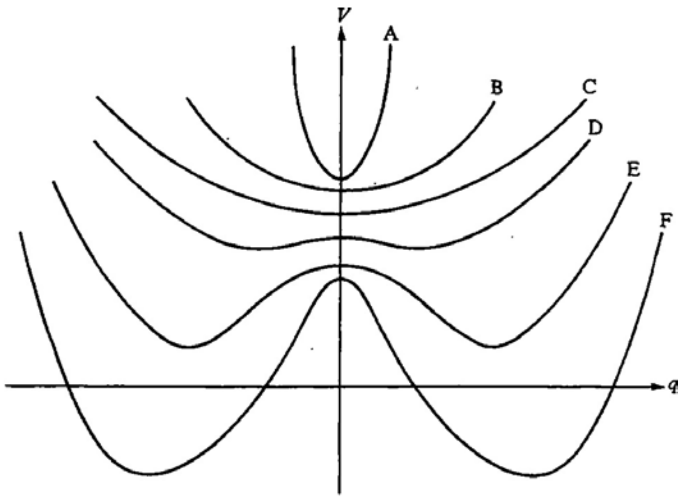


Figure 2 Time sequence of potentials starting at A (for a particle known to be near $q = 0$) and changing continuously to the deep bistable wells at F.

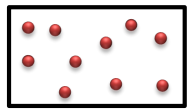
Adiabatic change of the energy potential of logic:
Single well ➔ Double well

Minimum energy dissipation when the "entropy" of information decreases:
$\sim k_B T \log 2$

R. W. Keyes, R. Landauer, *IBM Journal of Research and Development*, 14, 152 (1970).

Landauer's Principle

Thermodynamic entropy = Information entropy



101100010100110

- Equivalence between thermodynamic entropy and information entropy
- For computation reducing the information entropy, the minimum bit energy, $E_{bit} = k_B T \ln 2$, is consumed.
- For computation conserving the information entropy, there is no minimum limit of bit energy in computation.
- In erasure of results in computation, the bit energy is consumed.

R. Landauer, *IBM Journal of Research and Development* 5, 183 (1961).
C. H. Bennett, *IBM Journal of Research and Development* 17, 525 (1973).

Verification of the Landauer's Principle using Small Beads

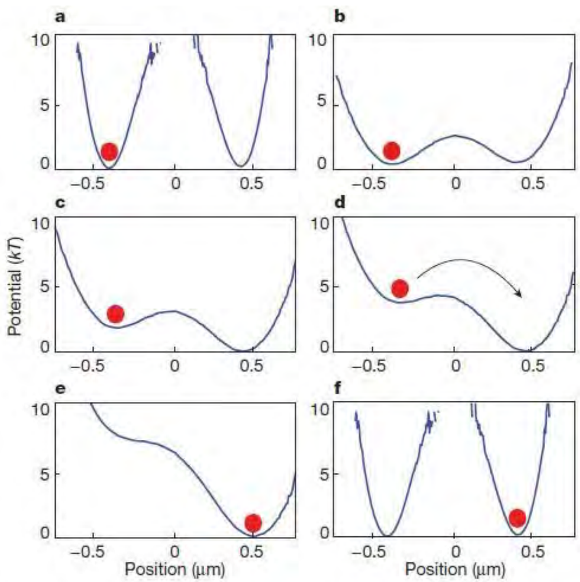


Figure 1 | The erasure protocol used in the experiment. One bit of information stored in a bistable potential is erased by first lowering the central barrier and then applying a tilting force. In the figures, we represent the transition from the initial state, 0 (left-hand well), to the final state, 1 (right-hand well). We do not show the obvious $1 \rightarrow 1$ transition. Indeed the procedure is such that irrespective of the initial state, the final state of the particle is always 1. The potential curves shown are those measured in our experiment (Methods).

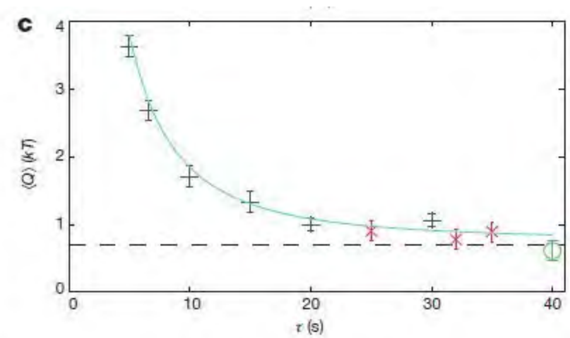


Figure 3 | Erasure rate and approach to the Landauer limit. a, Success rate of the erasure cycle as a function of the maximum tilt amplitude, F_{max}, for constant $F_{max}\tau$. **b,** Heat distribution P(Q) for transition $0 \rightarrow 1$ with $\tau = 25$ s and $F_{max} = 1.89 \times 10^{-14}$ N. The solid vertical line indicates the mean dissipated heat, $\langle Q \rangle$, and the dashed vertical line marks the Landauer limit, $\langle Q \rangle_{Landauer}$. **c,** Mean dissipated heat for an erasure cycle as a function of protocol duration, τ, measured for three different success rates, r: plus signs, $r \geq 0.90$; crosses, $r \geq 0.85$; circles, $r \geq 0.75$. The horizontal dashed line is the Landauer limit. The continuous line is the fit with the function $[A\exp(-t/\tau_K) + 1]B/\tau$, where τ_K is the Kramers time for the low barrier (Methods). Error bars, 1 s.d.

A. Berut *et al*., *Nature,* 483, (2012) 187.

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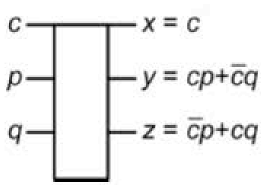
Reversible Computing

- For reversible computation, there is no minimum bound in bit energy.
- The entropy in computation is conserved.
- Logical reversibility is required.
- In addition, physical reversibility or thermodynamical reversibility is required.

R. Landauer, *IBM Journal of Research and Development* 5, 183 (1961).
C. H. Bennett, *IBM Journal of Research and Development* 17, 525 (1973).

Example: Fredkin gate



Truth table of Fredkin gate

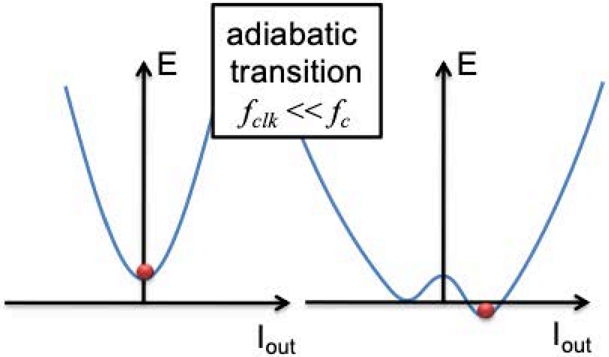
Input			Output		
c	p	q	x	y	z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Injective function

E. Fredkin and T. Toffoli, *Int. J. Theor. Phys.* **21**, 219-253 (1982).

Adiabatic and Reversible Computing

Adiabatic computing



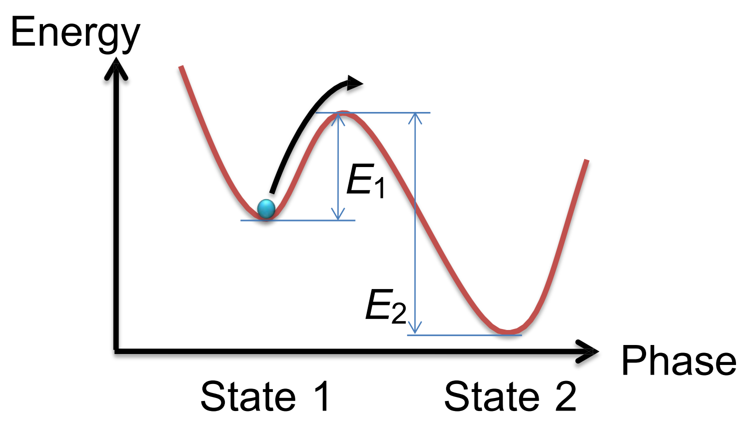
- Potential of the system is changed adiabatically
- No nonadiabatic energy dissipation

$$E_{bit} \propto f_{clock}$$

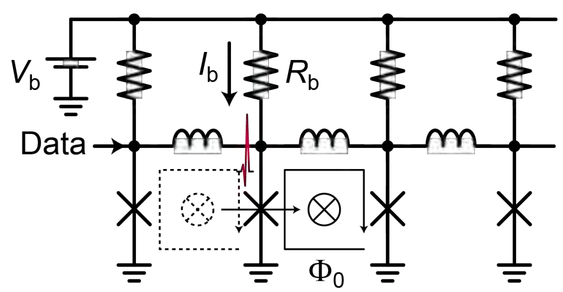
Reversible computing

- Input data can be calculated from output data.
- Number of input = Number of output
- No change in information entropy

Energy Potential of RSFQ Circuits



RSFQ Circuits



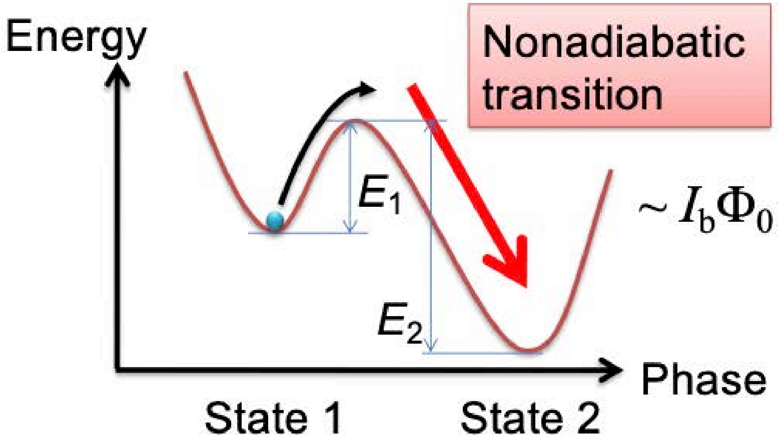
Input energy: E_1
Output energy: E_2

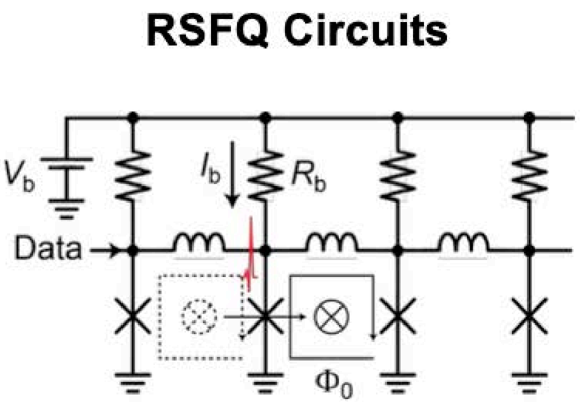
Energy gain : E_2/E_1
Energy dissipation : E_2 - E_1

Requirement for the reduction of switching errors

$$E_1 > 100\ k_B T$$

Energy Potential of RSFQ Circuits

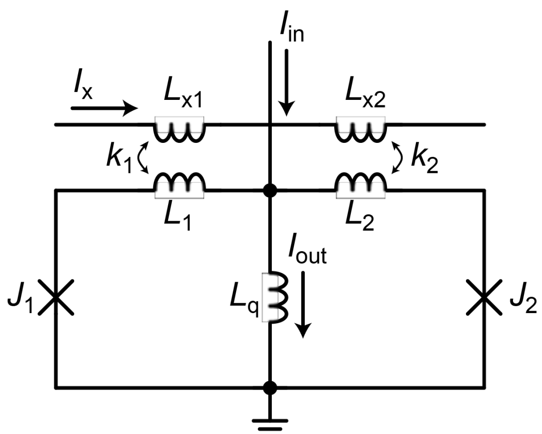




Adiabatic operation of the system is required for energy-efficient computing.

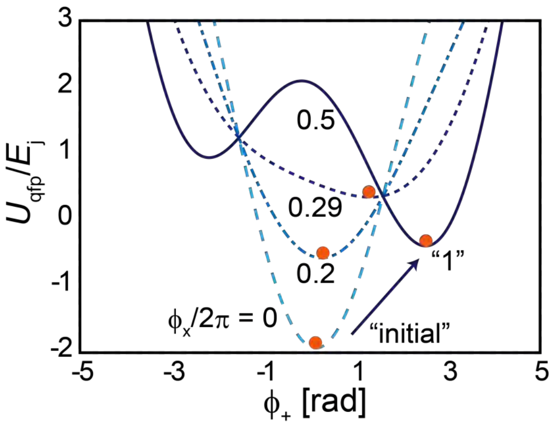
Operation Principle of Adiabatic Quantum Flux Parametron (AQFP)

AQFP gate



An SFQ is stored in the right or left loop depending on I_{in}.

Potential energy of the gate



Potential energy changes adiabatically during switching.

E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984.*

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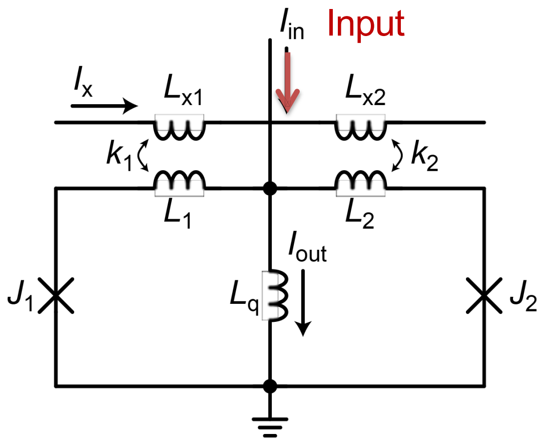
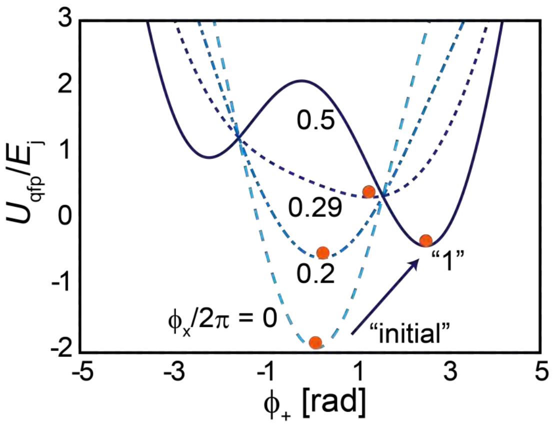
Operation Principle of Adiabatic Quantum Flux Parametron (AQFP)

AQFP gate



Potential energy of the gate



Potential energy changes
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Operation Principle of Adiabatic Quantum Flux Parametron (AQFP)

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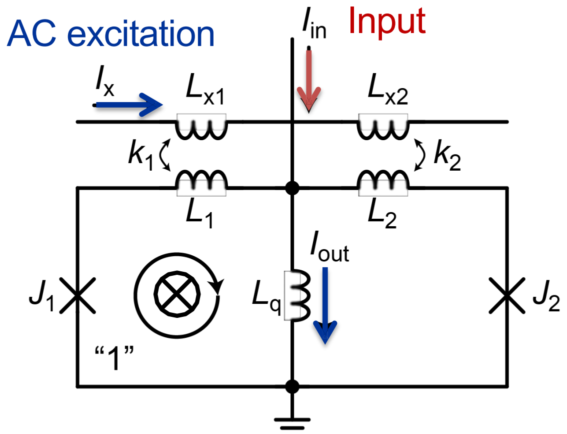
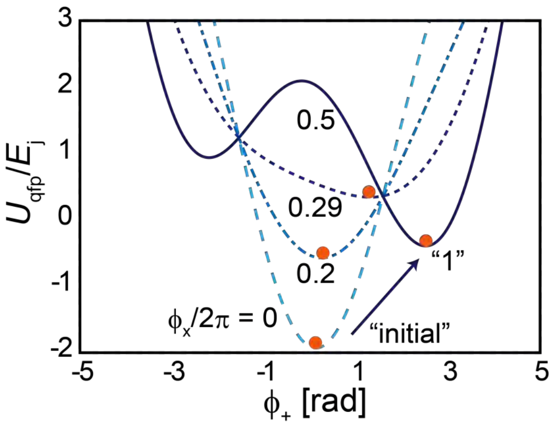


I_{out} flows downward.

Potential energy of the gate



Potential energy changes adiabatically during switching.

E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984.*

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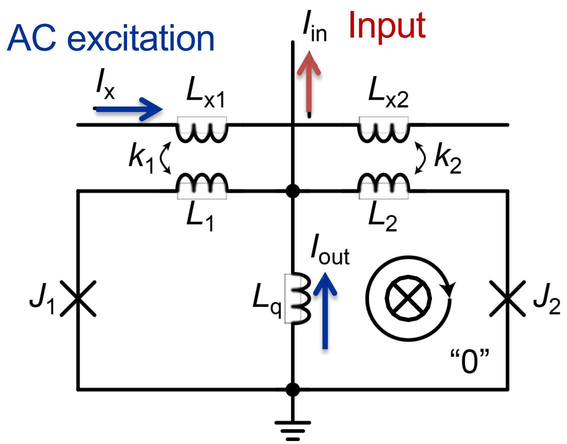
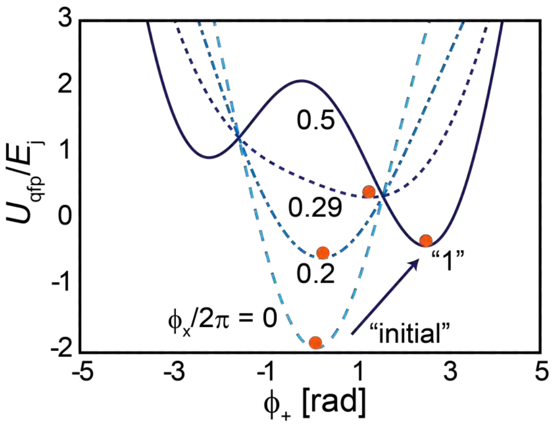
Operation Principle of Adiabatic Quantum Flux Parametron (AQFP)

AQFP gate



I_{out} flows upward.

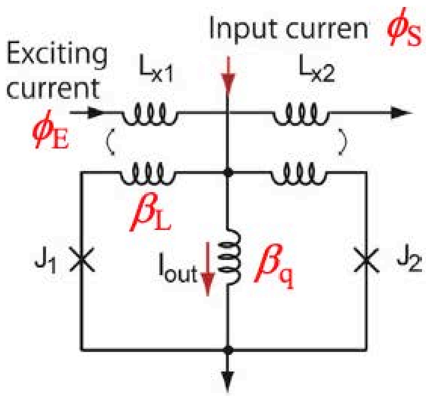
Potential energy of the gate



Potential energy changes adiabatically during switching.

E. Goto, *Pros. 1st RIKEN Symp. Josephson Electronics, 1984*.

Potential Energy of QFP



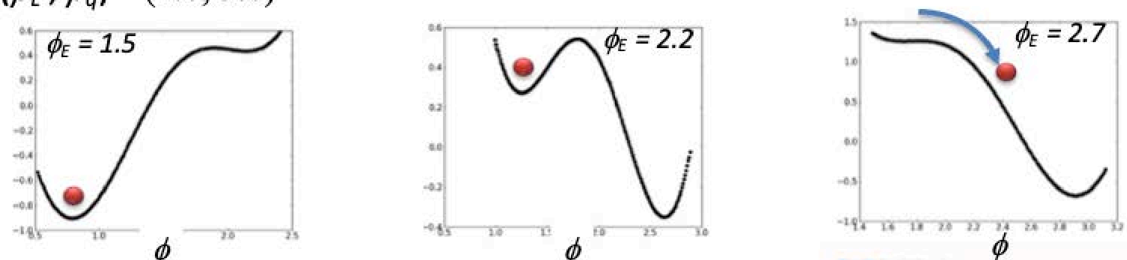
$$U_{qfp} = E_j \left[\frac{(\phi_E - \phi_-)^2}{\beta_L} + \frac{(\phi_S - \phi_+)^2}{\beta_L + 2\beta_q} - 2\cos\phi_- \cos\phi_+ \right]$$

Normalized exciting current $\phi_E = 2\pi \frac{M_1 I_E}{\Phi_0}$, Normalized input current $\phi_S = 2\pi \frac{L_q I_S}{\Phi_0}$

Normalized loop inductance $\beta_L = 2\pi \frac{L_1 I_0}{\Phi_0}$, Normalized output inductance $\beta_q = 2\pi \frac{L_q I_0}{\Phi_0}$

$$E_j = \frac{E_J}{2\pi} = \frac{I_0 \Phi_0}{2\pi}, \quad \phi_+ = \frac{\phi_1 + \phi_2}{2}, \quad \phi_- = \frac{\phi_1 - \phi_2}{2}$$

◆ $(\beta_L, \beta_q) = (1.0, 3.0)$



M. Hosoya *et al.*, *IEEE Trans. Appl. Supercond.* 1, 77 (1991).

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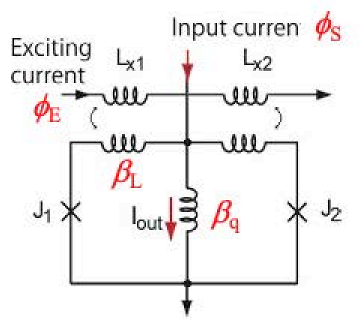
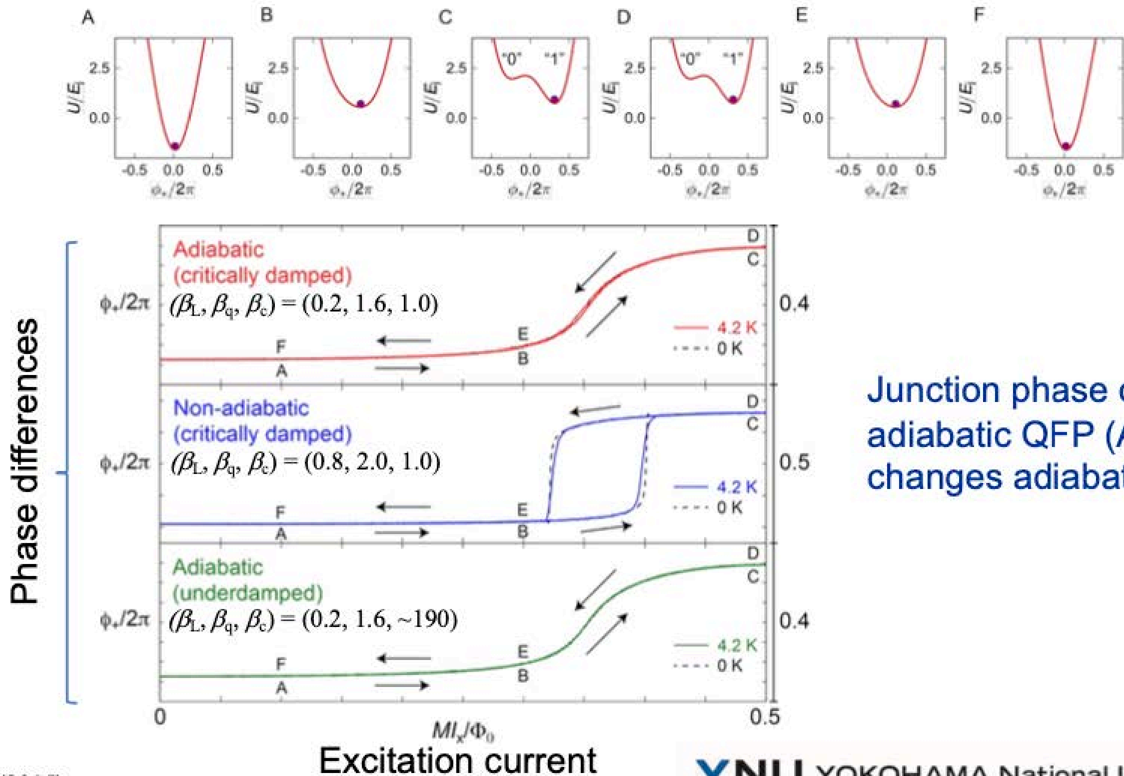
Junction Phase vs. Excitation Current of QFP



- β_c: McCumber parameter

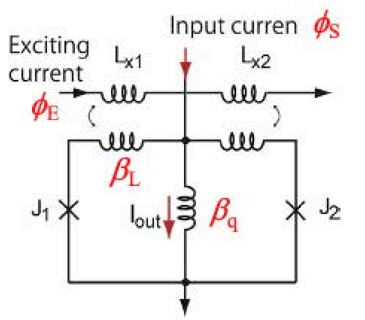
$$\beta_c = \frac{\omega_c C}{G}$$



Junction phase of adiabatic QFP (AQFP) changes adiabatically.

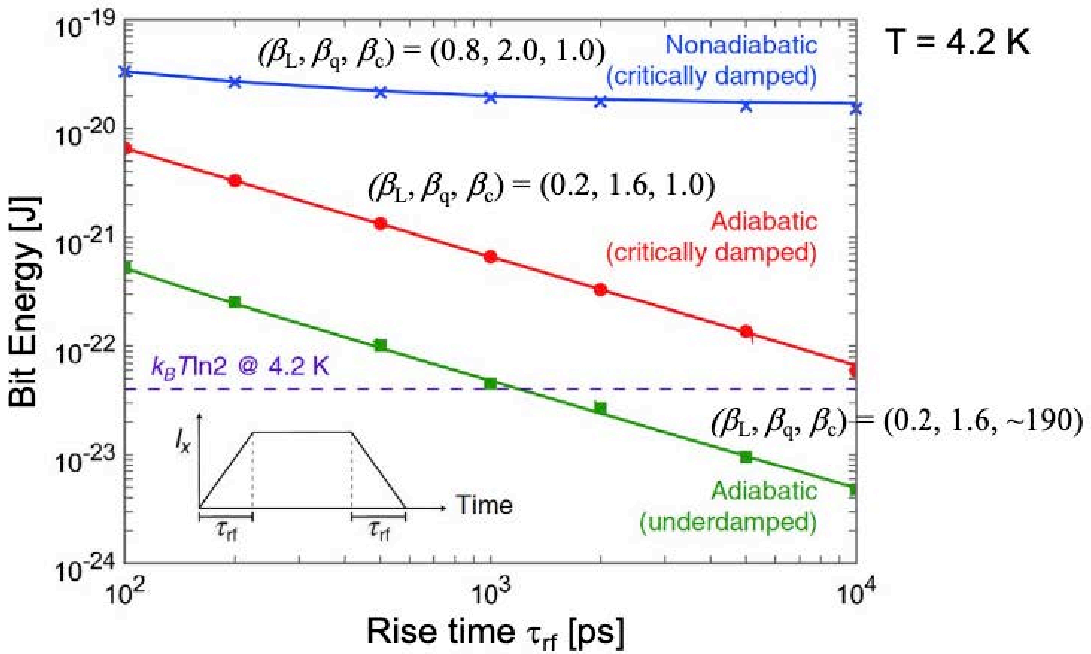
Takeuchi *et al.,* Phys. Rev. Appl. 4, 034007 (2015).

Bit Energy vs. Rise Time of Excitation Current of AQFP



- β_c: McCumber parameter

$$\beta_c = \frac{\omega_c C}{G}$$



E_{bit} ~ 0.05 zJ (~ $k_B T$) when rise time = 1000 ps

Takeuchi *et al.*, Phys. Rev. Appl. 4, 034007 (2015).

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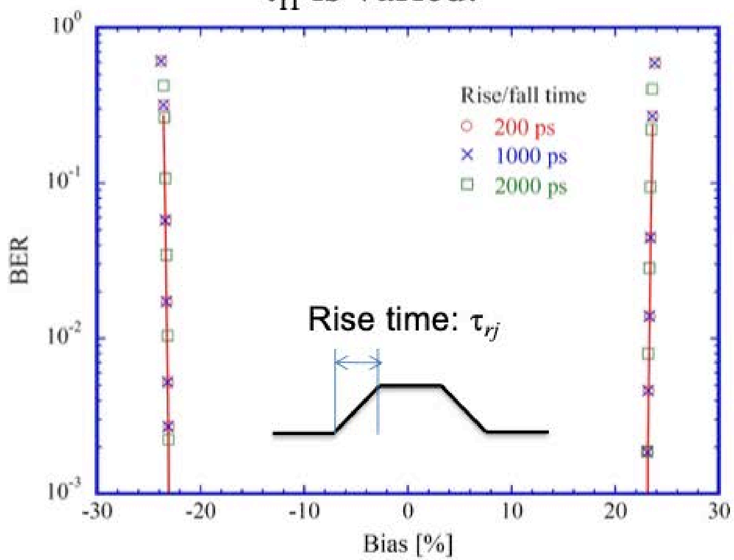
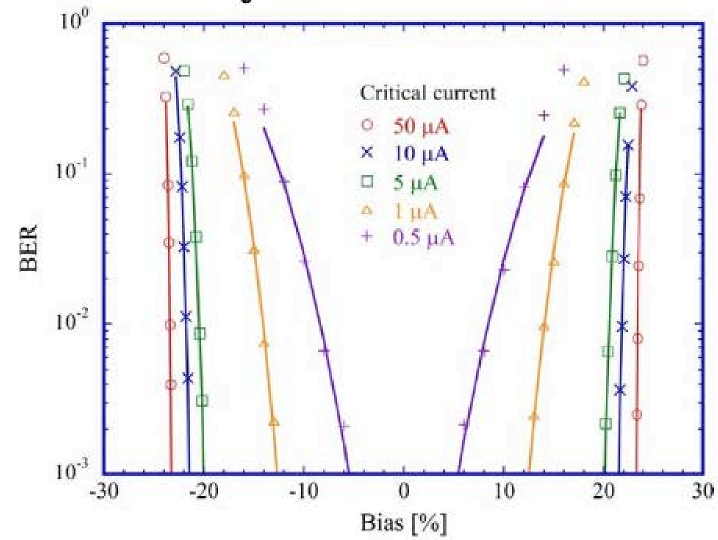
Bit Error Rate (BER) of AQFP at 4.2 K

τ_{rf} is varied.



$\beta_c \sim 2600$, $I_c = 50\ \mu A$.

I_c is varied.



$\beta_c \sim 2600$, $\tau_{rf} = 200$ ps.

- When τ_{rf} increases → decrease of the bit-energy, no increase of BER
- When I_c decreases → decrease of the barrier height, increase of BER

N. Takeuchi, *et. al*., *Appl. Phys. Lett.*, 103, 062602 (2013).

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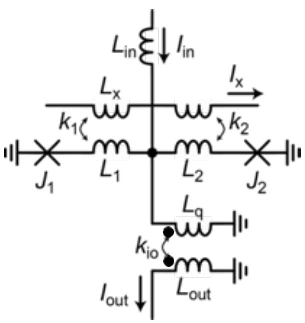
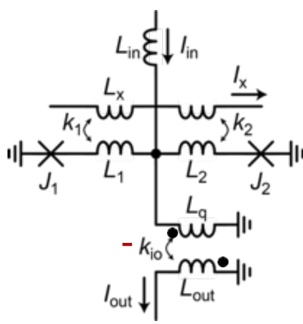
Primitive of AQFP Logic

- NOT gate is cost free.
- Majority gate is a basic logic gate.

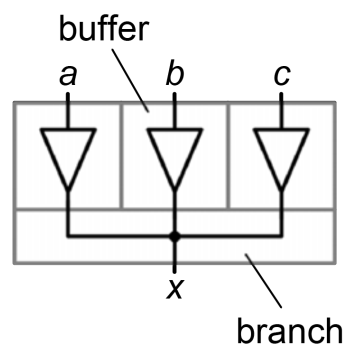
Buffer



NOT

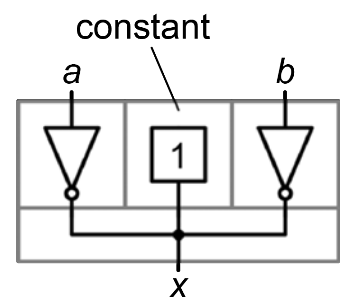


Majority



$x = \mathrm{MAJ}(a, b, c)$
$= ab+bc+ca$

NAND



$x = \mathrm{MAJ}(\bar{a}, 1, \bar{b})$
$= \overline{ab}$

K. Inoue, *et al*. IEEE Trans. Appl. Supercond., **23**, 1301105 (2013).

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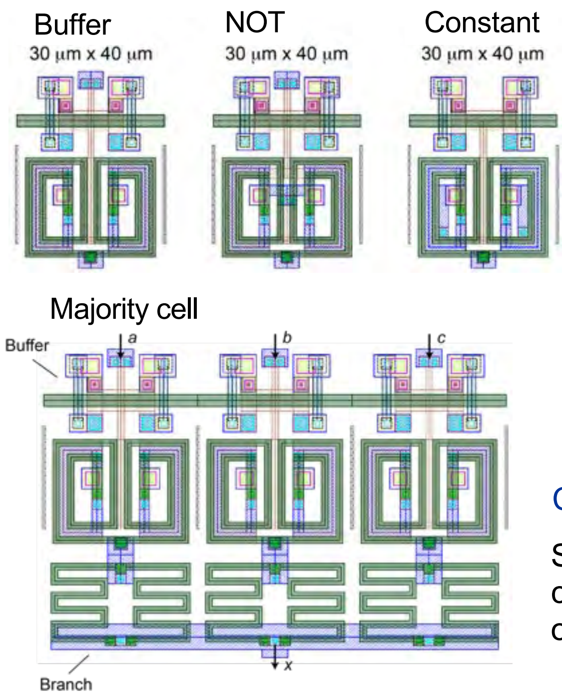
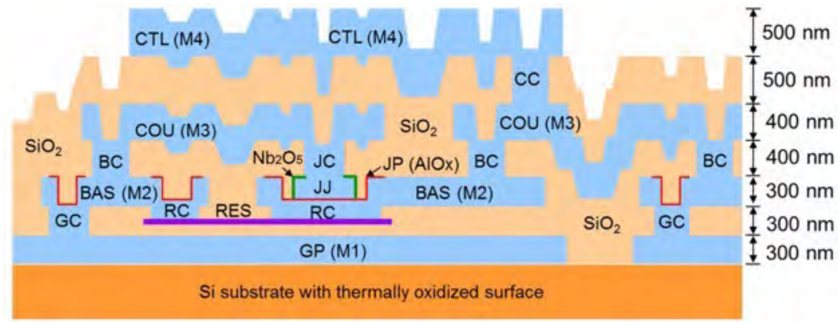
Layout of AQFP Basic Cells (AIST Process)

AQFP cell layouts



N. Takeuchi *et al.*, J. Appl. Phys. **117**, 173912 (2015).

AIST superconductor IC process



CRAVITY AIST

4-metal layers Nb/AlO$_x$/Nb 10 kA/cm^2 Josephson high-speed standard process (HSTP)

Cell size: 30 µm x 40 µm

Symmetric design reduces the parasitic coupling between the excitation and output inductances.

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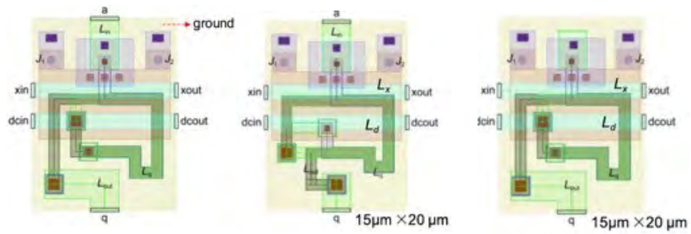
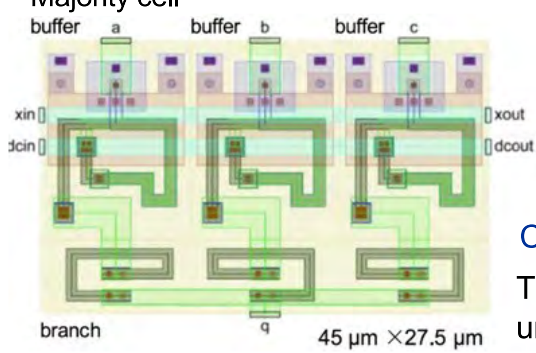
Layout of AQFP Basic Cells (MIT LL Process)

AQFP cell layouts

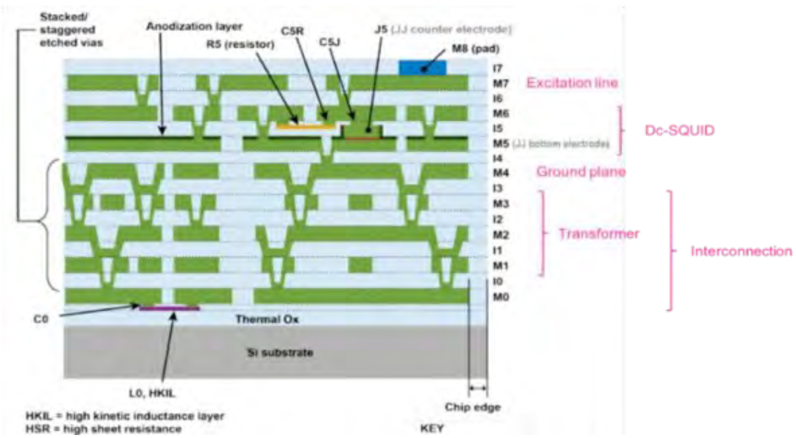
Buffer NOT Constant



Majority cell



MIT LL superconductor IC process



MIT LL 8-metal layers Nb/AlO$_x$/Nb 10 kA/cm^2 Josephson process

Cell size: 15 μm x 20 μm.

Transformer is placed underneath the AQFP gate.

Y. He, *et. a*l., *SUST*, 33, 035010 (2020).

IARPA

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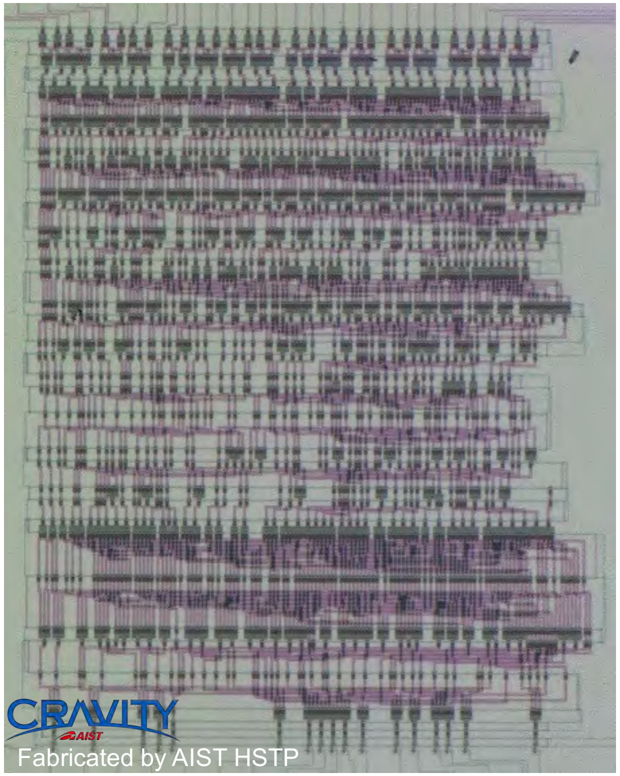
Demonstration of AQFP 16b Carry Look-Ahead Adder



Low-speed test results

f = 100 kHz
T = 4.2 K

Area	10.1 mm^2
Complexity	4976 JJs
Bias current	3.0 mA (AC)
Target frequency	5 GHz
Energy/op	~3.5 aJ

T. Tanaka *et al*., IEICE 105-C, 2022

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- Adiabatic quantum flux parametron (AQFP)
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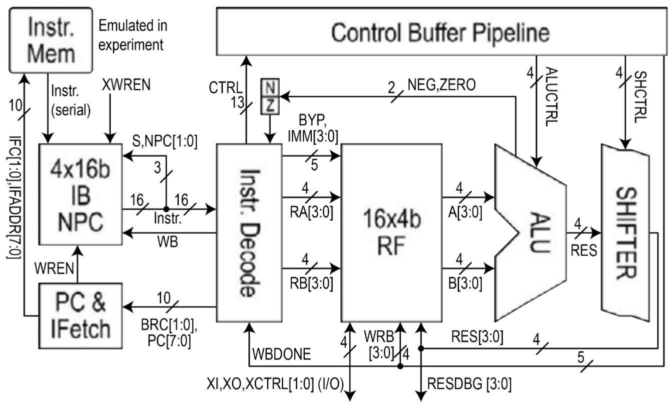
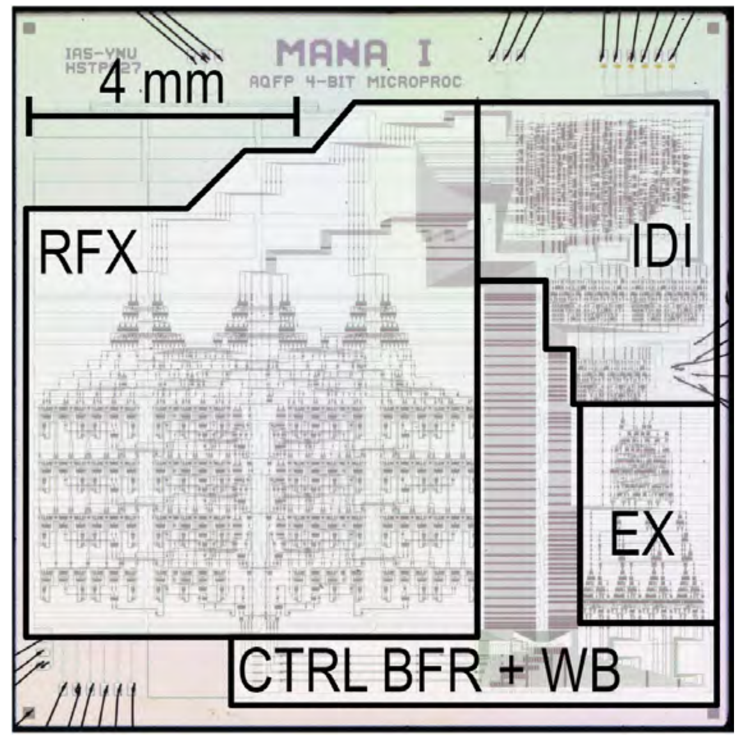
Demonstration of AQFP 4b RISC Microprocessor





MANA – **M**onolithic **A**diabatic i**N**tegration **A**rchitecture

- RISC + dataflow (4-bit data, 16-bit instruction)
- 15 aJ/op @ 5GHz
- 27 cycles/operation (5.4ns @ 5GHz)
- Nb/AlOx/Nb 10 kA/cm^2 AIST process
- 21,460 JJs on 1 x 1 cm^2 chip

Fabricated by AIST HSTP

C. Ayala *et al*., IEEE Journal of Solid-State Circuits, 2020

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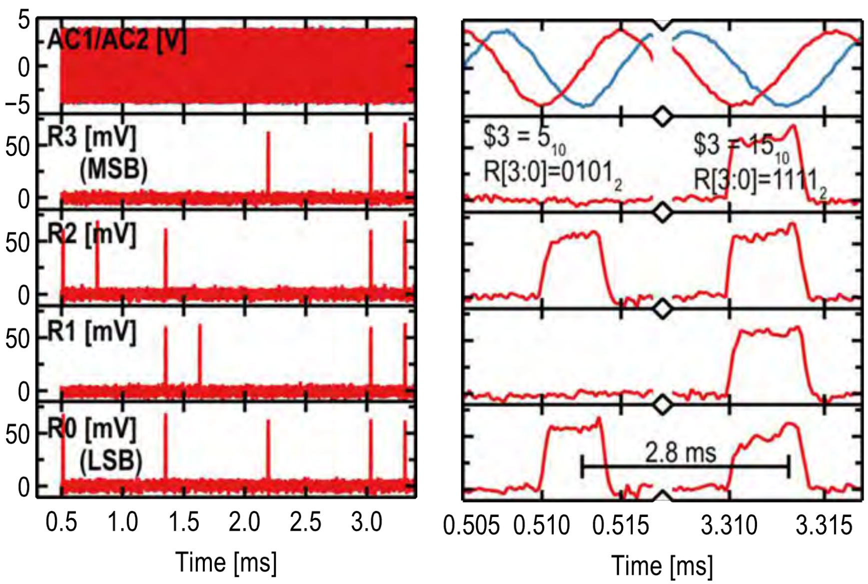
Execution of Test Program: add/sub + branch

(a) Full-waveform [0.5 ms to 3.4 ms] (b) Zoom-in of first and last result



(c) Test program 01

```
//Zero all reg with $0
//Set $1=0x1, $2=0x2, $3=0x3, $4=0x4…

//Main program loop
00: add $3, $2      //add 2 to $3
01: subnw $9, $3    //compare to 9 in $9
10: bneq 0x00       //if !zero, go to 0x00
11: add $3, $6      //add 6

//Check program
00: add $3, $0      //Check $3, expect 15
```

(d) Output sequence

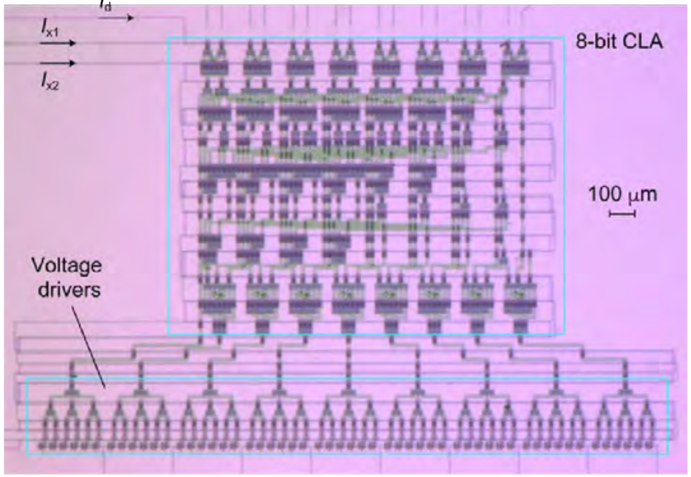
```
RES1: 0b0101  //1st add: $3 = $3+$2 = 5
RES2: 0b0100  //1st cmp: $9-$3 = 4
RES3: 0b0111  //2nd add: $3 = $3+$2 = 7
RES4: 0b0010  //2nd cmp: $9-$3 = 2
RES5: 0b1001  //3rd add: $3 = $3+$2 = 9
RES6: 0b0000  //3rd cmp: $9-$3 = 0
RES7: 0b1111  //Add 6: $3 = $3+$6 = 15
RES8: 0b1111  //Check: $3 = $3+$0 = 15
```

Test program successfully passes.

C. Ayala *et al.*, IEEE Journal of Solid-State Circuits, 2020

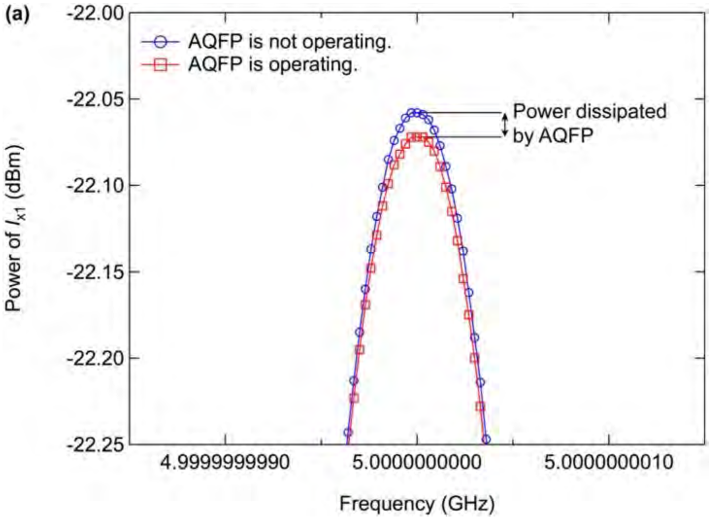
Measurement of Energy Consumption

8-bit AQFP Cary Look-ahead Adder



The total junction count: 1,638

Measurement of Power consumption @5 GHz



Energy consumption: 1.5 aJ/operation
~ 24 k_BT/junction

Fabricated by AIST HSTP

Takeuchi *et al*., APL 114 (2019) 042602

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Comparison of AQFP and FinFET Inverters

	AQFP	5 nm FinFET (FO3/FO4)	7 nm FinFET (FO3/FO4)
Power Supply	2 mA (AC) + 1 mA (DC)	0.45 V ~ 0.65 V	0.45 V ~ 1 V
Delay (ps)	~10 [1]	??~ 8.3	0.667 ~ 40
Switching Energy (fJ)	~1.4 x 10^{-6} @ 5 GHz	0.106 ~ 0.291	0.111 ~ 1.317

[1] N. Takeuchi *et al.*, *Appl. Phys. Lett.*, vol. 115, no. 7, p. 072601, Aug. 2019.

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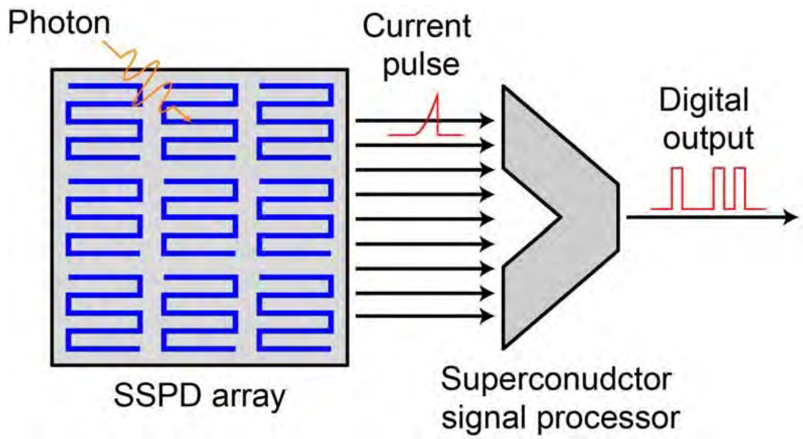
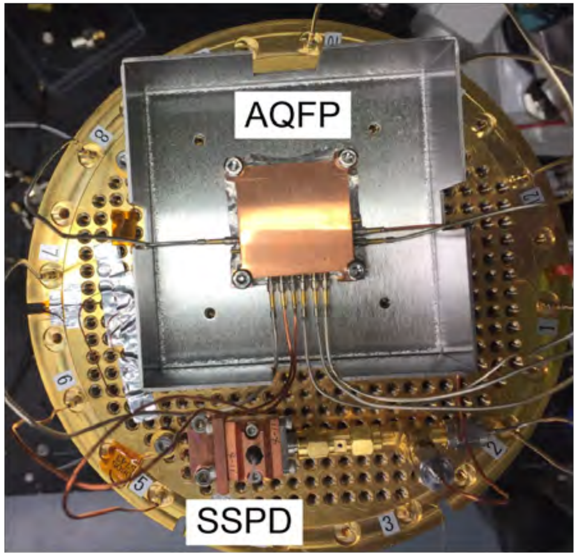
AQFP Readout Circuits for SSPD Arrays



- AQFP has high input sensitivity: ~1 μA @4.2 K
- The spatial information of an SSPD array is digitized and encoded by superconductor digital circuits for reducing # of cables.

N. Takeuchi *et al*., Opt. Express **25** (2017).

SSPD with AQFP readout circuits in a 0.1-W GM cryocooler



Sample-stage temperature: 2.4 K

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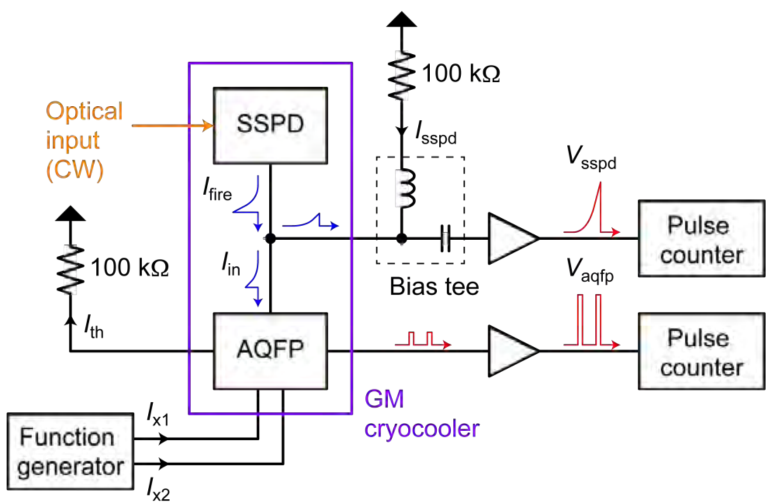
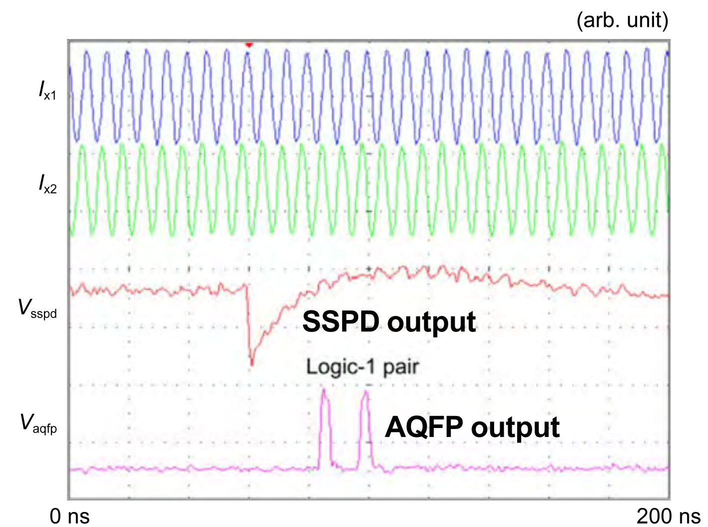
Measurement of a Single SSPD by AQFP Circuits

Measurement setup



Readout signal from SSPD and AQFP



- AQFP readout circuit generates a logic-1 pair for an input signal from SSPD.

N. Takeuchi *et al.*, IEEE TAS **29,** 2201004 (2019).

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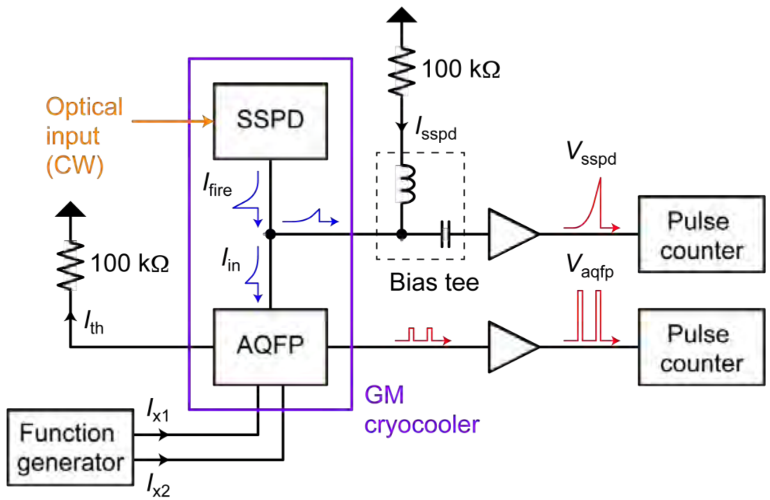
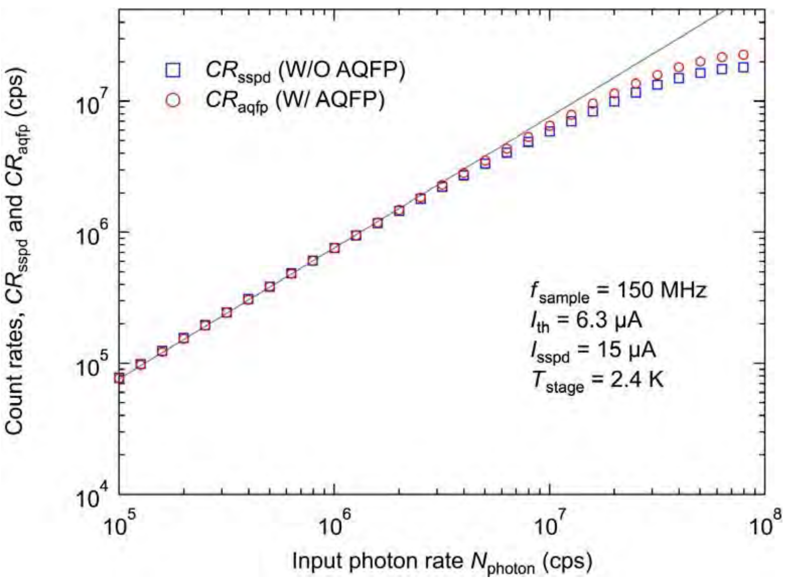
Measurement of a Single SSPD by AQFP Circuits

Measurement setup



Photon count rates w/ and w/o AQFP



- The count rate w/ AQFP agrees well with that w/o AQFP.

N. Takeuchi *et al.*, IEEE TAS **29,** 2201004 (2019).

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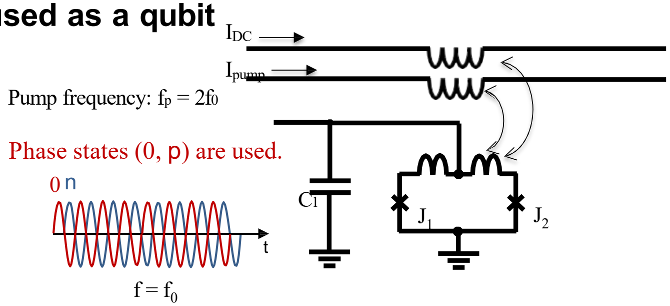
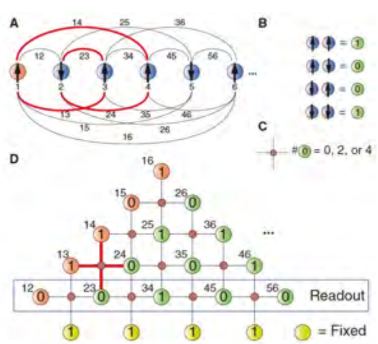
All-to-All Connected JPO Quantum Annealer

Josephson parametric oscillator (JPO) used as a qubit



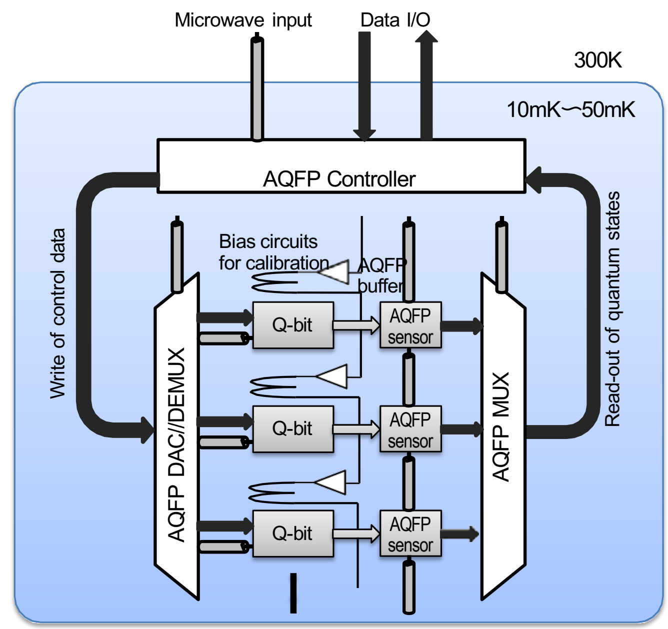
LHZ architecture for all-to-all connectivity



All-to-all connection can be formed by using four-bit unit cells with the four-body interaction. N(N-1)/2 physical bits are necessary to implement N logical bits.

Lechner, Hauke, Zoller Sci. Adv. 2015

Superconductor circuits are used as interface and controller



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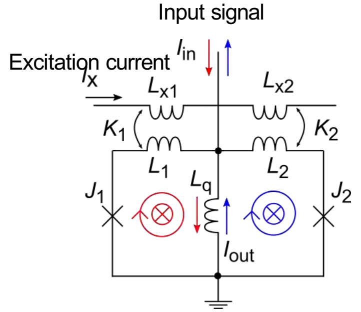
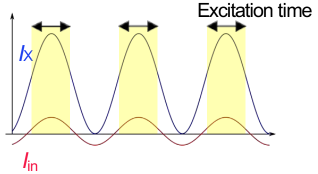
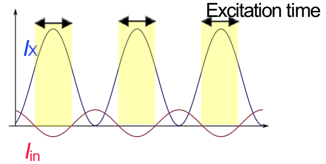
AQFP Readout Circuits for JPO Qubit



Input and excitation signal are in-phase ➔Output " 1 "

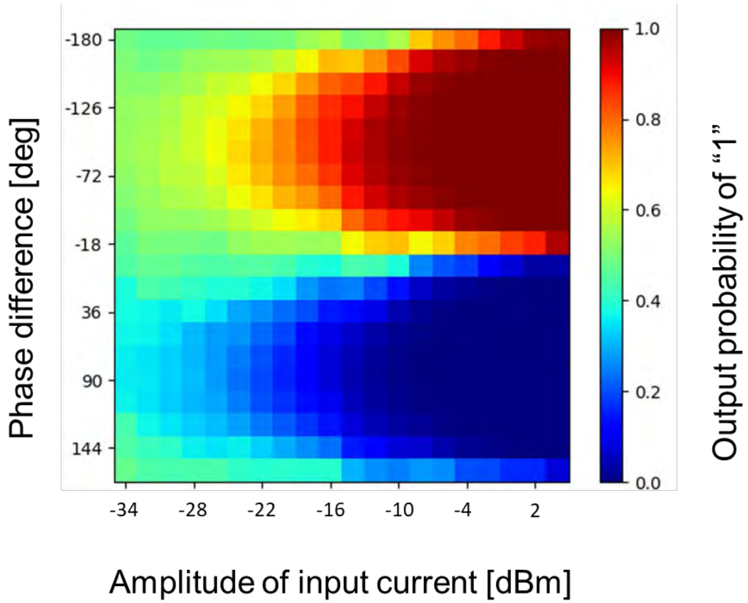


Input and excitation signal are out of phase ➔Output "0"



	Input sensitivity@1 GHz@4.2K
Simulation	0.085 μA
Experiment	0.326 μA

Phase readout characteristics at 1GHz



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Outline

- Background and motivation
- The minimum energy in computation?
  - Laudauer's principle
  - Adiabatic and reversible computing
- Adiabatic quantum flux parametron (AQFP)
- Present research activities of AQFP logic
  - High-performance computing
  - Readout circuit for a superconductor sensor array
  - Interface circuit for a quantum computer
- Reversible quantum flux parametron (RQFP)
- Summary

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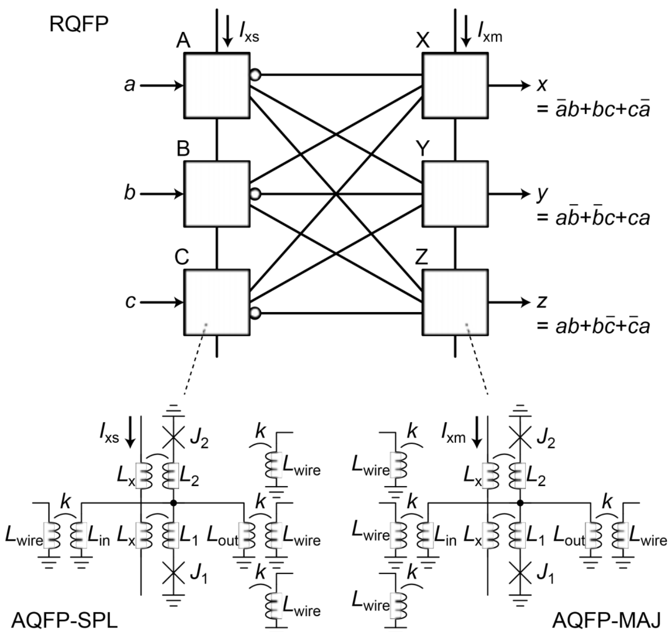
Reversible QFP (RQFP)

Reversible majority QFP gate



Truth table

Input			Output		
a	b	c	x	y	z
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Injective function

A logically and physically reversible gate can be realized by using Majority and Splitter gates.

N. Takeuchi, *et. al.*, *Scientific Reports* 4, 6354 (2014).

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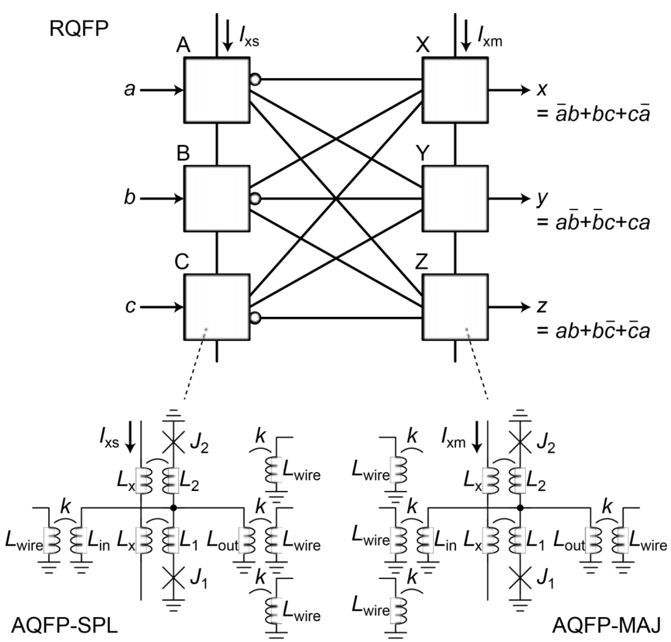
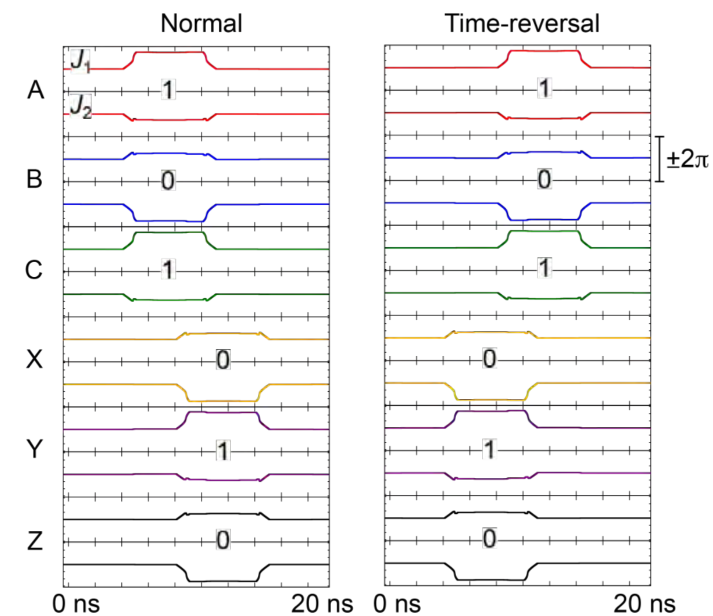
Physical Reversibility of RQFP

Reversible majority QFP gate



Time reversibility of junction phases



N. Takeuchi, *et. al.*, *Scientific Reports* 4, 6354 (2014).

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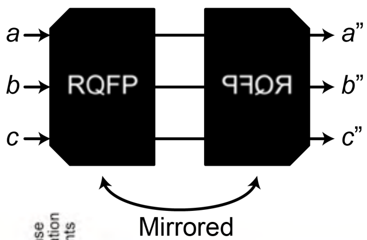
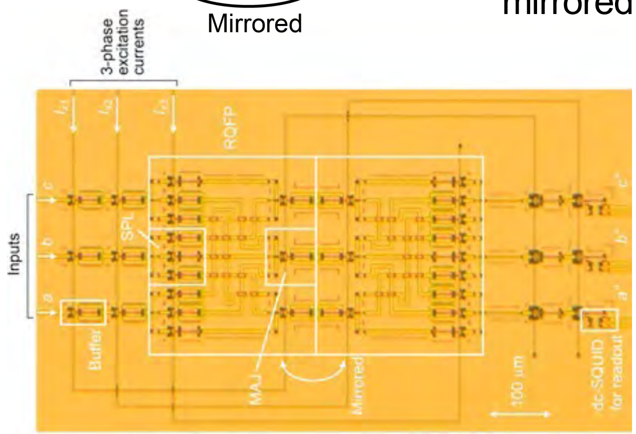
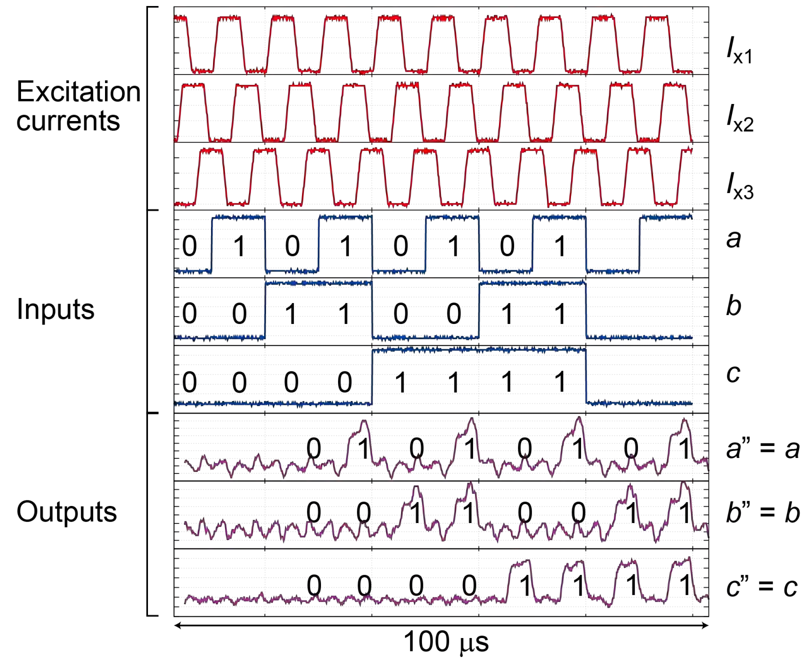
Demonstration of Physical Reversibility



- Two RQFP gates are serially connected, one of which is physically mirrored.





CRAVITY AIST

Fabricated by AIST STP2

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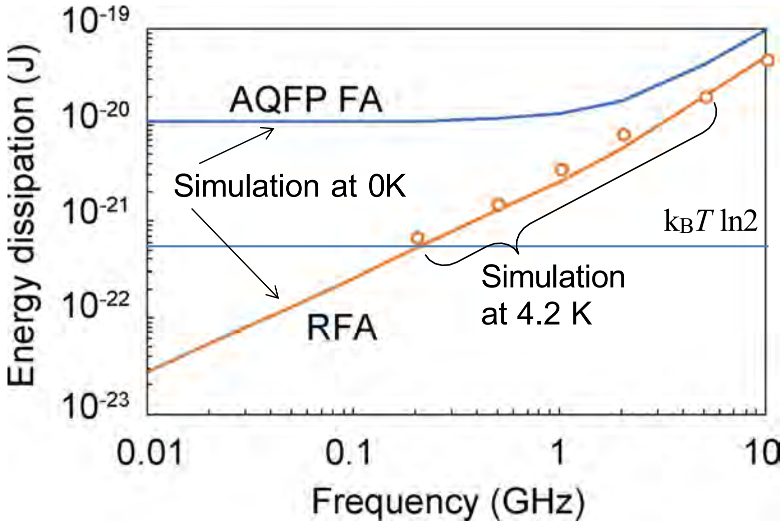
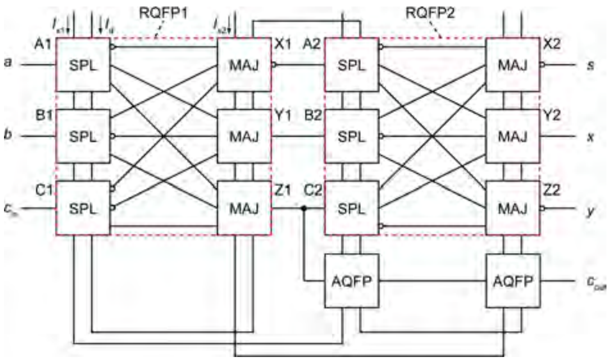
Energy Consumption of RQFP Full Adder

Calculated Energy dissipation of 1-bit full adder at T = 4.2 K



Schematic of 1-bit full adder

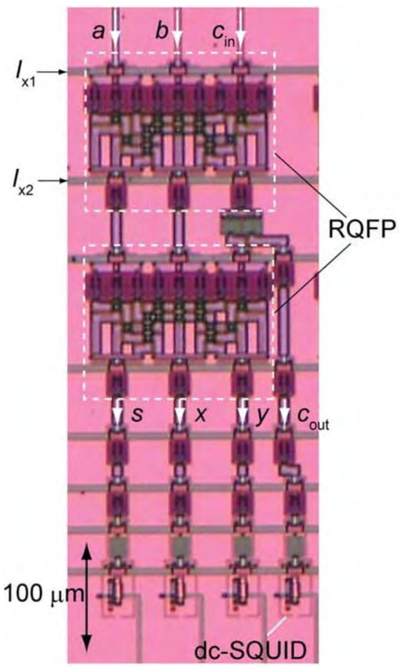


The total junction number: 28

Bit energy smaller than $k_B T\ln 2$ is possible in RQFP circuits.

T. Yamae *et al.*, *SUST,* 32, 035005 (2019).

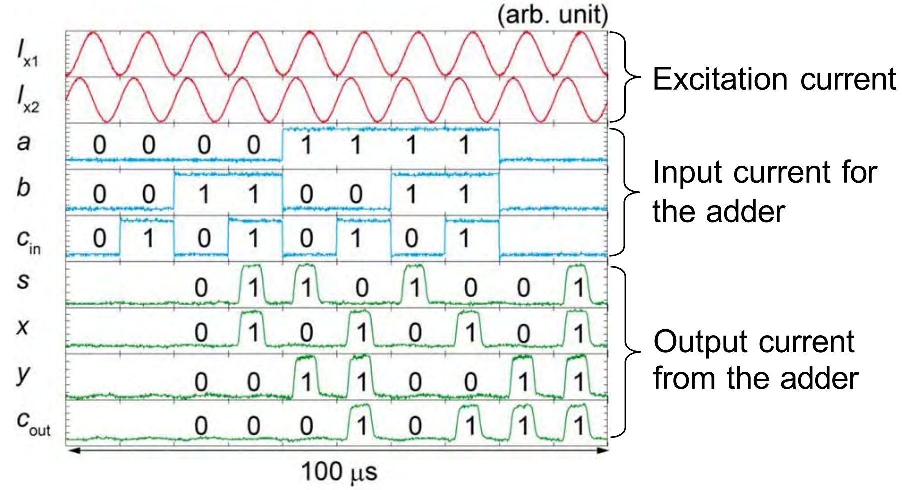
Demonstration of 1-bit RQFP Full Adder



Fabricated by AIST HSTP

T. Yamae *et al.*, *SUST*, 32, 035005 (2019).

Measurement results of 1-bit RQFP Full Adder at 4.2 K



Excitation current margins:
I_{x1} = 5.4 dB, I_{x2} = 6.1 dB

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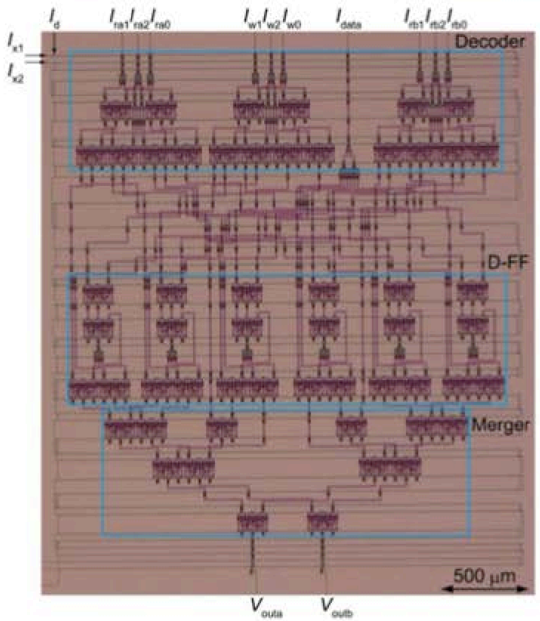
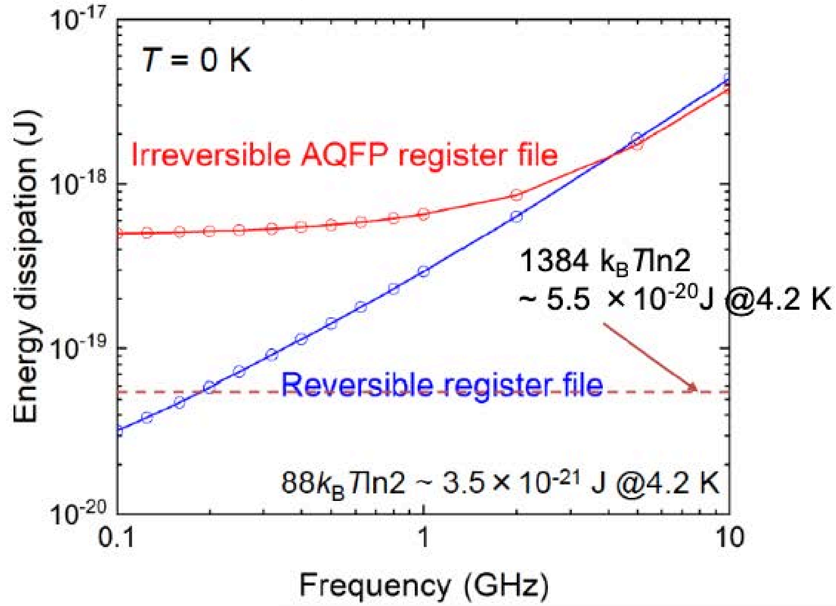
Demonstration of 8-Word by 1-bit RQFP Register File



Calculated energy dissipation of 8-word 1-bit register file at T = 0 K



CRAVITY AIST

T. Yamae *et al.*, ASC 2020

Number of junction: 1384
Number of garbage output: 88

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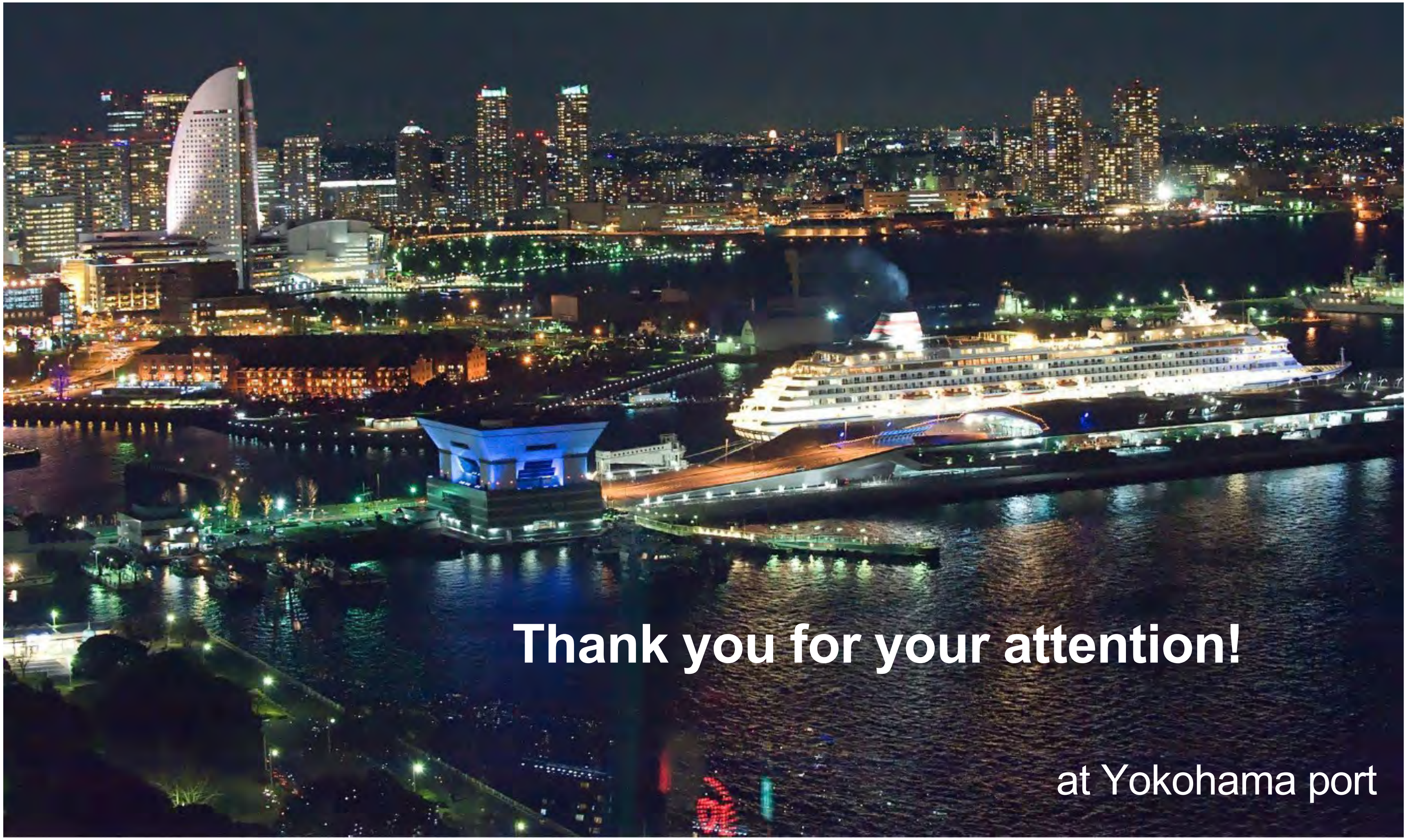
Summary

- The latest research status of superconductive integrated circuit technologies based on adiabatic flux quantum logic were presented.
- AQFP is extremely energy efficient logic.
    - More than 10^5 times less power than that of current CMOS.
- Current research activities using AQFP were introduced.
    - High-performance computers
    - Read-out circuits for superconductor sensor arrays
    - Control circuits for quantum computers
- More energy efficient logic is possible based on Reversible QFP.
    - Bit energy less than $E_{bit} = k_B T \ln 2$ is possible.


Thank you for your attention!
at Yokohama port