ASC 2022
StdP-E-03

60-GHz Single Flux Quantum Pulse Transfer Circuit for Serial Biasing

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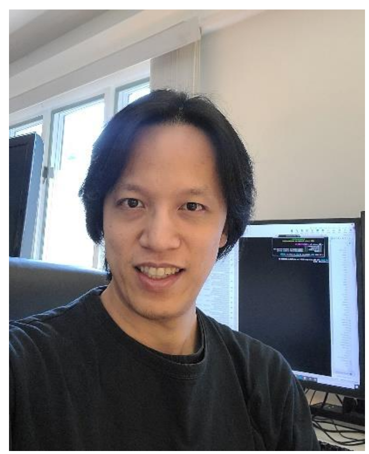

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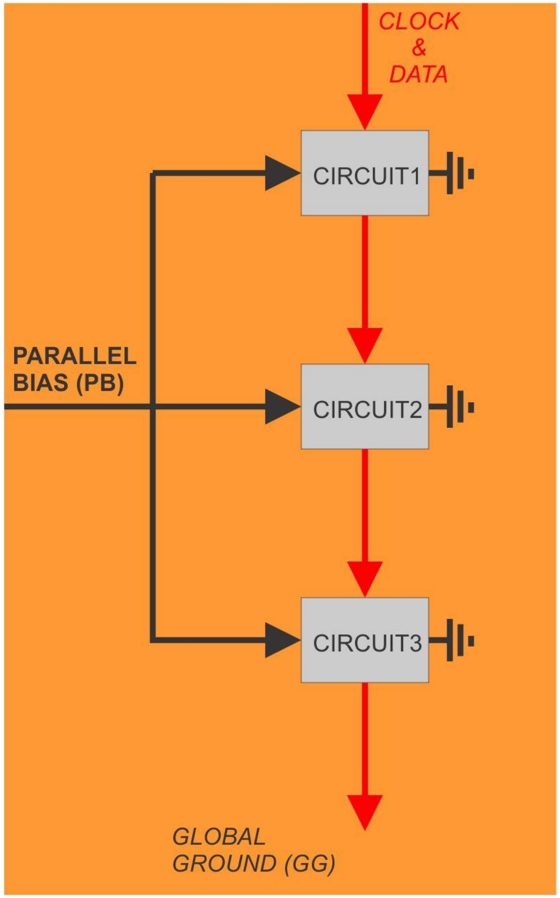
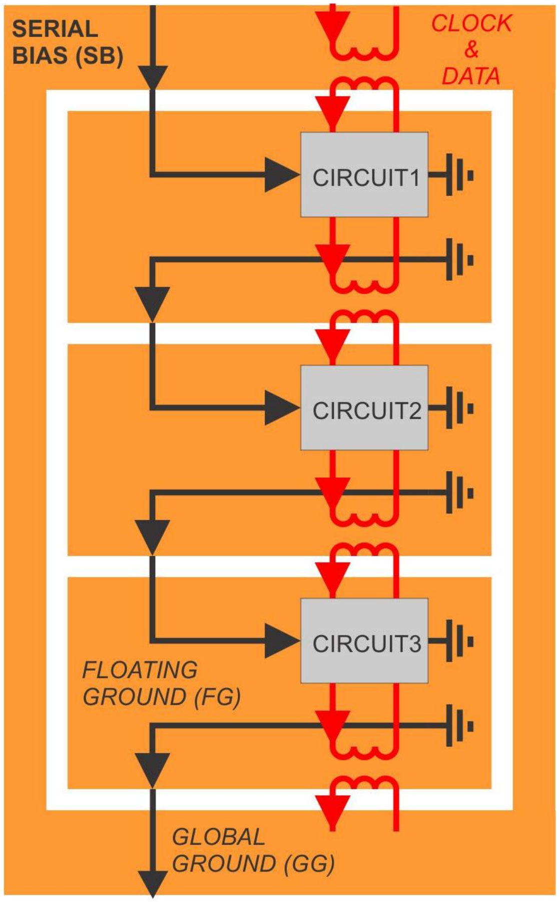
Parallel Bias (PB) vs Serial Bias (SB)

Parallel Bias (PB)



- **Parallel bias for circuit blocks**
- **Galvanic Connection for Clock and Data Pulses**

Serial Bias (SB)



- **Serial bias for circuit blocks**
- **Galvanic Isolation for Clock and Data Pulses**
- **$I_{SB}=I_{PB}/N$, N is number of islands**

Motivation and 2022 Results

- **Serial Biasing reduces**
  - **Number of bias current leads and associated heat load**
  - **The total bias current delivered to a chip and associated on-chip magnetic fields**
- **The new Grapevine (GV) Biasing Approach**
  - **3x3 matrix of 3-to-2 counters with BER<10^{-12} at 20GHz**
  - **A. Shukla et al, "Pulse interfaces and current management techniques for serially biased RSFQ circuits," TAS 2022, Art #1300407**
- **Adaptation of the recent results to the RSFQ/ERSFQ standard cell library as a part of the SuperTools program led by IARPA**
  - **4-island test structure for SuperTools cell library, BER<10^{-12} at 50GHz**
  - **A. Shukla et al, "Serial biasing technique for electronic design automation in RSFQ circuits," ASC'22, 4EPo1B-01**
- **In this work we address Driver-Receiver Pair (DRP) design, test and simulation results**

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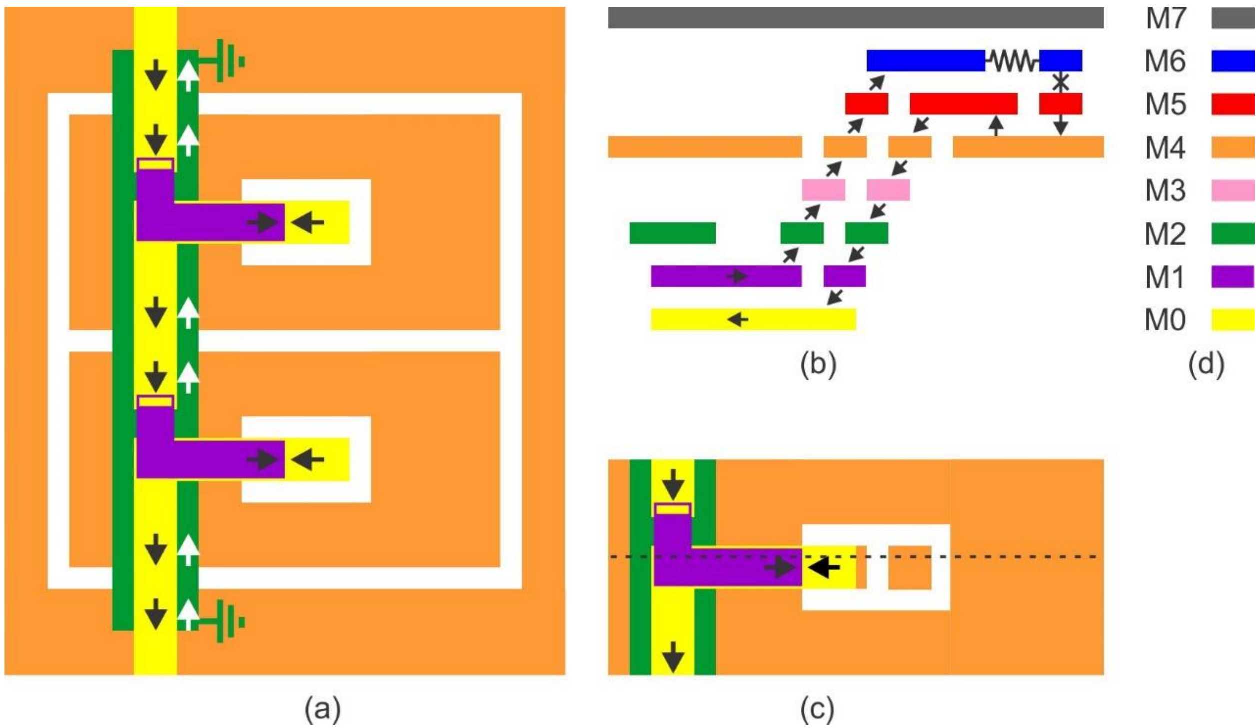
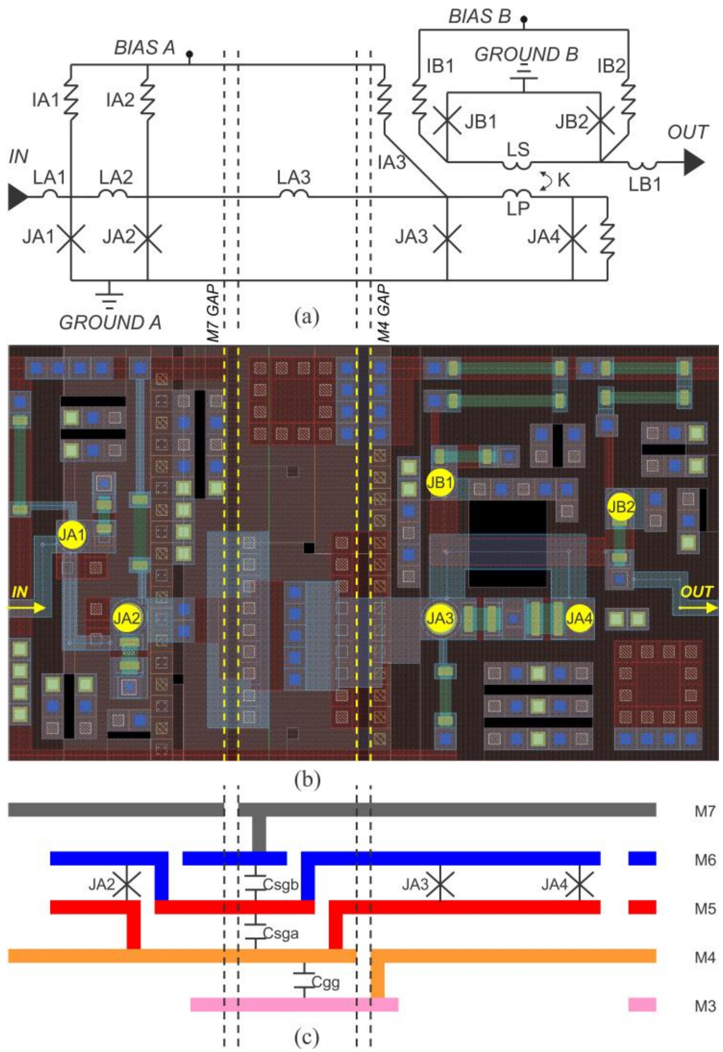
Grapevine Biasing Approach



- Any metal layer to carry “current in” has a dedicated metal layer to carry “current out”
- These metal layers are always placed above each other to localize magnetic fields in between

The metal layers stack (b) is given for 100μA/μm² SFQ5ee fab node at MIT-LL.

DRP: Schematic, Layout, and Cross-section

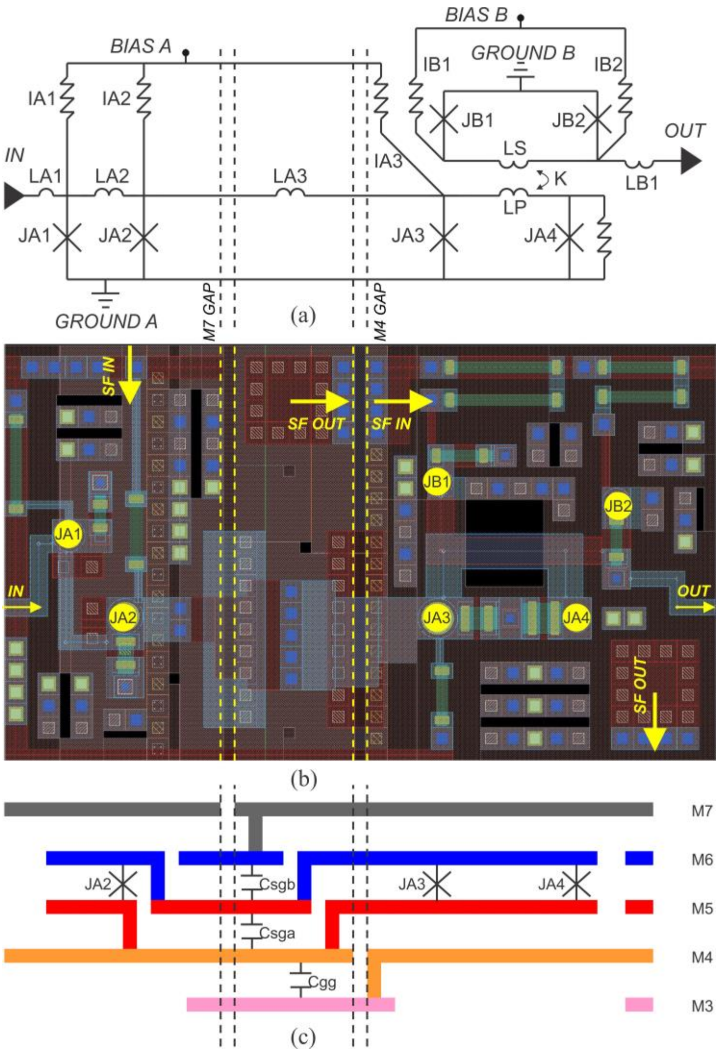


Key layout features are

- M5 “tongue” [1]
- Staggered M4 and M7 ground moats [2]
- Additional layers used to shield ground moats [2]

[1] M. W. Johnson et al., IEEE Trans. Appl. Supercond., vol. 13, no. 2, pp. 507-510, Jun 2003.
[2] V. K. Semenov and Y. Polyakov, IEEE Trans. Appl. Supercond., vol. 29, no. 5, Aug 2019, Art no. 1302304.

DRP: Schematic, Layout, and Cross-section



Straightforward (SF) current flow

The metal layers stack (c) is given for 100µA/µm² SFQ5ee fab node at MIT-LL.

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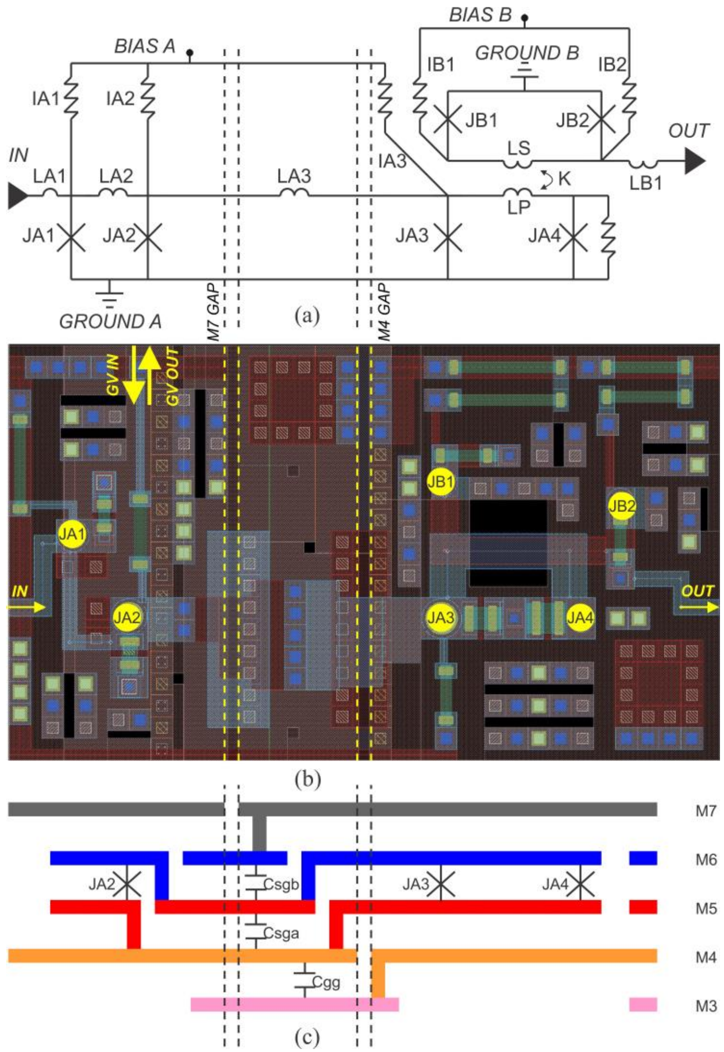

Grapevine (GV) current flow

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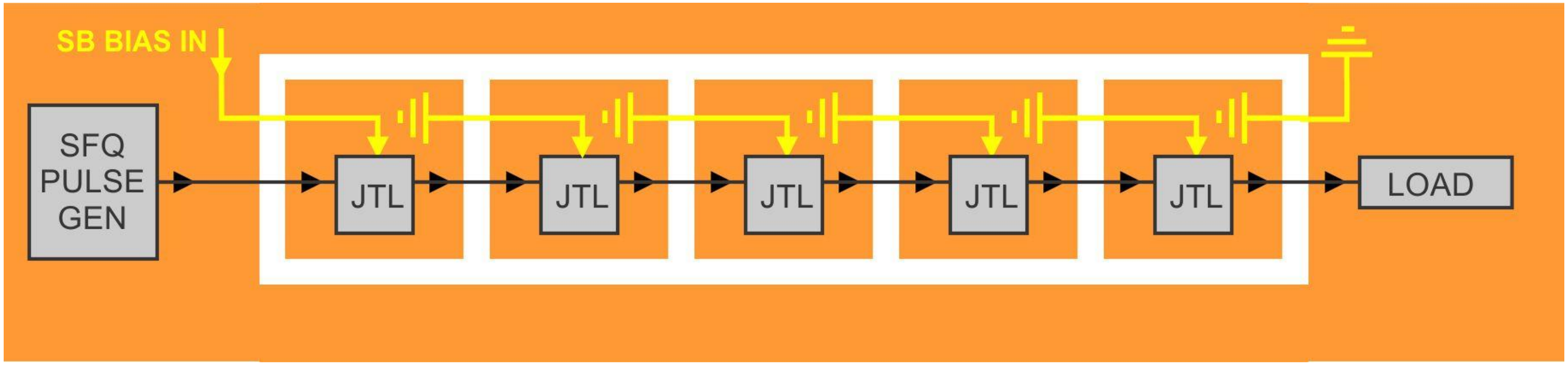
Simulating the Driver Receiver Pair (DRP)

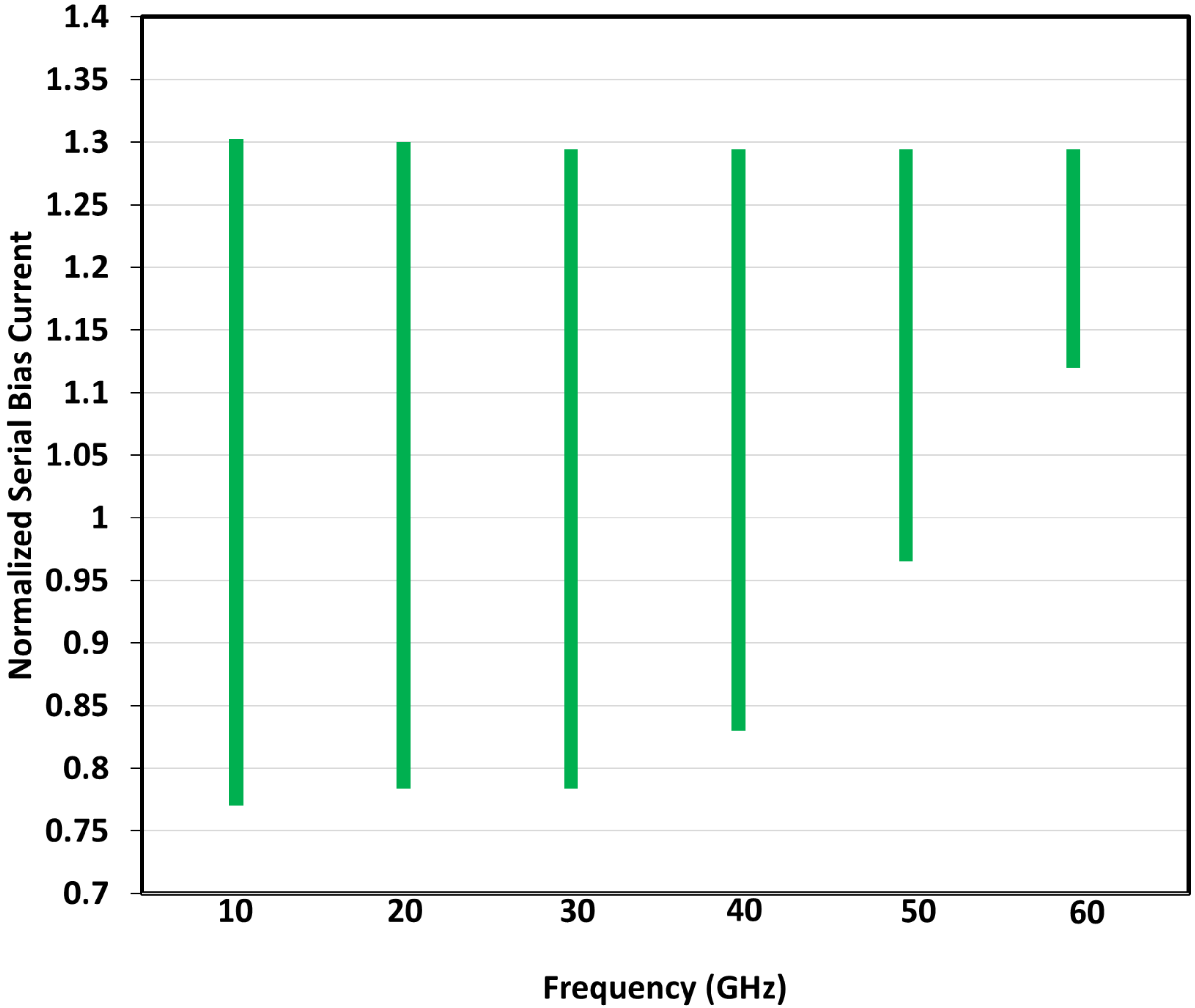


PSCAN [1] and Cadence Spectre [2] used for circuit simulation and optimization

[1] S. Polonsky, et al., IEEE Trans. Appl. Supercond., vol. 7, no. 2, pp. 2685-2689, Jun 1997.

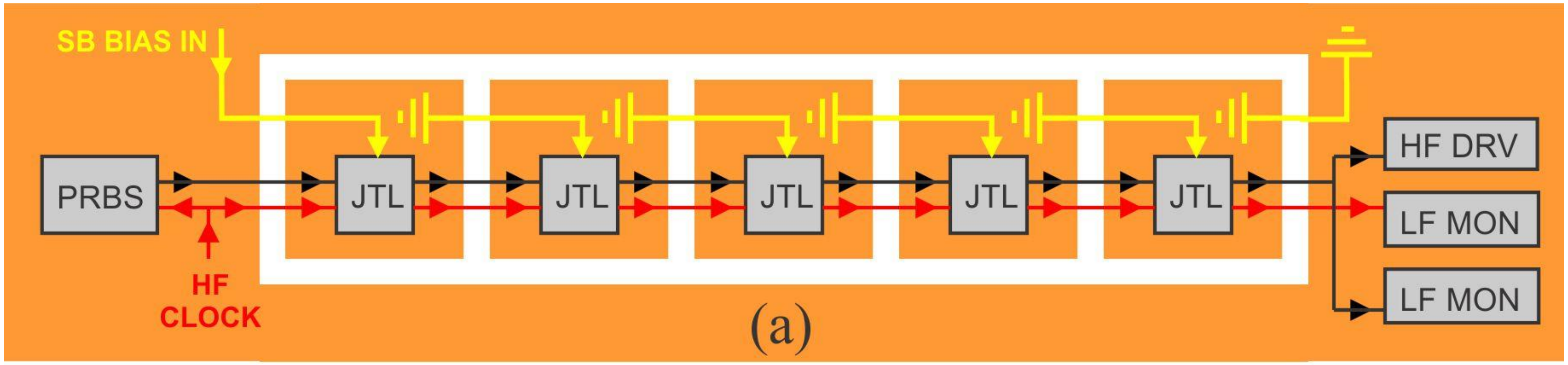
[2] A. Inamdar, J. Ren and D. Amparo, IEEE Trans. Appl. Supercond., vol. 25, no. 3, Jun 2015, Art no. 1300308.

Simulating the Driver Receiver Pair (DRP)

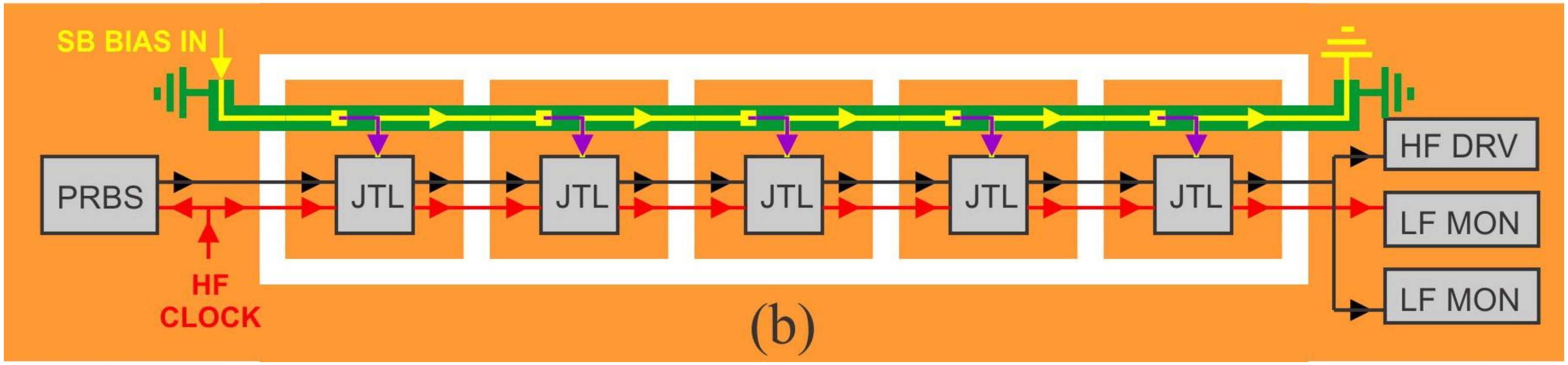


- ±25% margins up to 30 GHz
- Lower-end of margins shrinks starting 40 GHz

Five Islands Test Structure: SF vs GV



(a) DRP testbed with straightforward (SF) biasing



(b) DRP testbed with grapevine (GV) biasing

- **3.2 mA bias current required**
- **Pseudo Random bit Sequence (PRBS) circuit produces random data with 127-bit periodicity**

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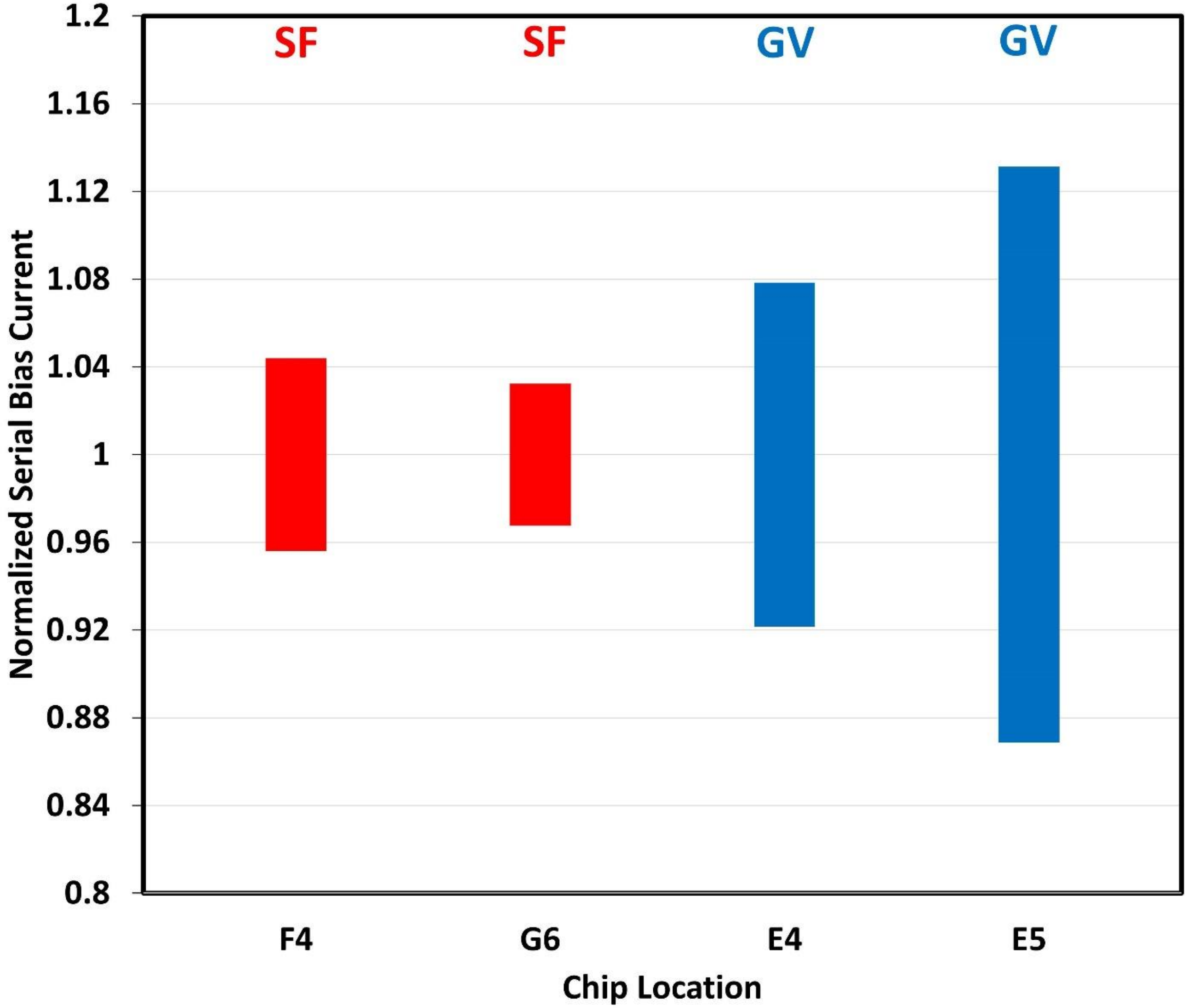
Low Frequency (LF) Test Results (SF vs GV)



Straightforward Biasing: ±4% **Grapevine Biasing: ±8%**

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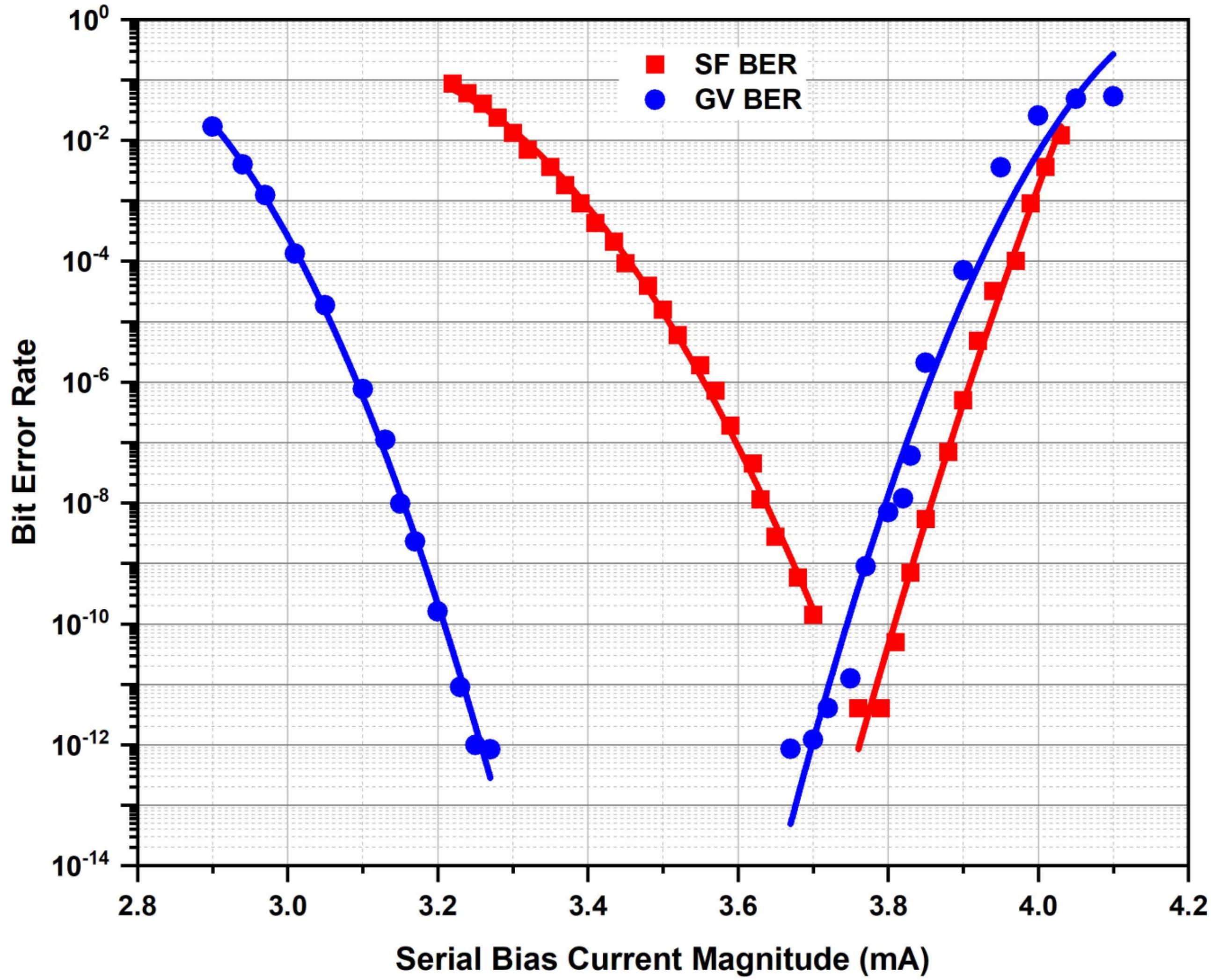
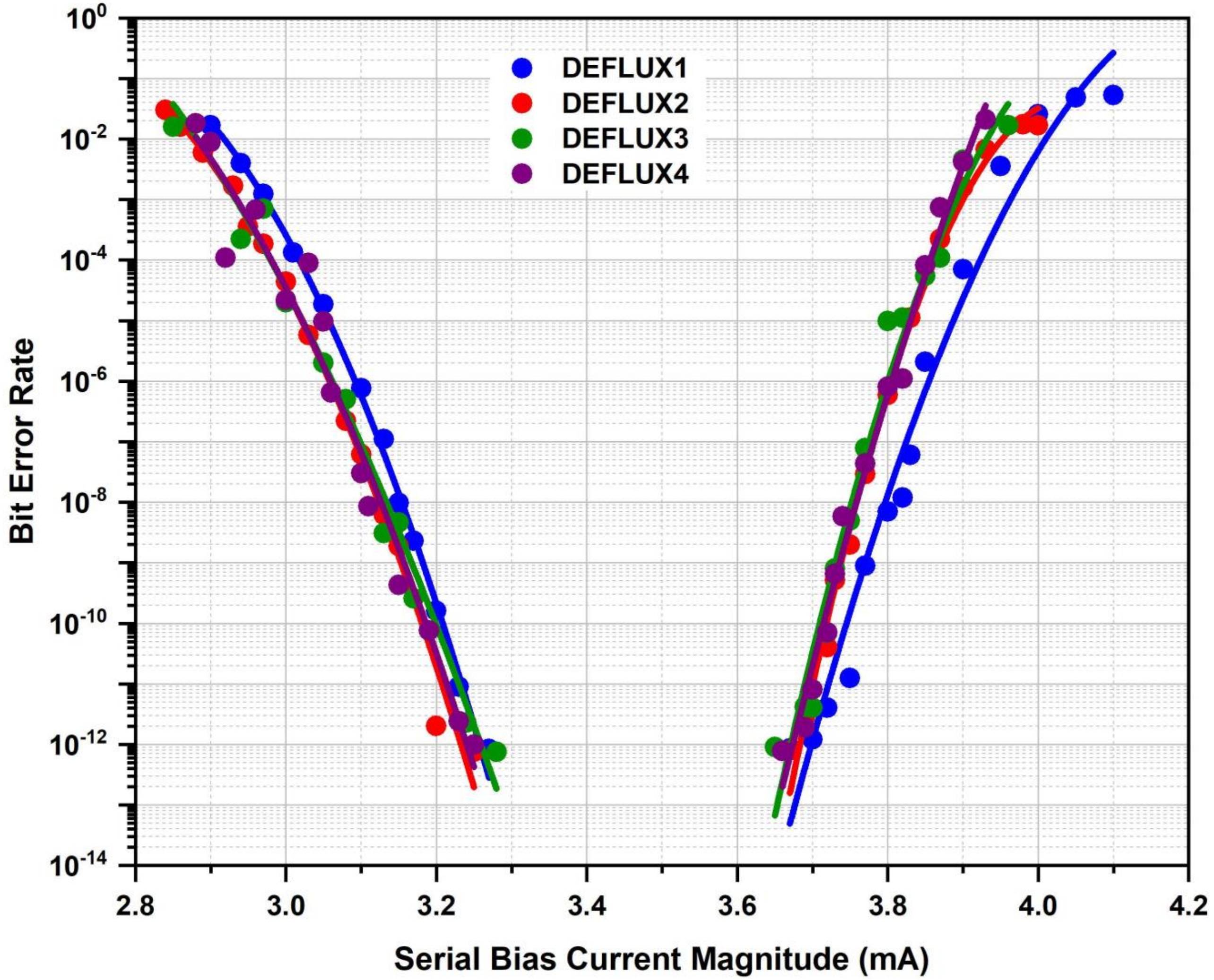
BER vs Serial Bias Current at 10.16 GHz for SF vs GV



- @BER = 10^{-12}, margins for straightforward biasing : ±0%
- @BER = 10^{-12}, margins for grapevine biasing : ±5.8%

BER vs Serial Bias Current at 10.16 GHz after 4 Defluxes (Grapevine Biasing)



Grapevine biasing results in repeatable margins across multiple defluxes

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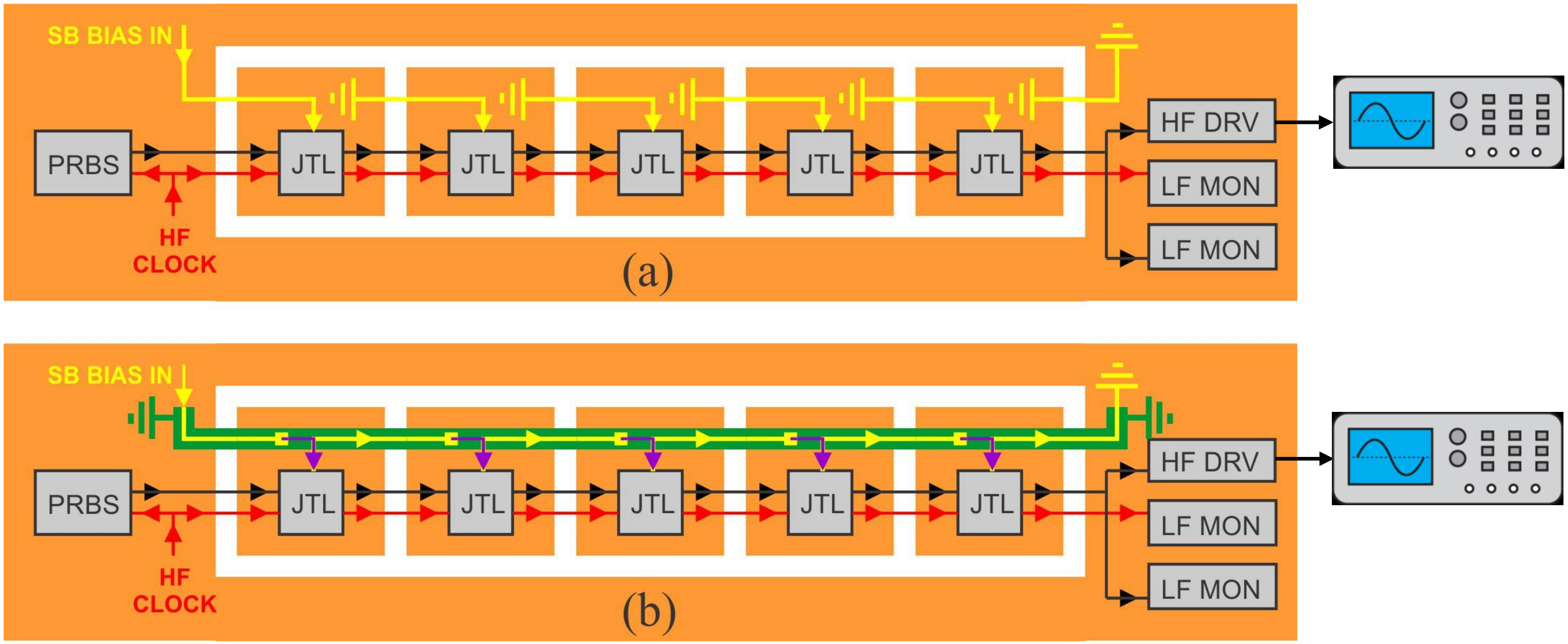
Waveform Stability Test up to 60 GHz



- T-Flip-Flop precedes the HF driver
- High sensitivity to missed or added pulse

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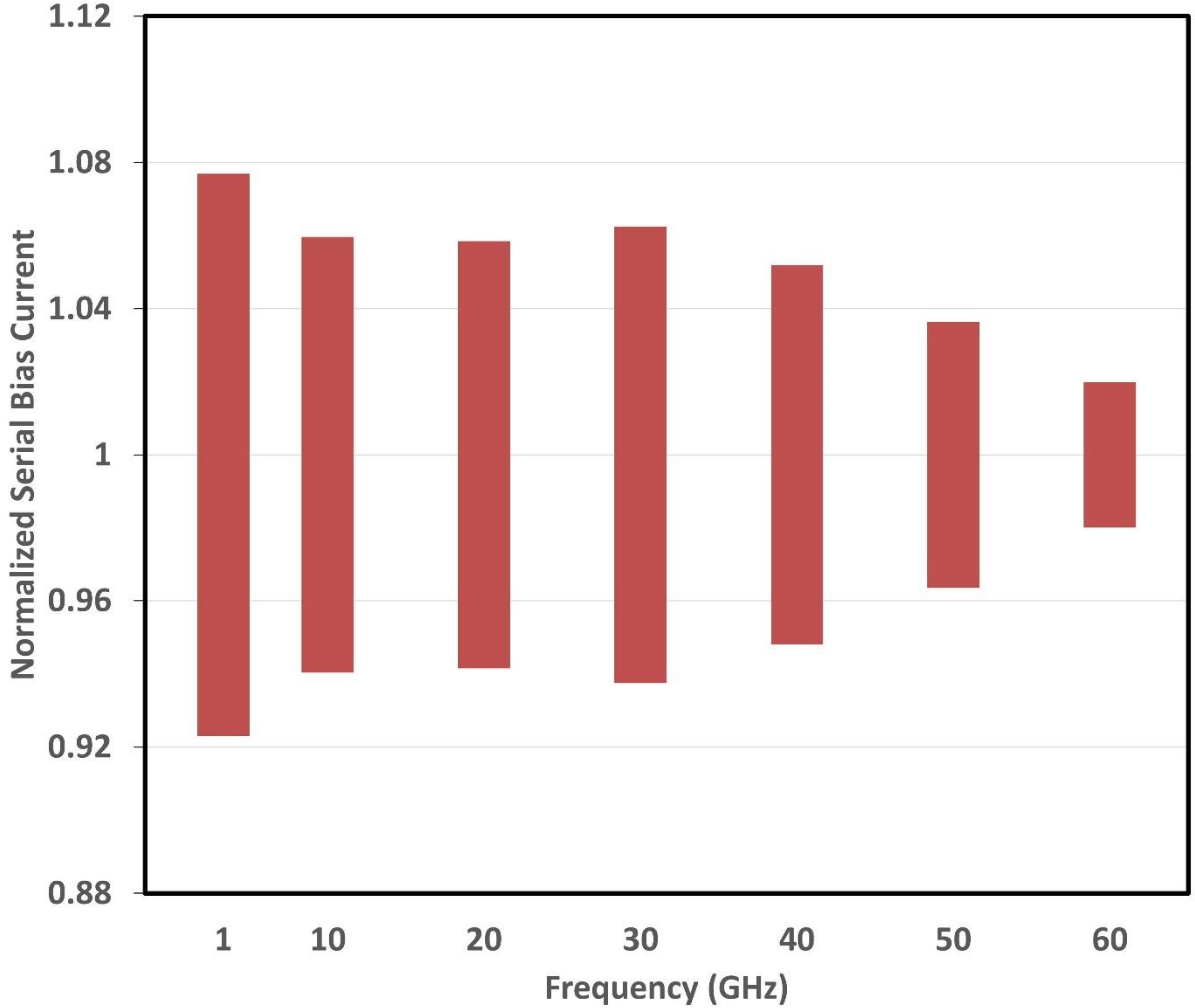

DRP testbed with grapevine biasing has ±5% margin at 40 GHz and is operational up to 60 GHz

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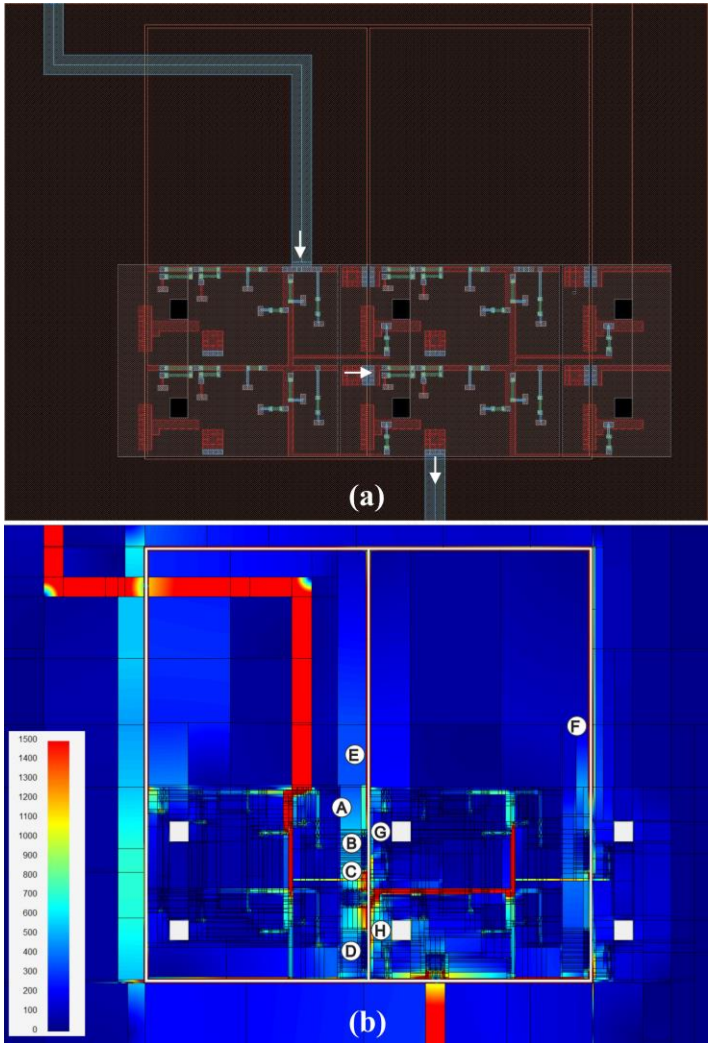
Sonnet-Based EM Simulations: SF Biasing



- A
- B
- C
- D

Proximity to signal inductors

- E
- F

Proximity to ground moat

- G
- H

Proximity to transformer hole

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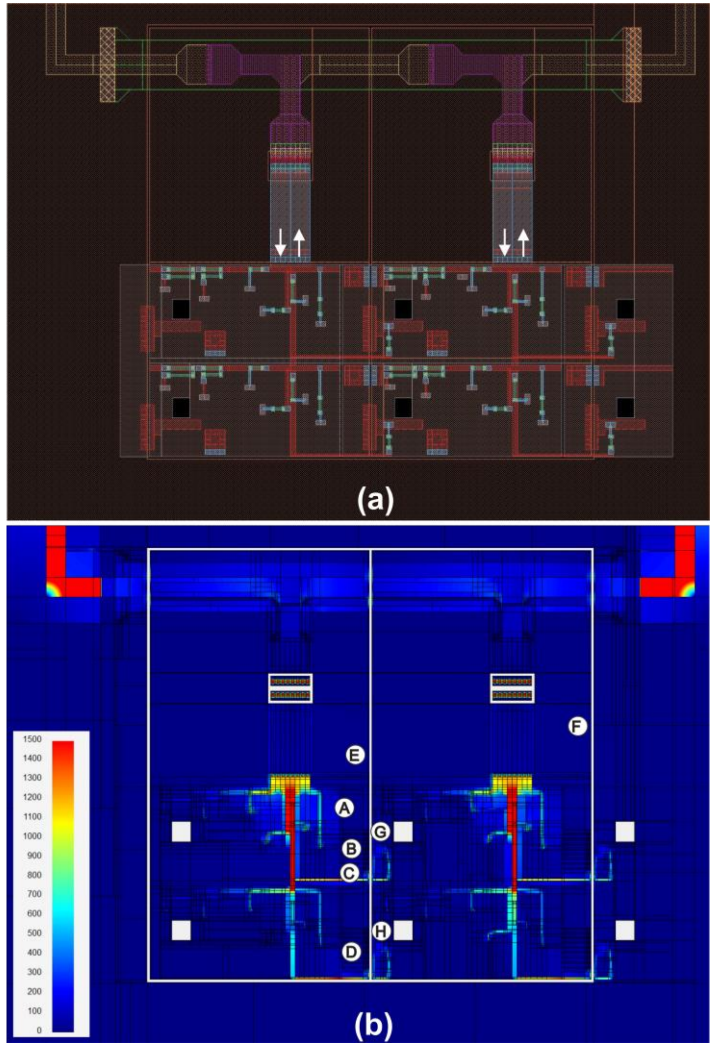
Sonnet-Based EM Simulations: GV Biasing



- A
- B
- C
- D

Proximity to signal inductors

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Comparing M4 densities for SF and GV Biasing

Location	SF Current Density (A/m)	GV Current Density (A/m)	Ratio SF/GV
A	620	40	15.5
B	600	40	15.0
C	1600	40	40
D	260	40	6.5
E	3300	35	94.3
F	2400	35	68.6
G	120	20	6.0
H	510	20	25.5

- **Straightforward biasing has M4 current densities 6-100 times greater than in case of grapevine biasing**
- **Grapevine biasing results in well behaved M4 current distribution**

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Conclusions

- We designed a driver-receiver pair (DRP) for serially biased RSFQ circuits and tested it up to 60 GHz with a BER of 10^{-12}
- We show that the grapevine technique must be used even for bias current values on the scale of 1 mA
- We proved that the grapevine biasing scheme helps improve the circuit margins
- The test results are confirmed by EM simulations

Acknowledgment

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Thank You!

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