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Experimental Investigation of ERSFQ Circuit for Parallel Multibit Data Transmission

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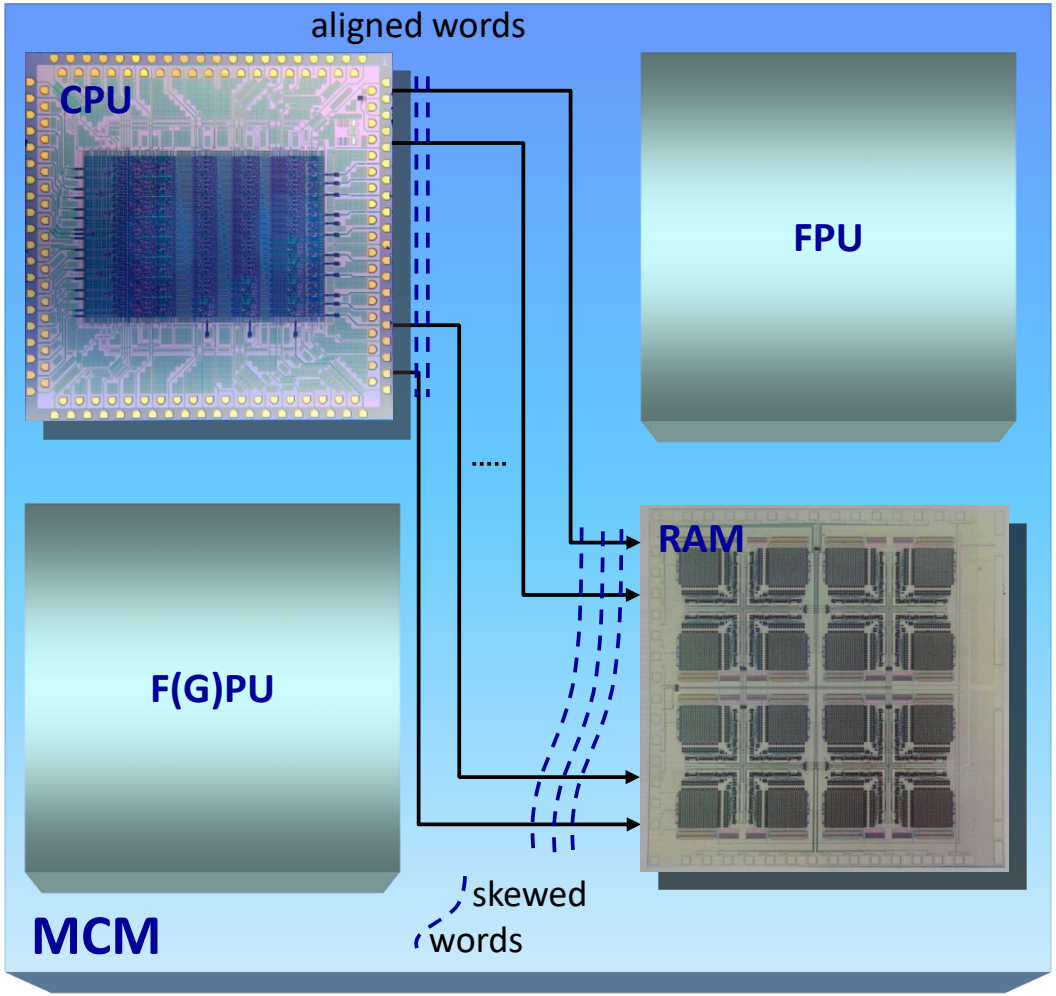
Motivation

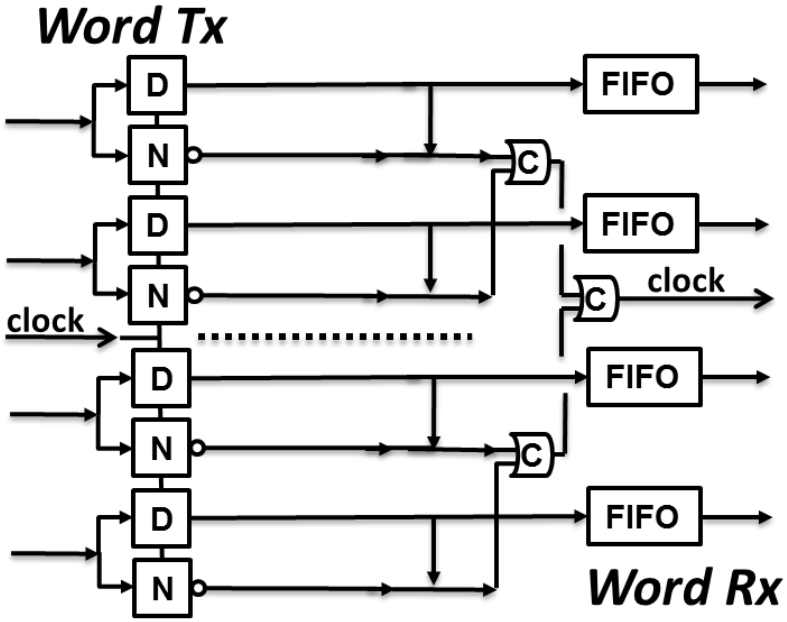


- Transmitting parallel data over long distances is a challenging task complicated by
  - 64-bit words
  - Chip-to-chip transmission with chips mounted on MCM
  - High >1 GHz clock rate
- There is inevitable word misalignment during transmission due to design/fab imperfections
- Digital data words have to be aligned
- Clock has to be recovered

8-bit, 20 GHz ALU: T. Filippov, A. Sahu, A. Kirichenko, I. Vernik, M. Dorojevets, C. Ayala, and O. Mukhanov, *Physics Procedia* 36, pp. 59-65, 2012
4-kbit VT memory RAM: S. Nagasawa, Y. Hashimoto, H Numata, and S. Tahara, *IEEE TAS*, 9 (2), p. 3708, 1999

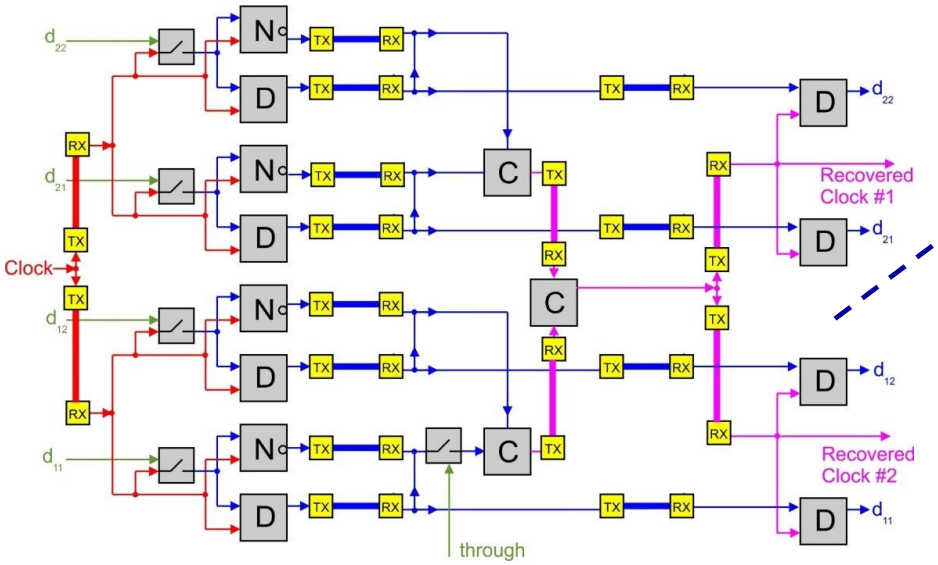
Design Approach

Long distance clock-recovery scheme for SFQ ballistic transmission

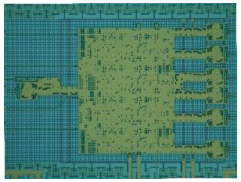


- At the Tx side the data are converted and transmitted in true or complementary form by D-cells and NOT gates
- At the Rx side, all channels are combined by tree of C-elements to restore “all-channel” clock for each word

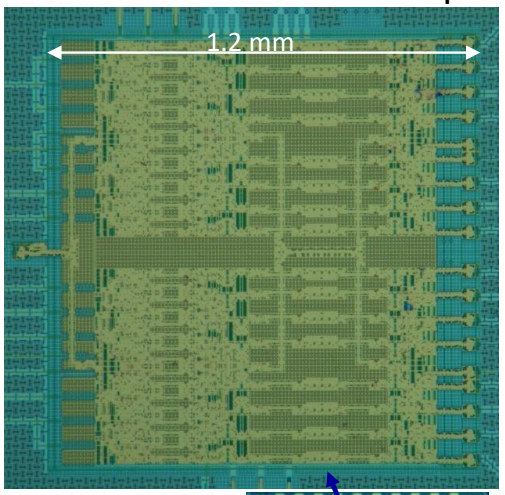
Layout: on-chip version

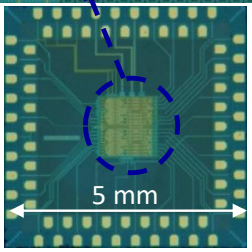


4-bit version of the circuit



16-bit version of the circuit laid out at 5x5 mm^2 chip





- Three versions of the ERSFQ circuit with increased complexity are designed
  - 4-bit, 8-bit, and 16-bit
- Data is generated by applying clock pulses to dc-switches
- 16-bit ERSFQ circuit comprises of >3200 JJs with signal distribution over JTLs and PTLs
- Single bit depth FIFO – D flip-flop
- Laid out for MIT-LL SFQ5ee process

Experimental results: on-chip version

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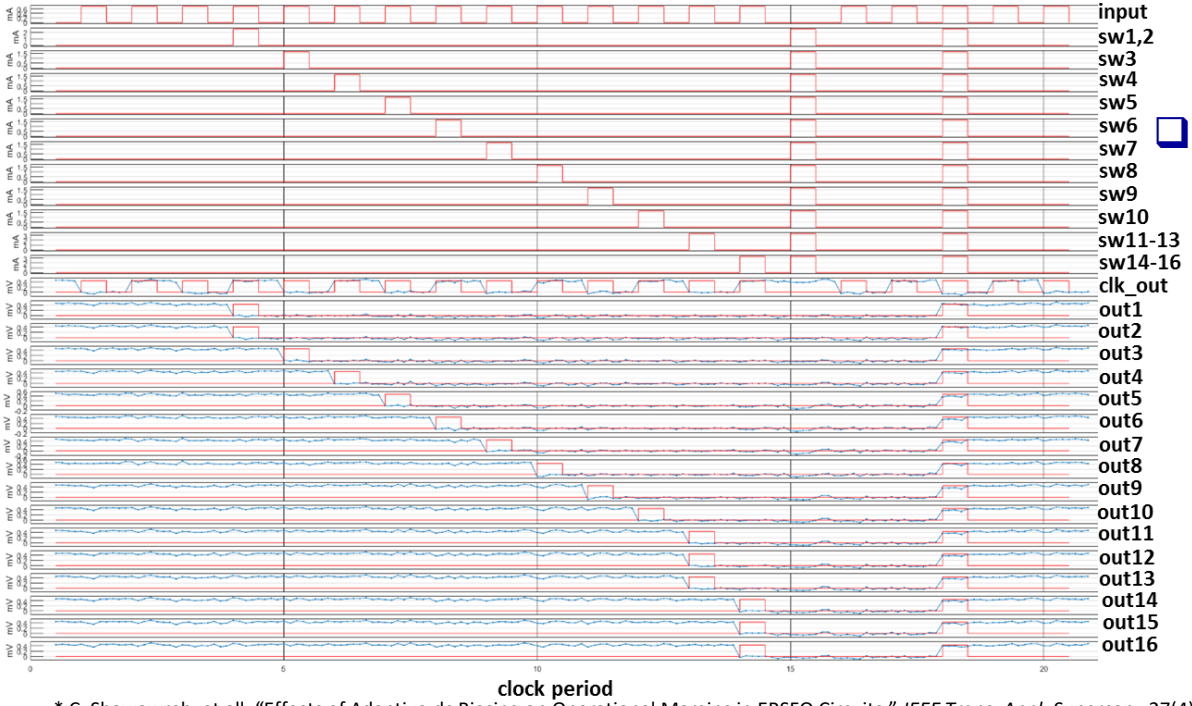
- Typical bias margins for on-chip ERSFQ communication circuits

	4-bit	8-bit	16-bit
Ic (mA)	33.55	119.7	350
Bias low (mA)	26	110.5	299
Bias high (mA)	42.5	140	414
Full margins (+/- %)	24.1	11.8	16.1
EE margins (+/- %)*	12.7	4	7.9



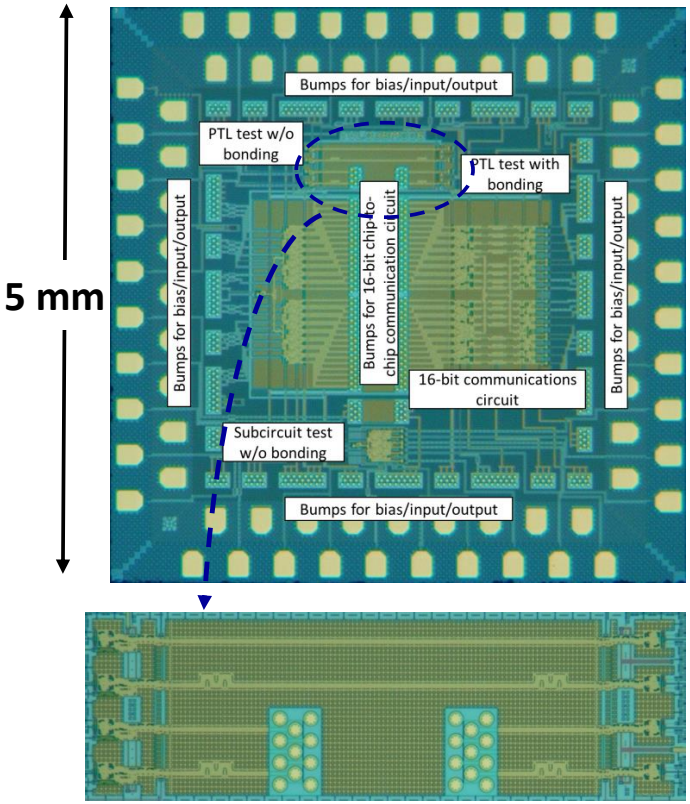
- Functionality test of the on-chip ERSFQ 16-bit communication circuit

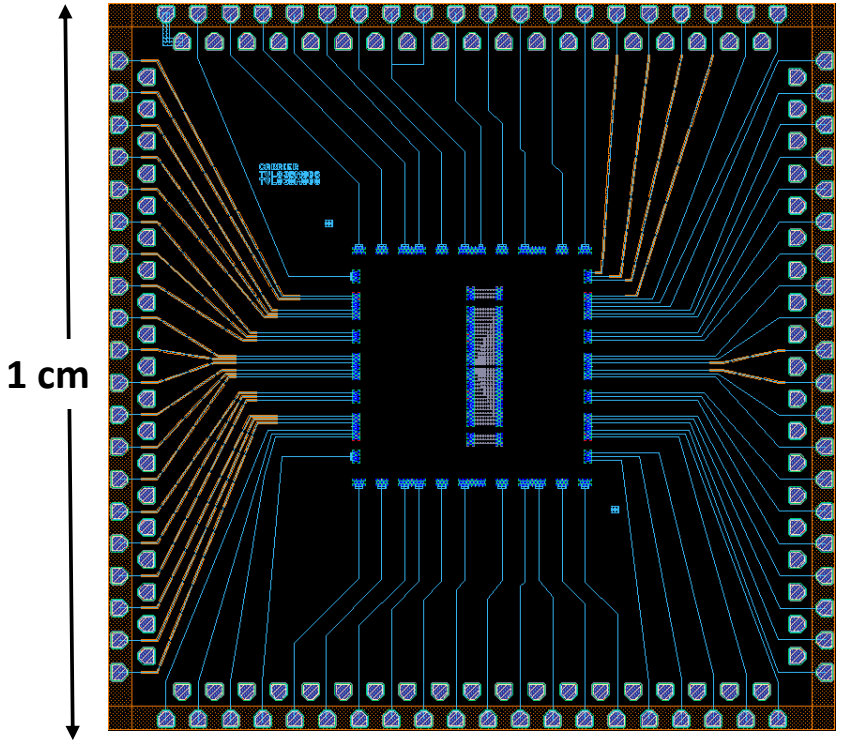
* C. Shawawreh, et all, "Effects of Adaptive dc Biasing on Operational Margins in ERSFQ Circuits," *IEEE Trans. Appl. Supercon.*, 27(4), 1301606, June 2017.

Layout: chip-to-chip version

- Fabricated at MIT-LL
- 16-bit circuit comprises of 3464 JJs with signal distribution over JTLs, PTLs & MCM bumps

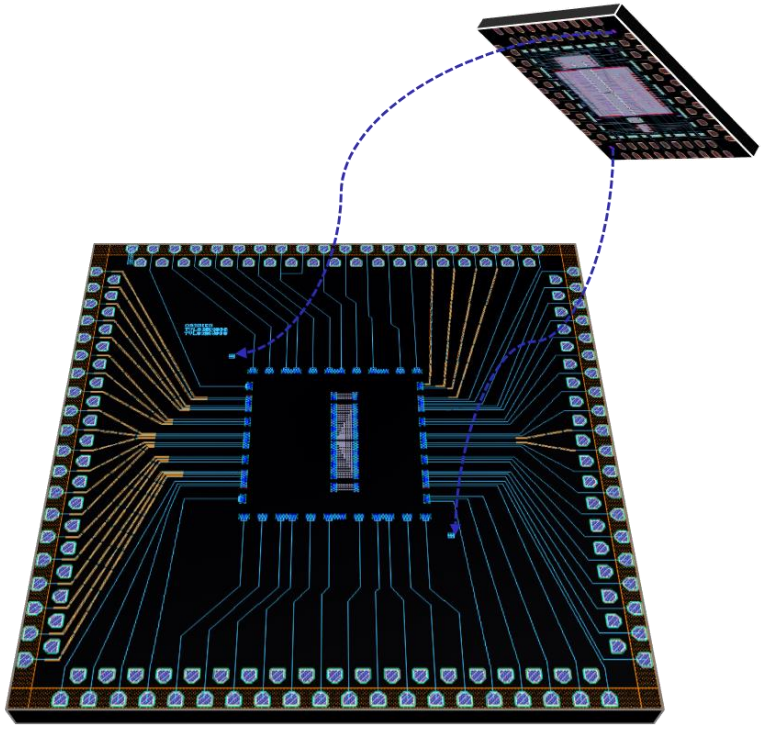
- Fabricated at Hypres
- Passive carrier (no JJs)

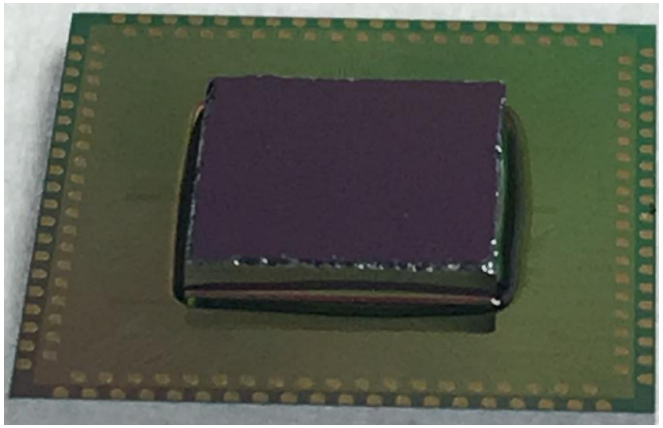




- MCM bumps with 50 μm pitch
- Example of test structures: PTLs w/o and with bonding

MCM assembly





- The MCMs are assembled using Hypres' epoxy- assisted Cu bumps technology
  - The bumps are designed with diameter of 15 µm and pitch of 50 µm.
  - 100% connectivity for 220 signal bumps (each surrounded by 4 GND bumps).

MCM results: test structures

Flip-chip test structure	Goal(s)	Test results
Single bumps connected to ground	1. To measure current when bias through the bump makes Nb non-superconducting 2. To measure bump resistance	1. ~150mA 2. 0.1-0.15 ohm
Series of 6 bumps	1. To evaluate fidelity of HYPRES MCM assembly 2. To measure bump resistance	1. 100 % connectivity 2. 0.1-0.15 ohm
Arrays of unshunted JJs	To I-V curves measured on-chip and via MCM	I-V curves measured on-flip-chip and via MCM are very similar.
Two PTL structures	To test how SFQ transmission through bumps affects the margins for PTL transmitter (Tx) and receiver(Rx)	Rx margins are unchanged while Tx margins are slightly worse: on-chip 0-7.1 mA; via MCM 0-5.7 mA

MCM with 16-bit communication circuit: functionality test

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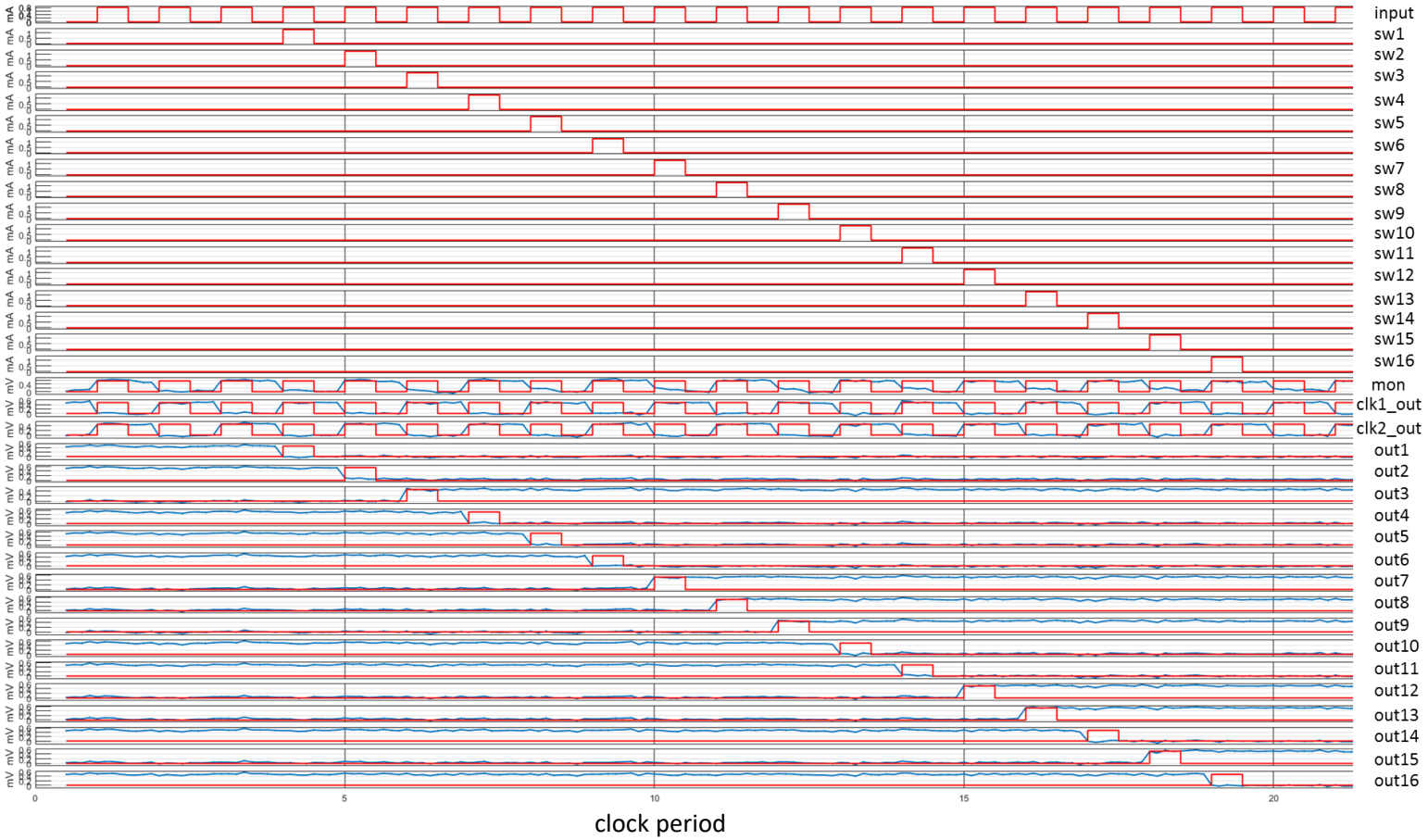

- Non-repetitive test patterns
  - Bias margins (+/- 12%) – similar to the on-chip version of the same circuit

MCM with 16-bit communication circuit: high speed test

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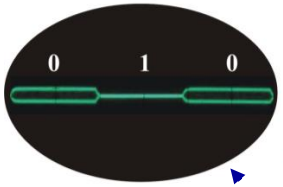
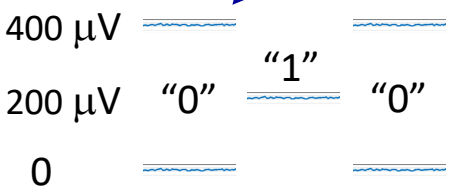
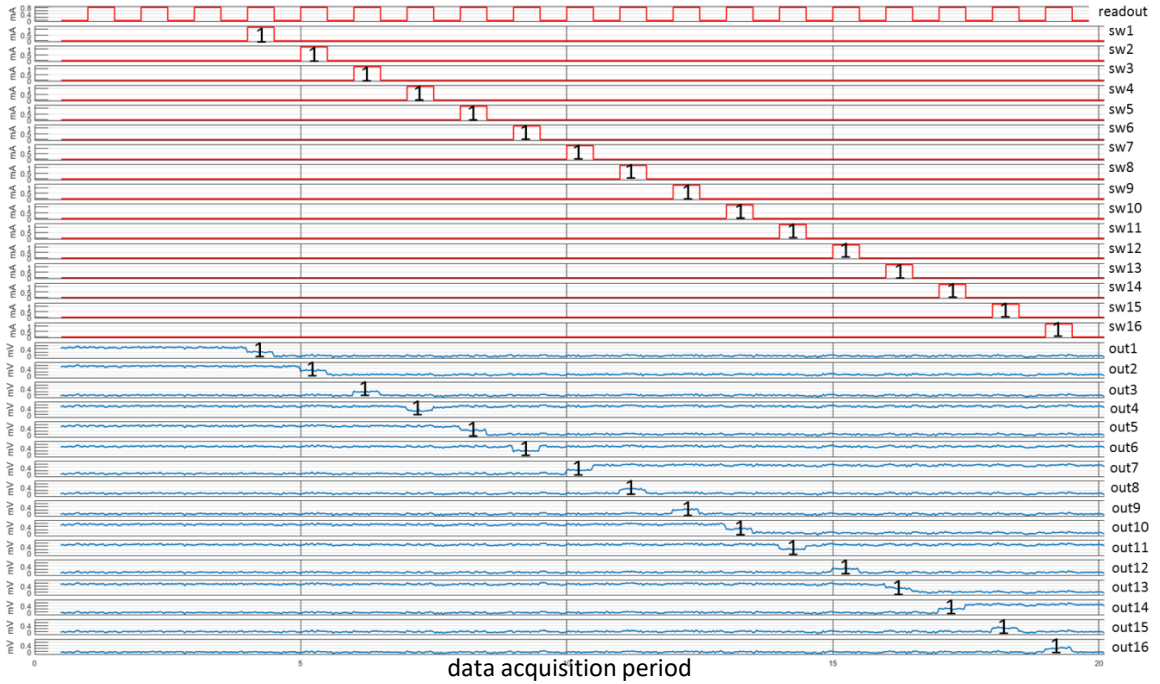
Test approach*



"1" = single line
"0" = double line on oscilloscope
and single line on Octopux





- A clock signal is applied from the high-frequency generator, the control signals are applied at ~2MHz from the Octopux. The outputs are measured by the Octopux on the TFF-based SFQ/dc converters.
- When the output is "0" and no pulses come to the SFQ/dc, the output is a static voltage at 0 or V_{max} ~ 400μV. If a high-speed stream of SFQ comes to the SFQ/dc, it oscillates between 0 and V_{max} resulting in voltage level at $V_{max}/2$ ~ 200μV.
- When measured with the Octopux, the "0" is represented with a line either at 0 or V_{max}, and "1" – as a line at $V_{max}/2$.
- This approach does not provide a bit-error rate (BER) and serves as an estimate of the correct high-speed functionality.

The circuit was operational up to 49 GHz clock frequency in average voltage mode

*T. Filippov, A. Sahu, A. Kirichenko, I. Vernik, M. Dorojevets, C. Ayala, O. Mukhanov, *Physics Procedia* 36, pp. 59-65, 2012
I. Vernik, A. Kirichenko, O. Mukhanov, and T. Ohki, *IEEE Transactions on Applied Superconductivity* 27 (4), 1301205, 2017

Conclusion

- We designed and tested the 4-, 8- and 16-bit on-chip communication circuit
- We designed, assembled and tested the MCMs with flip-chip with 16-bit chip-to-chip communication circuit
- The MCM is tested up to 49 GHz clock frequency using average-voltage approach with bias margins of +/- 8%
- Current version tolerates the transmission word skews of less than clock period
- Addition of multi-word FIFO enables corrections up to several clock periods
- Addition of the FIFO allows to support a token-based processor-memory interface

Acknowledgement

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  - The MIT-LL and Hypres fabrication teams
  - Coenrad Fourie for his assistance with inductance calculation of MCM bumps using InductEx
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