# Low-Cost Fan-Out with SFQ Cell Labeling

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### The Beauty...





#### Ultralow Logic Energy and High Speed



**They're Ultra-Efficient** > The 2.5 GHz prototype uses 80 times less energy than its semiconductor counterpart, even accounting for cooling







#### L. Johnson, 2018 S. Tolpygo, 2020 I. I. Soloviev, 2021 O. Mukhanov, 1997 S. Tolpygo, 2020 O. Mukhanov, 2011 A. Kadin, 2001 J. Kang, 2003 B. Dimov, 2005 M. Maezawa, 2007 M. Suzuki, 2004

B. Ebert, 2009

L. Schindler, 2021 S. Tolpygo, 2007 V. Semenov, 2021 S. Tolpygo, 2019 T. Ortlepp, 2007 V. Kaplunenko, 1995 D. Brock, 2001 L. Gronberg, 2007 I. Vernik, 1999 D. Balashov, 1999 T. Wolf, 2013

N. Yoshikawa, 1999

#### Method 2: EDA

#### Method 3: architecture

Method 1: device

- A. Fujimaki, 2014 G. Tzimpragos, 2019 G. Tzimpragos, 2020 G. Tzimpragos, 2021 J. Volk. 2022 M. Dorojevets, 2013 F. Zokaee, 2021 C. Fourie, 2020 M. Dorojevets, 2003 K. Gaj, 1995 P. Bunyk, 1997 D. Brock, 2001 R. Tadros, 2017
- D. Zinoviev, 1998 F. Feldhoff, 2021 P. Bunyk, 1995 M. Dorojevets, 2010 H. Gerber, 2007 Z. Deng, 1997 M. Dorojevets, 1999 N. Takagi, 2008 K. Ishida, 2020 C. Ayala, 2020 Y. Ando, 2016

#### M. Tanaka, 2015

#### Method 4: JJ utility

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# **Breakdown & challenge** 32-bit KSA JJ Count 33% 37% 30% Logic Gates DROs Splitters H. Cong, 2021



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### **Breakdown & challenge**











### This looks familiar...





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## This looks familiar...



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# **Reducing Redundancies: JJ Borrowing**







#### UCSB **Reducing Redundancies: JJ Borrowing** OR OR **Buffer JJs Decision JJs Blocking JJs** $\frown$ +OUT OUT CLK CLK-CLK CLK DFF DFF (◀) ← Split 250µA $\mathbf{T}$ В В Δ <u>×</u> × 250μA 270μA 355μA 🔆 355µA $\overline{\mathbb{X}}$ $\overline{\Lambda}$ 250ı OR OR 270µA 250µA $\leftarrow$ +250µA OUT OUT CLK CLK $\bigcirc$ -I +12

#### UCSB Reducing Redundancies: JJ Borrowing





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### **Generalizing Connectivity Rules**



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## **Generalizing Connectivity Rules**



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# **Generalizing Connectivity Rules**

#### Target

Î	Ι <sub>c</sub>	500µA	353µA	250µA	180µA	125µA	88µA	66µA	46µA
	500µA								
	353µA								
e	250µA								
ourc	180µA								
S	125µA								
	88µA								
	66µA								
	46µA								

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# **Generalizing Connectivity Rules**

#### Target

I <sub>C</sub>	500µA	353µA	250µA	180µA	125µA	88µA	66µA	46µA
500µA	FO1							
353µA		FO1						
250µA			FO1					
180µA				FO1				
125µA					FO1			
88µA						FO1		
66µA							FO1	
46µA								FO1

Source



# **Generalizing Connectivity Rules**

Target								
I <sub>C</sub>	500µA	353µA	250µA	180µA	125µA	88µA	66µA	46µA
500µA	FO1	FO2	FO3	FO4	FO5	FO6	FO7	FO8
353µA		FO1	FO2	FO3	FO4	FO5	FO6	FO7
250µA			FO1	FO2	FO3	FO4	FO5	FO6
180µA				FO1	FO2	FO3	FO4	FO5
125µA					FO1	FO2	FO3	FO4
88µA						FO1	FO2	FO3
66µA							FO1	FO2
46µA								FO1
	*		*	Amplif	ication		*	

# Source

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# **Generalizing Connectivity Rules**

	I <sub>c</sub>	500µA	353µA	250µA	180µA	125µA	88µA	66µA	46µA
	500µA	FO1	FO2	FO3	FO4	FO5	FO6	FO7	FO8
	353µA		FO1	FO2	FO3	FO4	FO5	FO6	FO7
a d	250µA			FO1	FO2	FO3	FO4	FO5	FO6
Ollro	180µA				FO1	FO2	FO3	FO4	FO5
U,	125µA					FO1	FO2	FO3	FO4
]	$\operatorname{og}\left(\frac{I_T}{I}\right)$						FO1	FO2	FO3
$N_{JTL} \geq -$	$\log(p_r)$							FO1	FO2
	46µA								FO1
	Amplification								

Target

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# **Generalizing Connectivity Rules**

					Target				
Î	Ι <sub>c</sub>	500µA	353µA	250µA	180µA	125µA	88µA	66µA	46µA
	500µA	FO1	FO2	FO3	FO4	FO5	FO6	FO7	FO8
	353µA	+1 JTL	FO1	FO2	FO3	FO4	FO5	FO6	FO7
e	250µA	+2 JTL	+1 JTL	FO1	FO2	FO3	FO4	FO5	FO6
ourc	180µA	+2 JTL	+2 JTL	+1 JTL	FO1	FO2	FO3	FO4	FO5
S	125µA	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1	FO2	FO3	FO4
log	$\left(\frac{I_T}{I_s}\right)$	+3 JTL	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1	FO2	FO3
$N_{JTL} \ge \overline{\log}$	$\overline{g(p_r)}$	+4 JTL	+3 JTL	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1	FO2
	46µA	+4 JTL	+4 JTL	+3 JTL	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1
					Amplif	ication			

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# Generalizing Connectivity Rules

	Rank	8	7	6	5	4	3	2	1		
Rank	Ι <sub>C</sub>	500µA	353µA	250µA	180µA	125µA	88µA	66µA	46µA		
8	500µA	FO1	FO2	FO3	FO4	FO5	FO6	FO7	FO8		
7	353µA	+1 JTL	FO1	FO2	FO3	FO4	FO5	FO6	FO7		
6	250µA	+2 JTL	+1 JTL	FO1	FO2	FO3	FO4	FO5	FO6		
5	180µA	+2 JTL	+2 JTL	+1 JTL	FO1	FO2	FO3	FO4	FO5		
4	125µA	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1	FO2	FO3	FO4		
3	88µA	+3 JTL	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1	FO2	FO3		
2	66µA	+4 JTL	+3 JTL	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1	FO2		
1	46µA	+4 JTL	+4 JTL	+3 JTL	+3 JTL	+2 JTL	+2 JTL	+1 JTL	FO1		
					Amplif	ication					



# **Design Methodology**

#### **1. All logic cells have same rank**



			Target	
		Rank	7	6
lce	Rank	Ι <sub>c</sub>	353µA	250µA
Sol	7	353µA	FO1	FO2









# **Design Methodology**

2. All logic cells have lowest rank



Rank-1







46µA

1

+2 JTL

FO1



#### **Design Methodology 3. Flexible rank**

CLK DFF A 125µA 136µA Rank-4

			Target					
		Rank	4	1				
	Rank	I <sub>c</sub>	125µA	46µA				
Sou	4	125µA	FO1	FO4				



Source

Rank

4

# **Design Methodology**

3. Flexible rank





### **Evaluation**

#### Bias current analysis

Cell	Fan-Out	Flex. Rank	Matched Rank
AND	FO2	59.18%	17.41%
	FO4	81.31%	23.92%
	FO8	68.87%	26.78%
OR	FO2	49.26%	14.49%
	FO4	74.44%	21.90%
	FO8	65.95%	25.64%
XOR	FO2	77.56%	22.81%
	FO4	91.20%	26.83%
	FO8	72.65%	28.25%
INV	FO2	41.84%	12.31%
	FO4	68.34%	20.10%
	FO8	63.12%	24.54%
DFF	FO2	77.61%	22.83%
	FO4	91.23%	26.83%
	FO8	72.66%	28.25%
AVG		70.35%	22.86%

**Percent Savings** 

#### Bias margin analysis

Configuration	Ranking	Splitters
JTL Chain R6:8	+38.5 / -65.4%	-
JTL Chain R6:8 + FO3	+38.5 / -57.7%	+30.8 / -53.8%
JTL Chain R6:8 + FO8	+38.5 / -46.2%	+26.9 / -34.6%
JTL Chain R1:8 + FO8	+42.3 / -46.2%	+26.9 / -34.6%
JTL Chain R6:8 + FO9	+38.5 / -46.2%	+26.9 / -46.2%
Average	+39.5 / -49.1%	+28.2 / -44.9%







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# Summary

#### **Key contributions**

- JJ borrowing
- Cell ranking

arXivhttps://arxiv.org/abs/2206.07817Image: the state of the state

#### Results

- Saves up to 45% of splitting JJs/15% of the total JJ count
- Up to ~70% lower bias current for splitting
- No bias margin degradation

#### Next task

- Integration with optimizers
- Align ranking methodology with design goals



### **Questions?**

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