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D:WAVE
The Quantum Computing Company™

Developing a commercial superconducting quantum annealing processor

30th International Symposium on Superconductivity
ISS 2017

Mark W Johnson
D-Wave Systems Inc.

December 14, 2017 ED4-1

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Overview

- Introduction to quantum annealing
- D-Wave 2000Q & technology
- What can it do?
- What's next?

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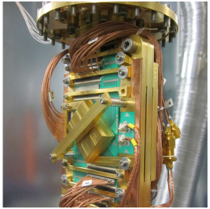
D:Wave
The Quantum Computing Company™

- Founded 1999
- H. Q. in Burnaby, BC
- 150 U.S. Patents

  Portfolio ranked 4th in 2016 in Computer Systems Industry by IEEE Spectrum



- 160 employees (45 w/ PhDs)
- Fourth generation of commercially available quantum annealing systems

Customers Include:

LOCKHEED MARTIN
USC University of Southern California
NASA
Google
Los Alamos National Laboratory EST. 1943
TDS Temporal Defense Systems
Oak Ridge National Laboratory

$50 Million in Quantum Systems deployed to customer facilities

The goal of quantum annealing (QA): model the Hamiltonian

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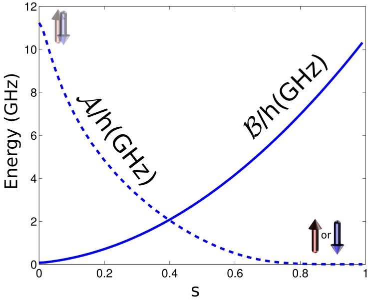
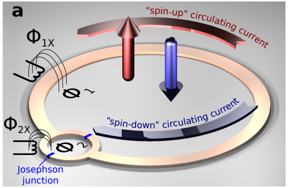
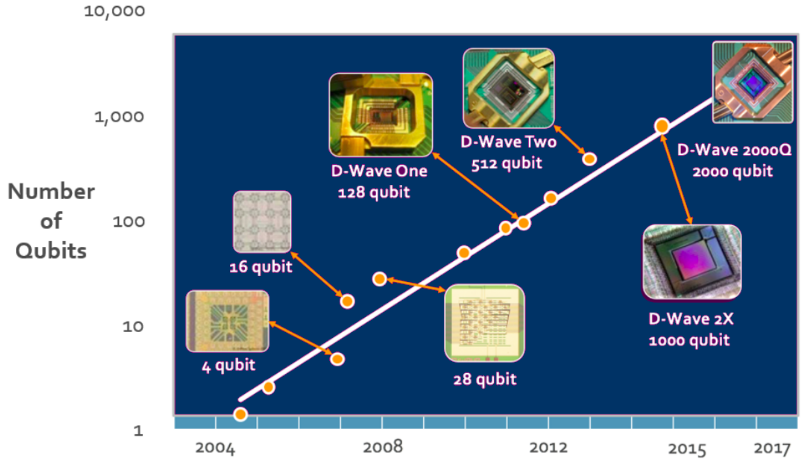
$$\mathcal{H}_S(s) = -\frac{1}{2}\mathcal{A}(s)\sum_i \sigma_{x,i} + \mathcal{B}(s)\left[-\sum_i h_i\sigma_{z,i} + \sum_{i<j} J_{ij}\sigma_{z,i}\sigma_{z,j}\right]$$

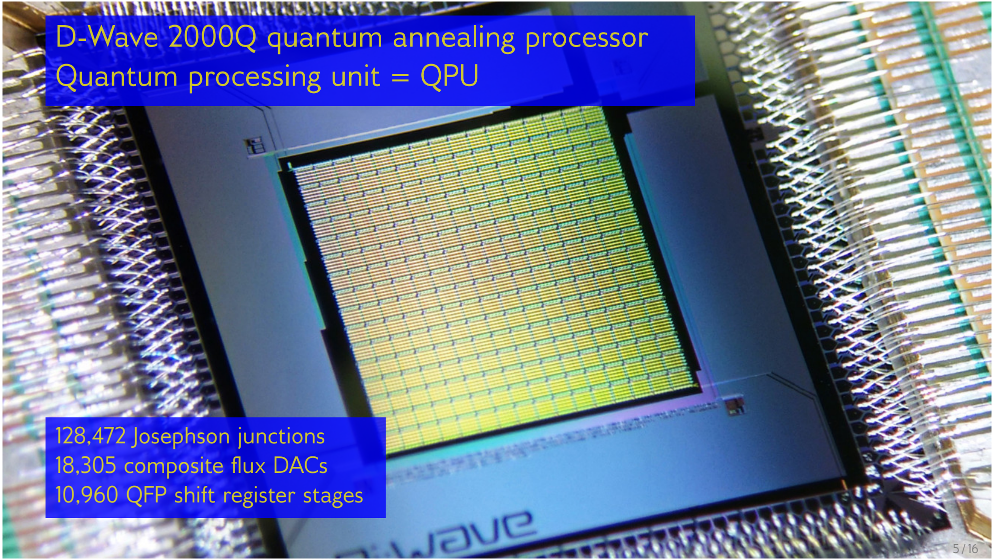




- T. Kadowaki and H. Nishimori, PRE, **58**(5), pp. 5355-5363, (1998)
- E. Farhi, *et al.*, Science **292**, 472 (2001)
- W. Kaminsky, S. Lloyd, T. Orlando, **arXiv:quant-ph/0403090**, “Scalable Superconducting Architecture for Adiabatic Quantum Computation”

Progression of processor scale over time




D-Wave 2000Q quantum annealing processor
Quantum processing unit = QPU
128,472 Josephson junctions
18,305 composite flux DACs
10,960 QFP shift register stages
5 / 16

Extreme environmental control affects many aspects of system design

Superconducting IC (QPU) held at ≤ 15 mK

- pulse tube dilution refrigerators (PTDR) commercially available
- modify PTDRs: make more suitable to our requirements and customer setting
- have achieved run times over 2 years
- QPU, wiring, filter designs constrained with power budget

Magnetic field on QPU $|B| < 1$ nT during cool-down

- passive shielding
- active field compensation

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QC is analog computing: *controlling parameters in a Hamiltonian*

- manufacturing variation in device parameters leads to unacceptably large error in problem specification
- integrated control circuitry enables device homogenization
- requires measuring device parameters first (scalable calibration)
- time scale for calibration consistent across many generations and *independent of device count*

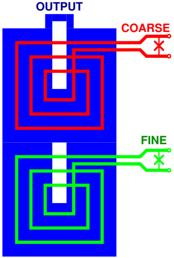
Classical integrated superconducting control circuitry

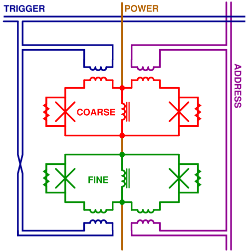
A 2048 Q processor requires ∼18,000 bias signals to operate,

- *only ∼150 bias lines passed to the chip via wirebonds*
- *local static (programmable) flux biases applied by on-chip flux-DACs*

Use on-chip DACs to:

- program $\{h_i\}$, $\{J_{ij}\}$
- homogenize devices
- coerce Ising behaviour





X/Y/Z addressing scheme uses ∼82 wires to address ∼36,000 DAC "loops"

∼22 kilobytes of on-chip memory ∼1 megabyte/s

See Bunyk *et al.*, arXiv:1401.5504 (2014),

or Johnson *et al.*, Supercond. Sci. Technol. **23**, 065004 (2010)

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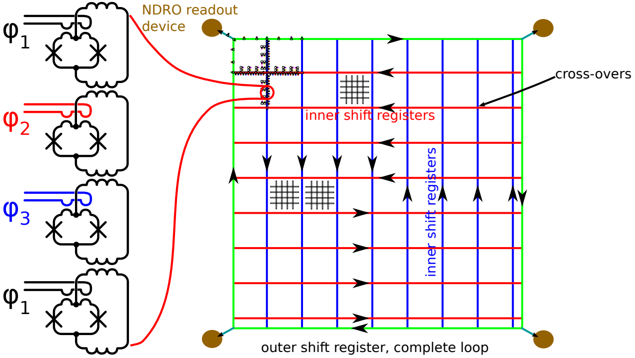
Reading out the processor

Shift register using quantum flux parametron[1] and 4 NDROs



[1]M. Hosoya, *et al.*, IEEE Trans. Appl. Supercond., Vol 1, pp. 77-89, (1991)

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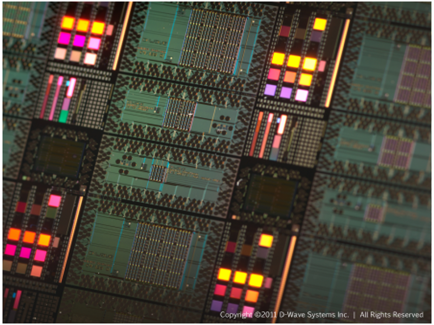
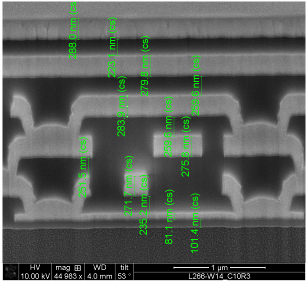
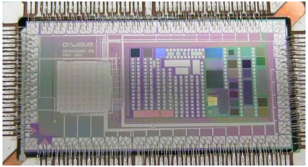
Superconductor fabrication at a commercial semiconductor foundry







- Nb/Al/AlOx/Nb trilayer process
- Six Nb wiring layers
- PE-CVD SiO_2 dielectric (with CMP)
- 0.25μm lines & spaces

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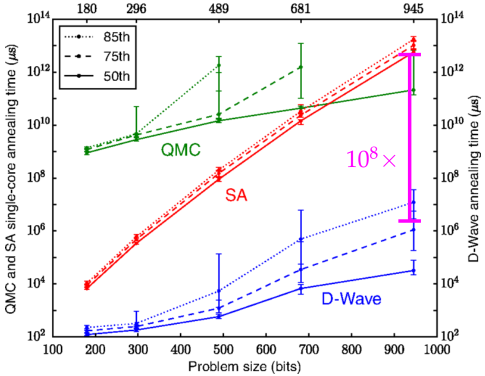
Google cluster result highlights role of quantum tunneling in computation

- Can quantum tunneling accelerate computation?
- synthetic problem designed to highlight quantum tunneling
- locally hard, globally easy
- did not include stronger heuristic solvers in comparison



V. S. Denchev, *et al.*, "What is the Computational Value of Finite-Range Tunneling?", Phys. Rev. X **6**, 031015 (1 Aug 2016).

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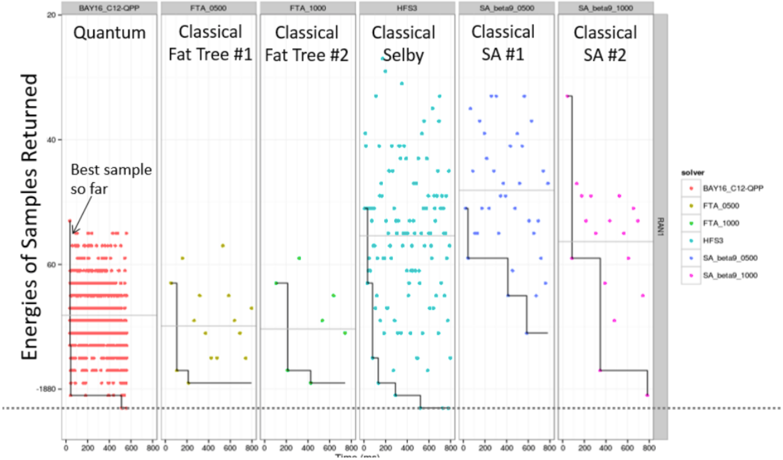
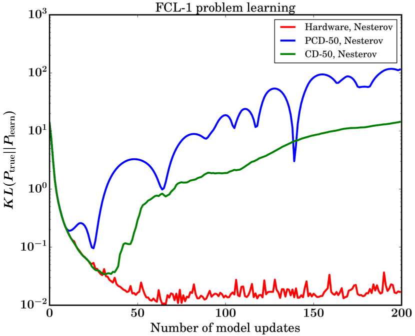
Quantum annealer quickly samples low-energy states



Quantum annealing accelerates machine learning

- Significant recent progress in supervised machine learning
- ***Un***supervised learning benefits from fast sampling of problem energy spectrum
- Sampling from diverse low-energy configurations enables efficient construction of accurate ML models
- Accurate models can be attained with fewer model updates during learning

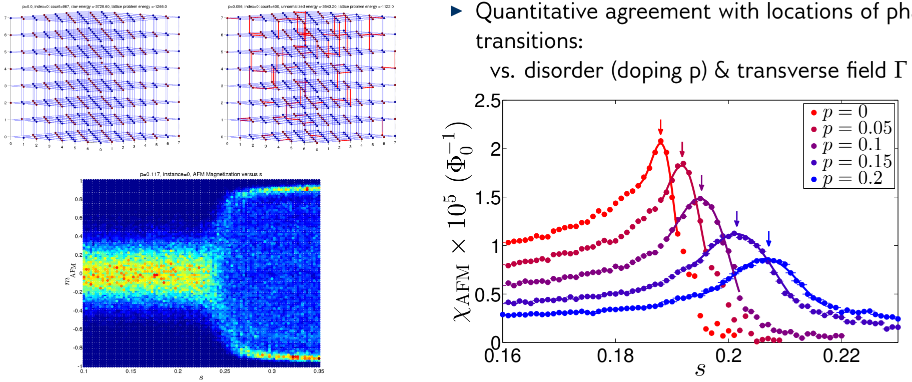


- "Benchmarking Quantum Hardware for Training of Fully Visible Boltzmann Machines", D. Korenkevych, *et al.*, `arXiv:1611.04528 [quant-ph]`
- "Quantum Boltzman Machine", M. H. Amin, *et al.*, `arXiv:1601.02036 [quant-ph]`

Quantum simulation of transverse field cubic Ising lattice (R. Harris)

$$\mathcal{H}_{3D}(s) = -\frac{\Gamma(s)}{2}\sum_i \sigma_i^x + \mathcal{J}(s)\sum_{\langle i,j\rangle} J_{ij}\sigma_i^z\sigma_j^z$$

- 3D transverse Ising models embedded in D-Wave QA processor
- Quantitative agreement with locations of phase transitions:
  vs. disorder (doping p) & transverse field Γ



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Summary

- D-Wave 2000Q processor
- Quantum computing as a product
- Next generation significant increase connectivity