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Design and high-speed demonstration of an SFQ complex event detector circuit for complex event processing

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The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2).

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Background

- ## Big data
  - ➢Large amount and various kinds of information
  - ➢Traditional data processing approach is inadequate.

	Batch processing	**Real time processing**
Equipment	Hard disk	Memory
Time scale of data	Days - Years	Seconds - Minutes
Example	・Comparison of monthly site accesses ・Calculation of monthly sales	・Detection of cyber terrorism ・Financial algorithm transaction

As the amount of data increases, real time processing is gathering attention.

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Complex Event Processing

- ## Complex Event Processing (CEP)

  ➢real-time processing for stream data

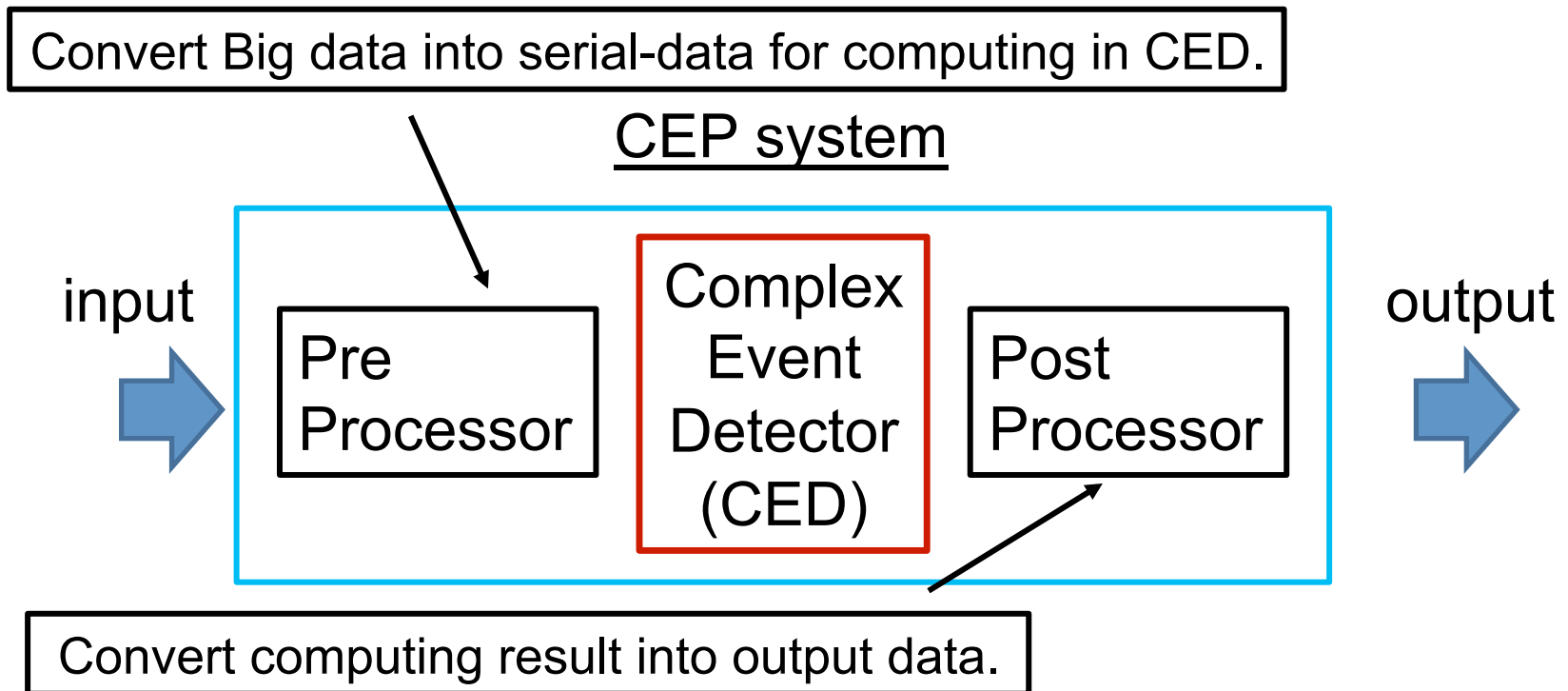 - detection of cyber terrorism
  - financial algorithm transaction

IBM Security Network Protection XGS (XGS5100)

[1]http://www.hitachi-solutions.co.jp/products/search_k/ids.html

Complex Event Detector

- ## Complex Event Detector (CED)
  - ➢ Component circuit of CEP system
  - ➢ Performs pattern matching between "Data" and "Symbol"

| Convert Big data into serial-data for computing in CED. |

CEP system

| input | Pre Processor | Complex Event Detector (CED) | Post Processor | output |

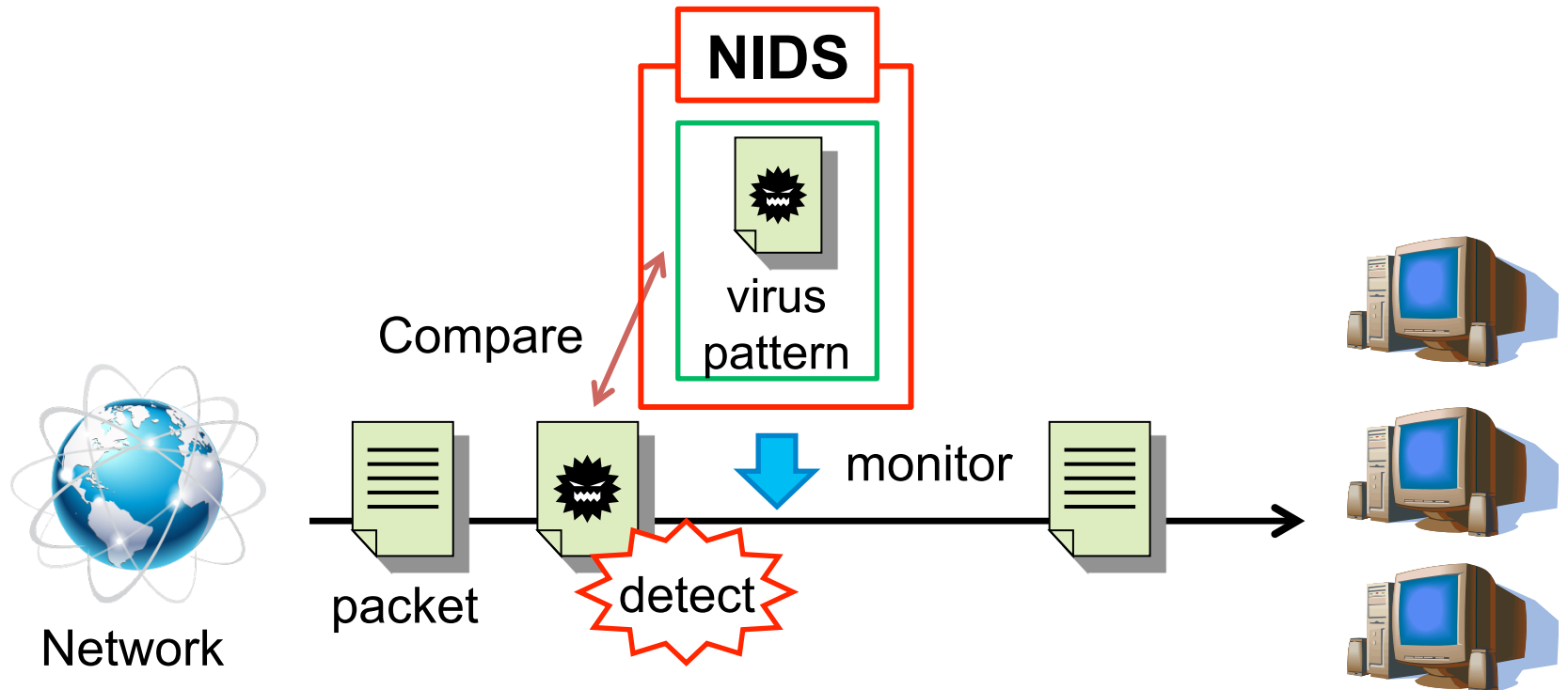| Convert computing result into output data. |

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Pattern Matching

- Main operation of CED circuit

- Detecting "Symbol" string from "Data" string by comparison

- Corresponding to regular expression, variety of patterns are detected.

Detect

Data | A | C | B | A | B | C | D | A

t

Symbol | A | B | C | D
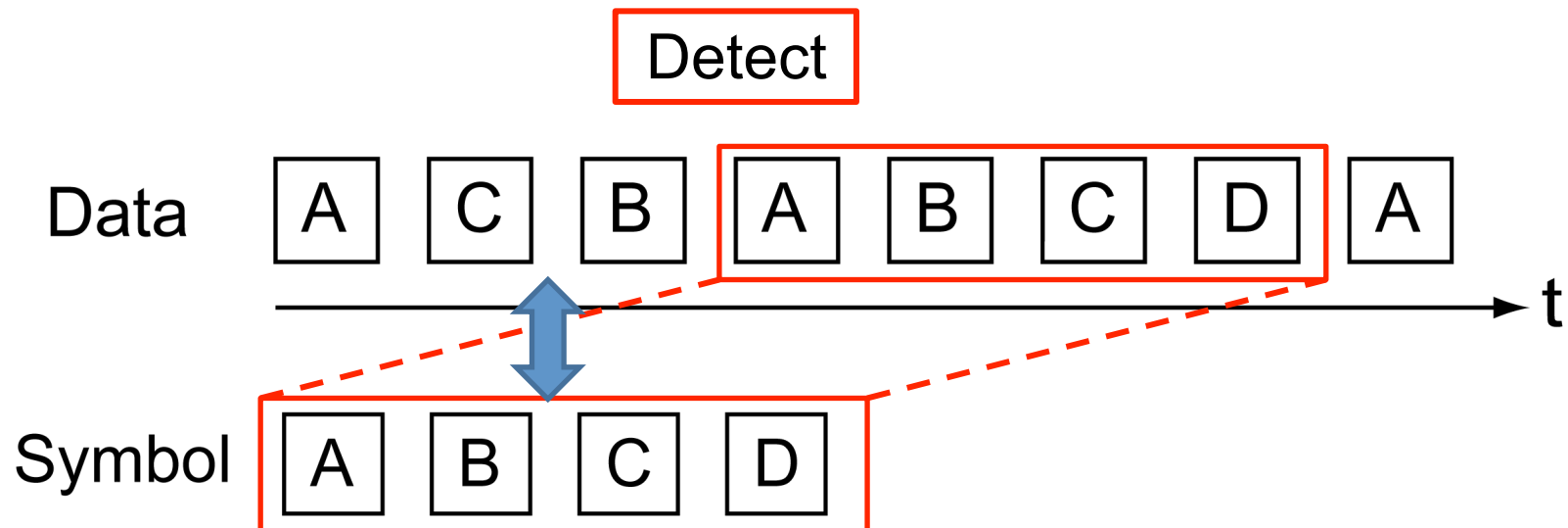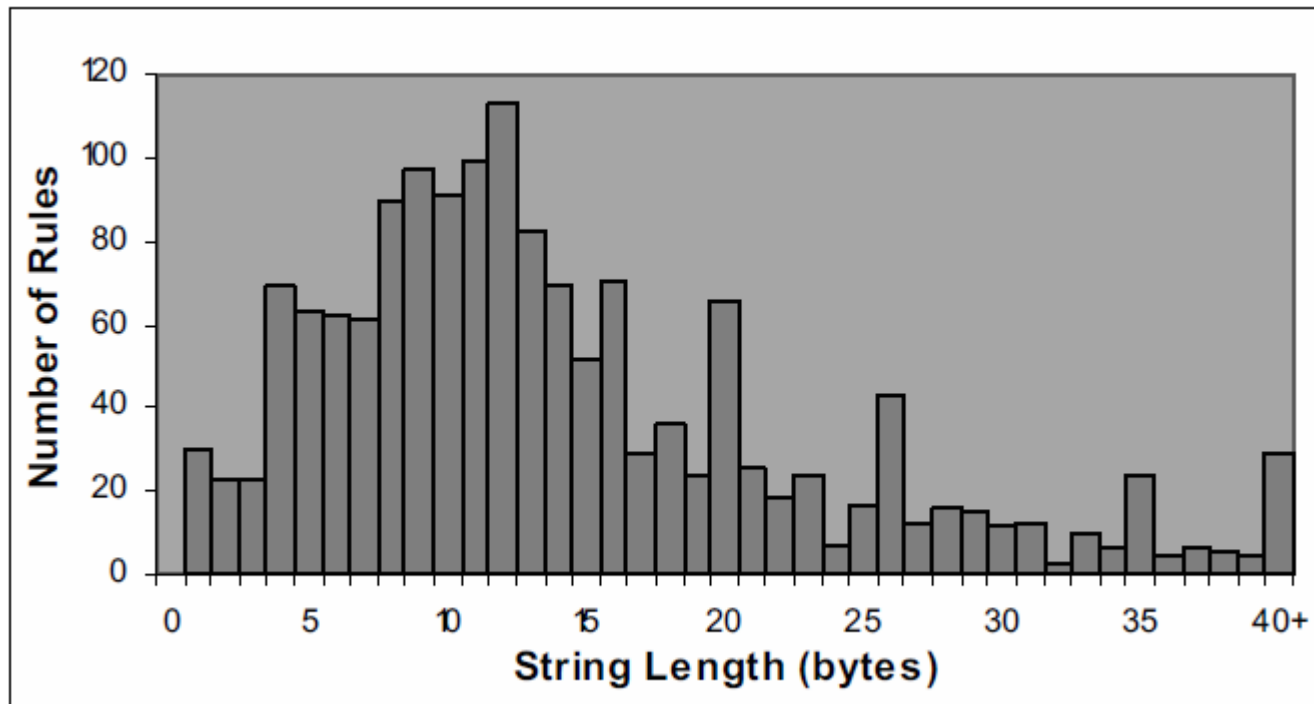
Network Intrusion Detection System

- Network Intrusion Detection System (NIDS)

NIDS detects virus by comparing packet and virus pattern.

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Virus Pattern of NIDS[2]

- Total number of virus pattern in snort at 2003 ：1542
- Average length：14 Symbol

[2] M. Aldwairi, T. Conte, and P. Franzon, "Configurable string matching hardware for speeding up intrusion detection," ACM SIGARCH Computer Architecture News, vol. 33, no. 1, pp. 99–107, Mar. 2005.

Problem of CMOS NIDS

CMOS NIDS[3]			
Method	Device	Logic cells	Throughput
NFA	Virtex2P	12822	1.85 Gbps

[3] T. T. Hieu, T. N. Thinh, T. H. Vu, and S. Tomiyama, "Optimization of Regular Expression Processing Circuits for NIDS on FPGA," in 2011 Second International Conference on Networking and Computing, 2011, pp. 105–112.

- ## Communication speed is getting faster.
  - ➢Optical communication is high speed.
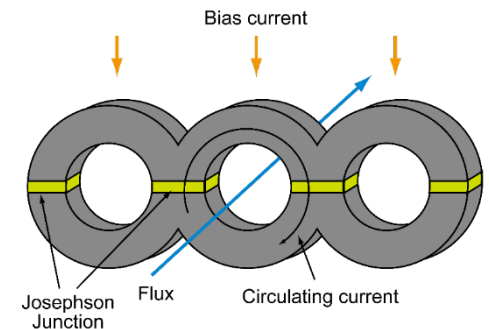 - ex. OC-768 (40Gbps)

<u>It is difficult to catch up with growth of communication speed.</u>

Purpose

NIDS must catch up with growth of communication speed.
ex. OC-768 (40 Gbps)

• Single Flux Quantum : SFQ
  ➤ High speed operation (10s of GHz)
  ➤ Low power consumption

• Purpose
  ➤ Design CED circuit for NIDS by SFQ circuit
  ➤ Demonstration CED circuit for regular expression

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Structure of SFQ CED Circuit

- Composed of 1-symbol matching circuit (1SMC)
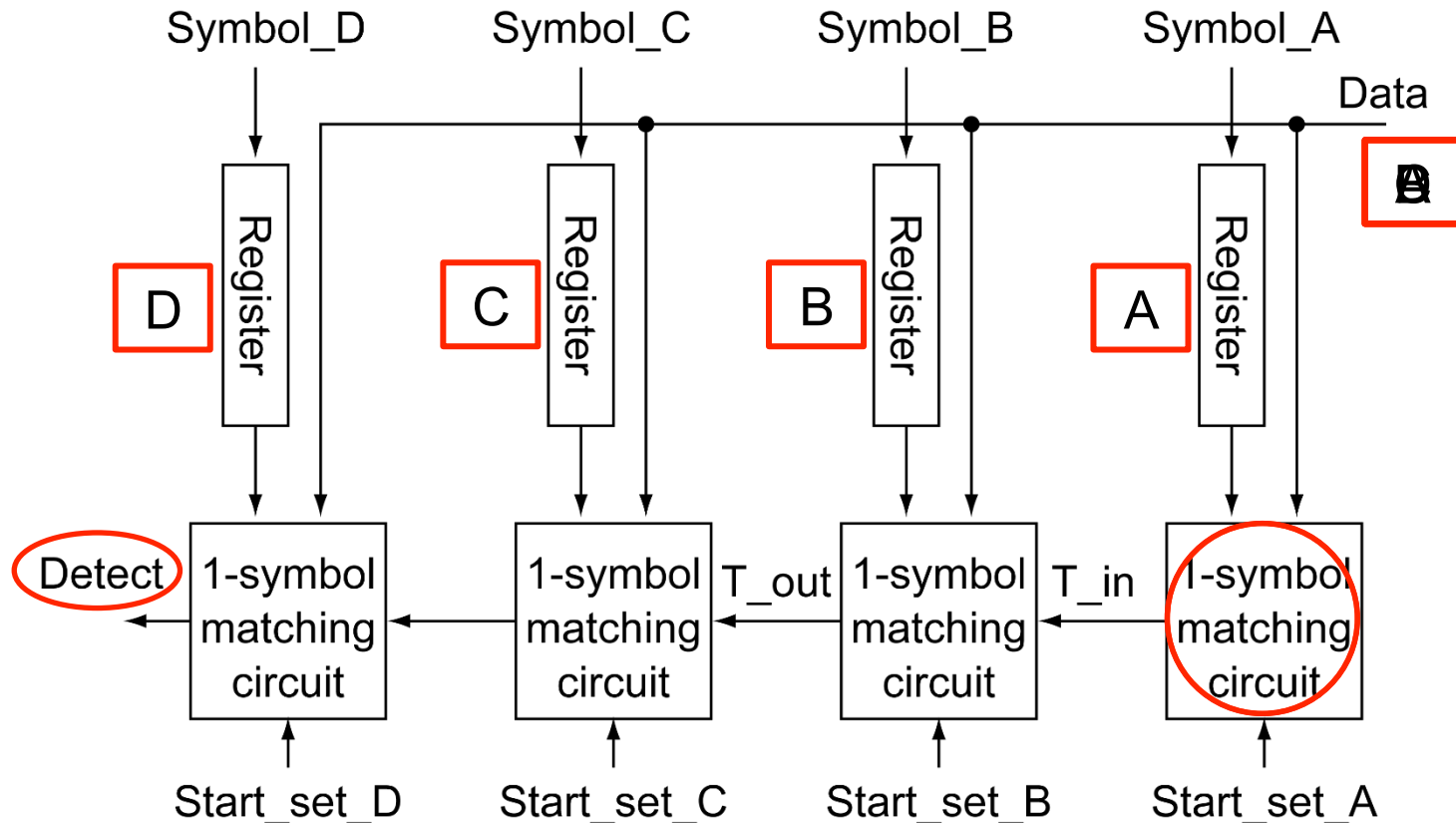- Comparing 8-bit "Data" with "Symbol" bit-serially at 1SMC

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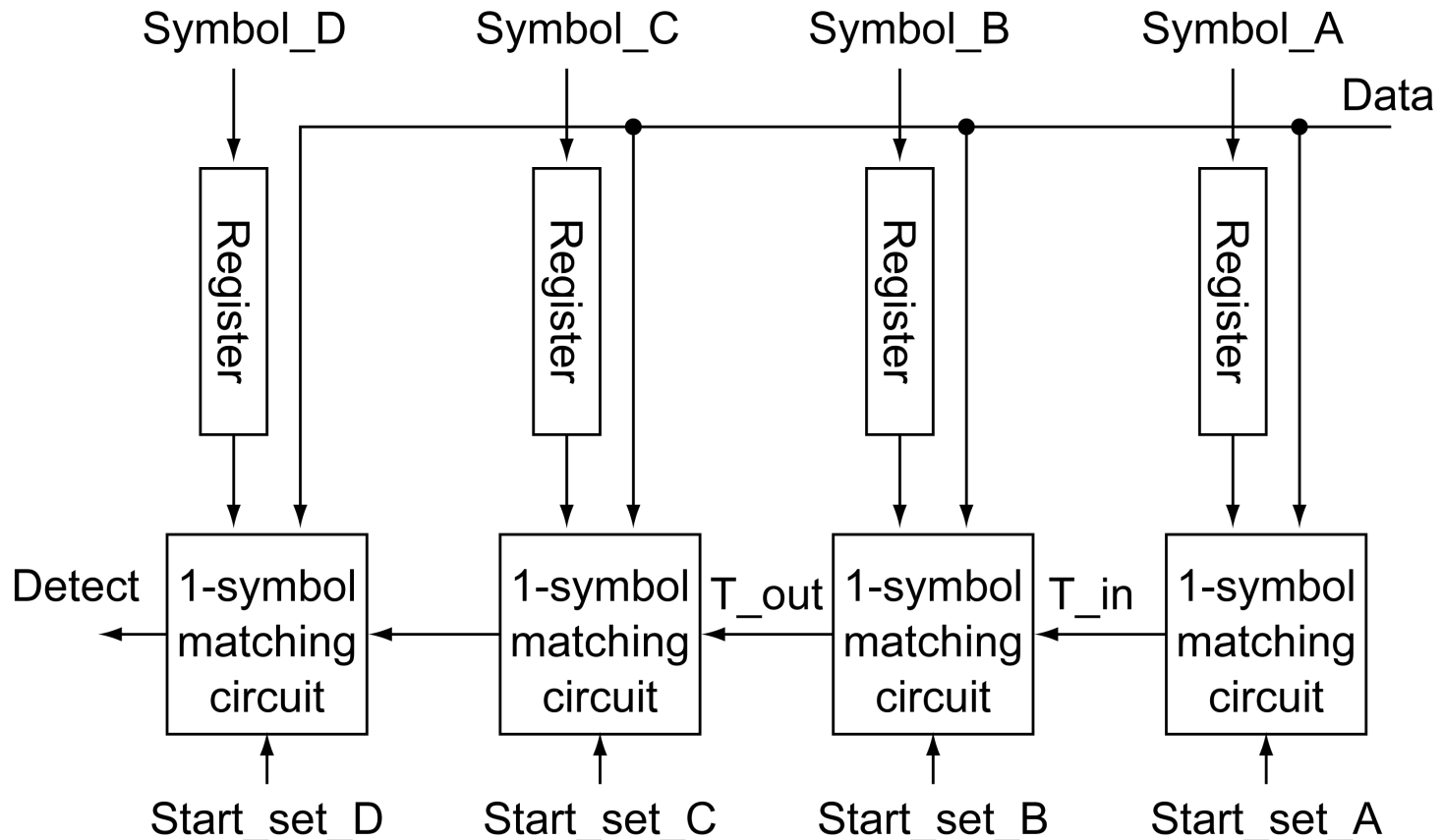
Operation of SFQ CED Circuit 1/2

- Data = Symbol : Next "Symbol" and "Data" are compared
- ex. Symbol : A B C D
  Data : A B C D

Data=Symbol_A

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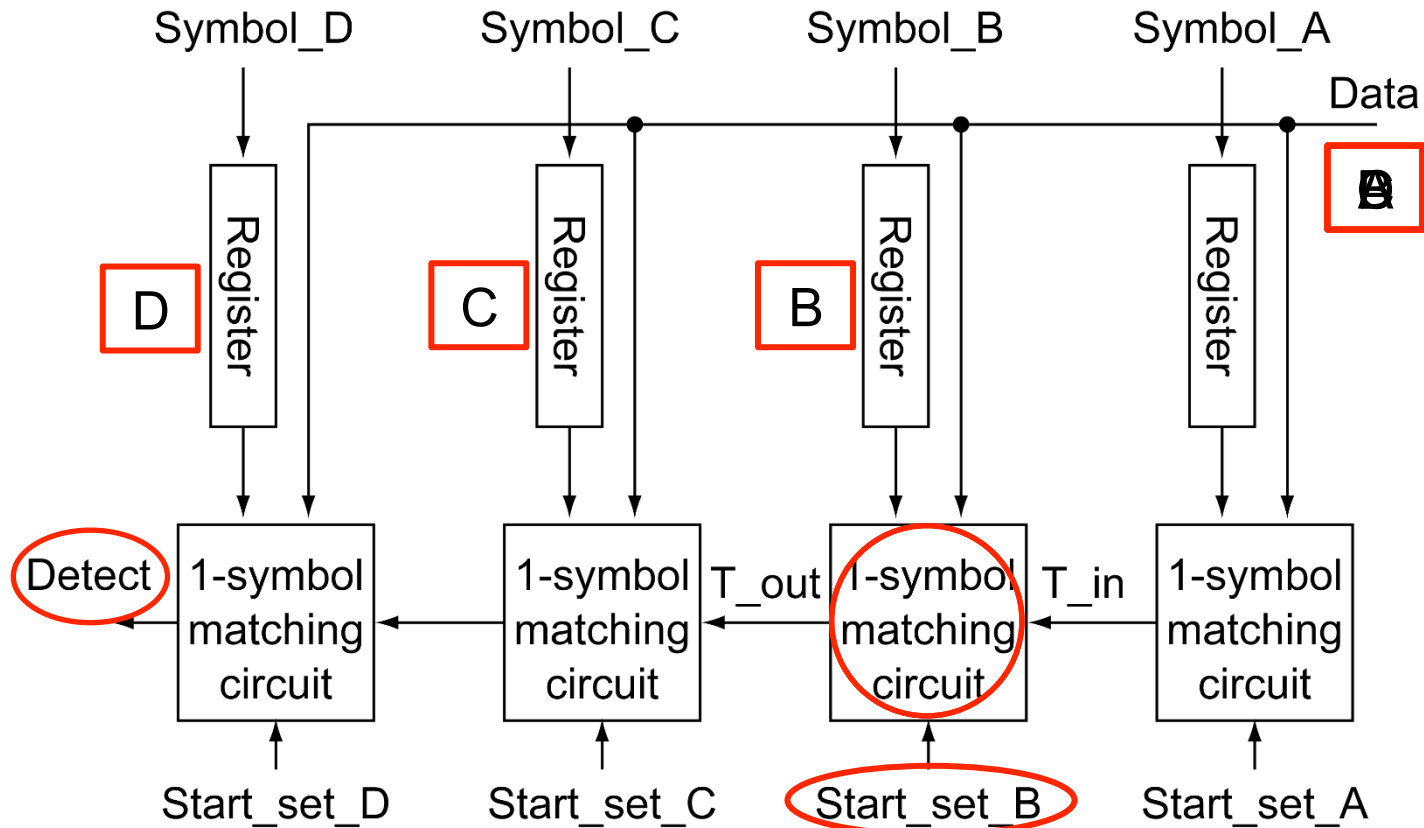# Operation of SFQ CED Circuit 2/2

- Decide length of Symbol by Start_set signal
- ex. Symbol : B C D
    Data   : A B C D

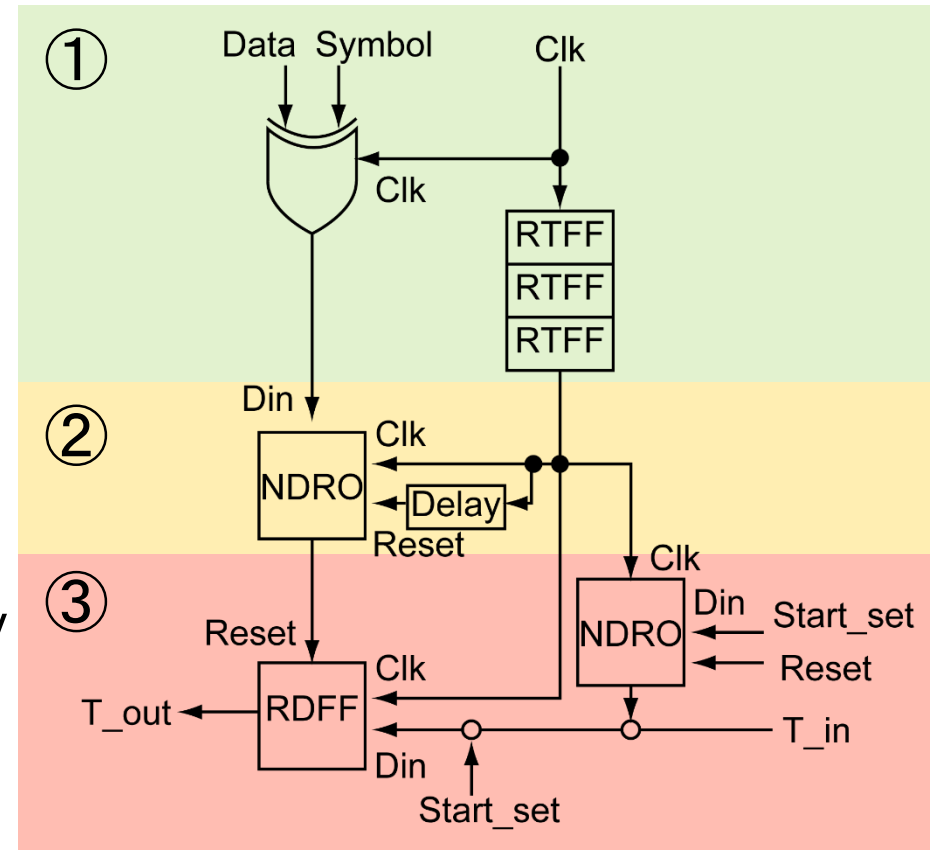# Operation of 1-Symbol Matching Circuit

- ## Structure
  - ➤ XOR, Flip Flops
  - ① Comparison part
  - ② Result storing part
  - ③ Result control part
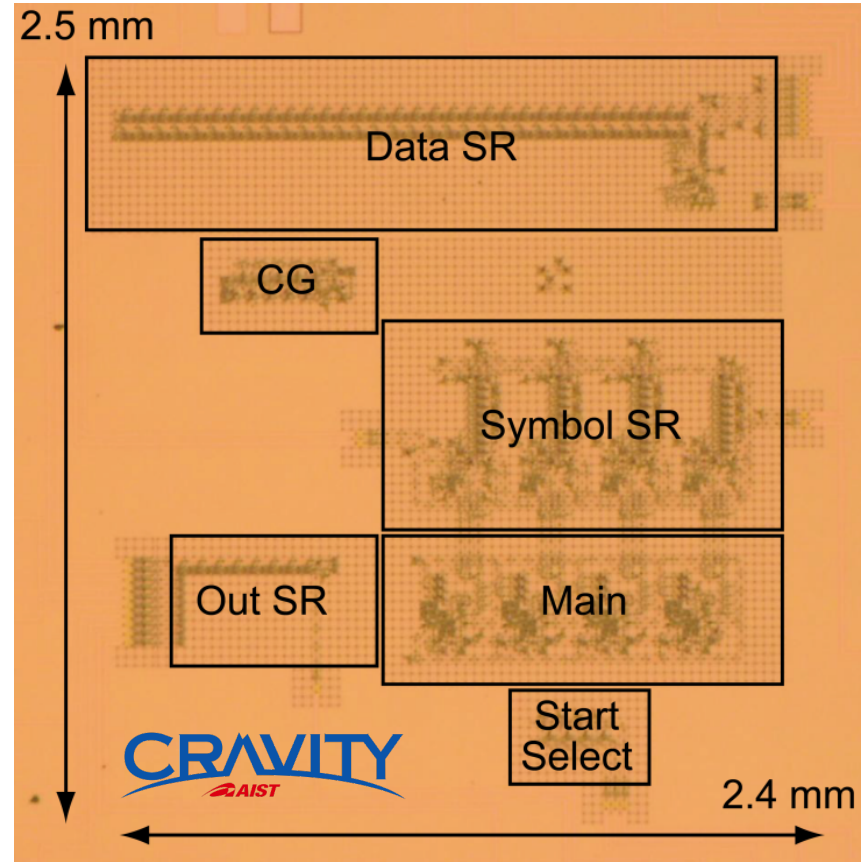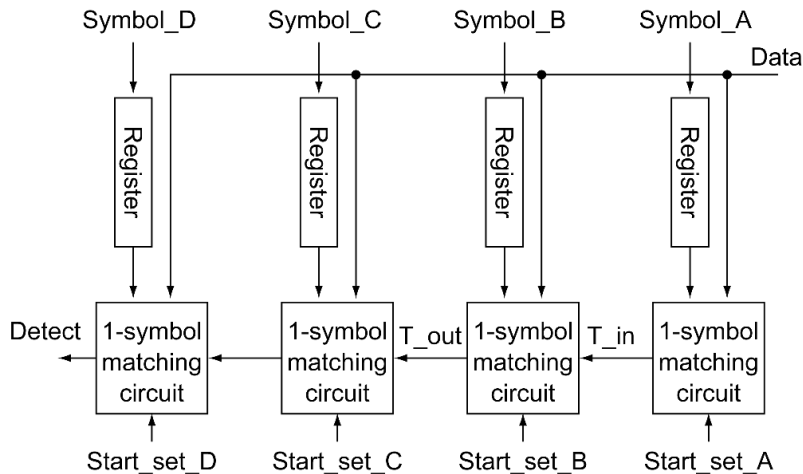
- ## Operation
  1. Compare 8-bit input bit-serially
  2. Register result of comparison
  3. Output result of comparison

If "Data" = "Symbol", T_out propagates to next 1SMC.

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Design 4-Symbol SFQ CED Circuit

- Pattern matching for 4 or less Symbol

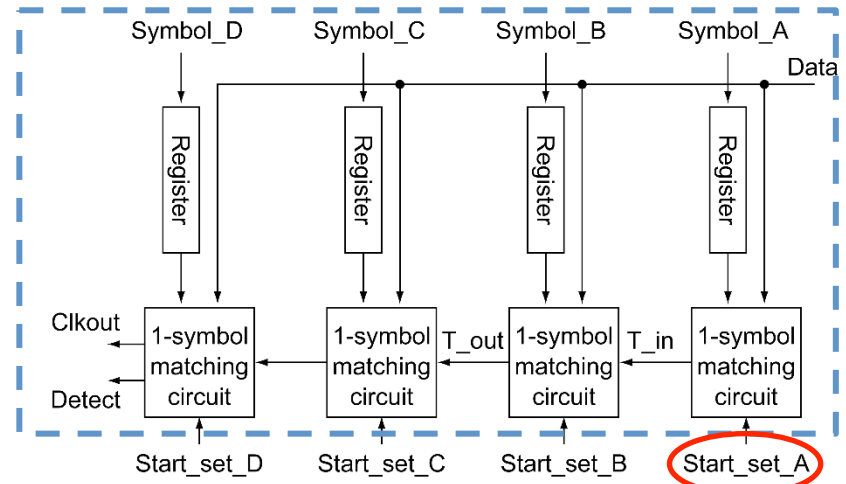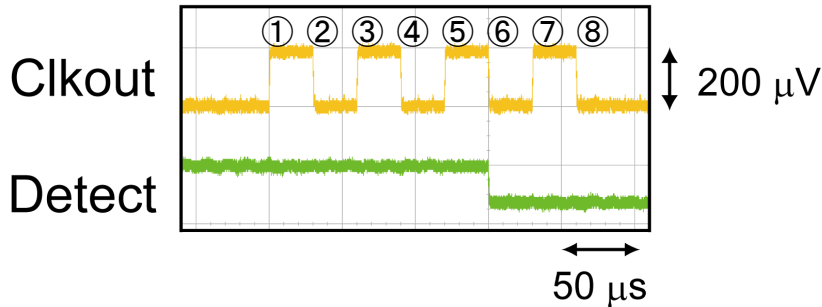- 1 Symbol is 8 bits.
  "Symbol" = $00001000_{(2)}$
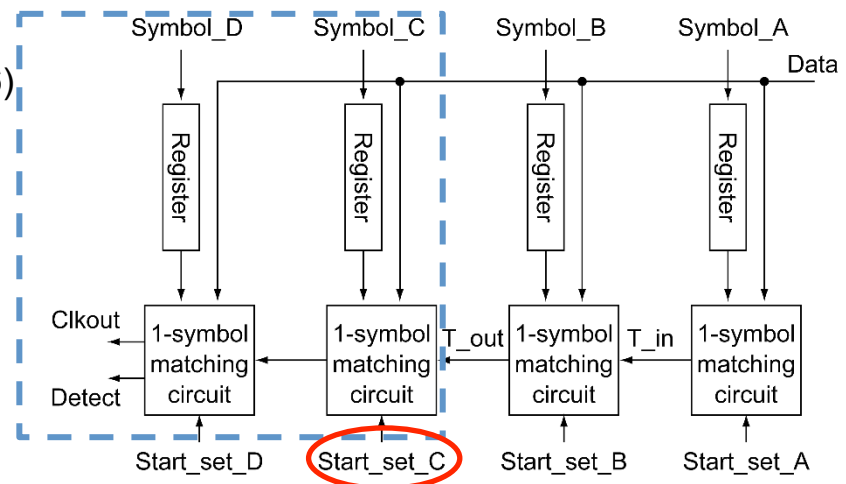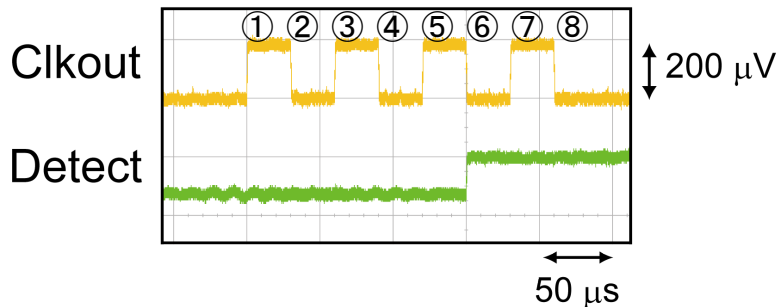 $= 08_{(16)}$

Process : AIST ADP2 (10 kA/cm^2)

Area	Bias current	Number of JJs
2.4 × 2.5 mm^2	540 mA	4476

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Waveform of High Speed Measurement

① ② ③ ④ ⑤ ⑥ ⑦ ⑧

Data : 01 80 68 6F 73 74 00 FF (16)

Symbol : 68 6F 73 74 (16)

Clkout

Detect

200 μV

50 μs

Symbol_D Symbol_C Symbol_B Symbol_A

Data

Register Register Register Register

Clkout

Detect

1-symbol matching circuit 1-symbol matching circuit 1-symbol matching circuit 1-symbol matching circuit

T_out T_in

Start_set_D Start_set_C Start_set_B Start_set_A

① ② ③ ④ ⑤ ⑥ ⑦ ⑧

Data : B4 80 B4 01 B4 B4 00 FF (16)

Symbol : B4 B4 (16)

Clkout

Detect

200 μV

50 μs

Symbol_D Symbol_C Symbol_B Symbol_A

Data

Register Register Register Register

Clkout

Detect

1-symbol matching circuit 1-symbol matching circuit 1-symbol matching circuit 1-symbol matching circuit

T_out T_in

Start_set_D Start_set_C Start_set_B Start_set_A

Correct operation was confirmed at high speed measurement.

Operation Margin of 4-Symbol SFQ CED Circuit
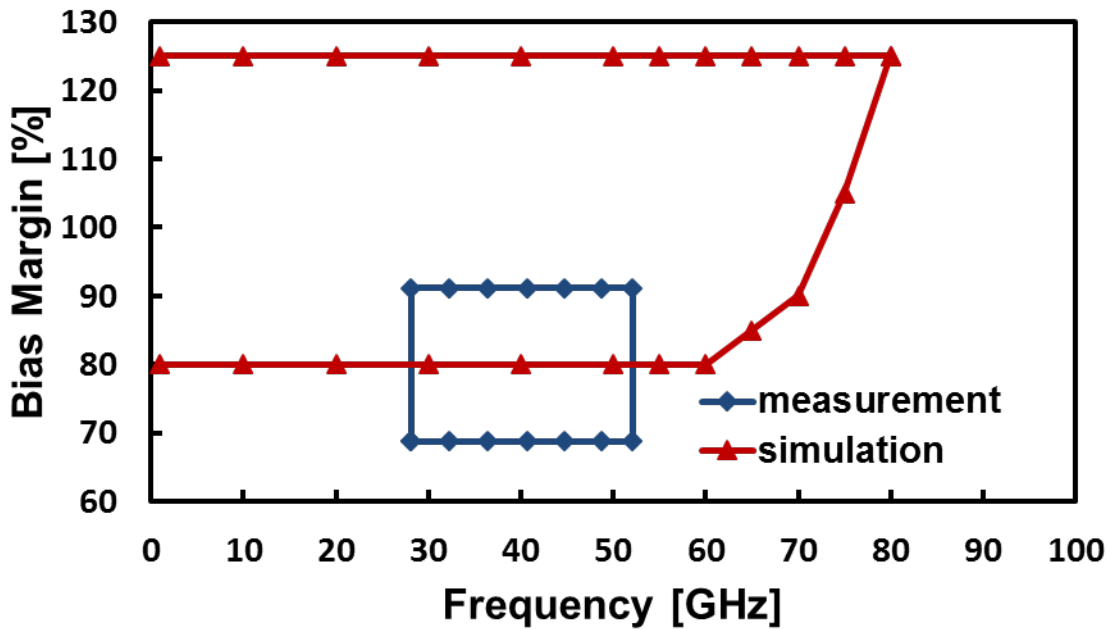
	Simulation	Measurement
Bias Margin @ 52.1 GHz	80%～125%	68.8%～91.2%

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Regular Expression

- We confirmed correct operation of exact matching.

- Regular expression
  - Description of flexible pattern
 - Virus pattern is written in regular expression.

ex: `A.CD = ABCD, ACCD, ADCD,` ···

Expression	Meaning
`[.]`	Matches any data.
`[A+]`	Matches a sequence of one or more data "A".
`[ A|B ]`	Matches either data "A" or "B".
`[^A ]`	Matches the all data except data "A".

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Corresponding to Regular Expression

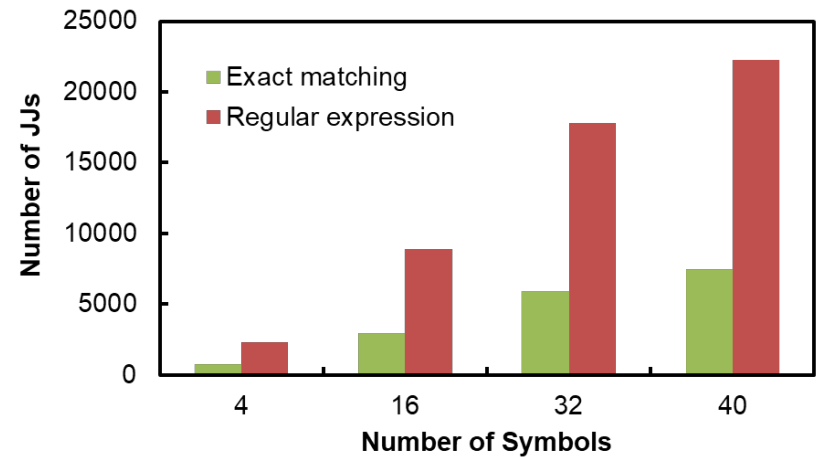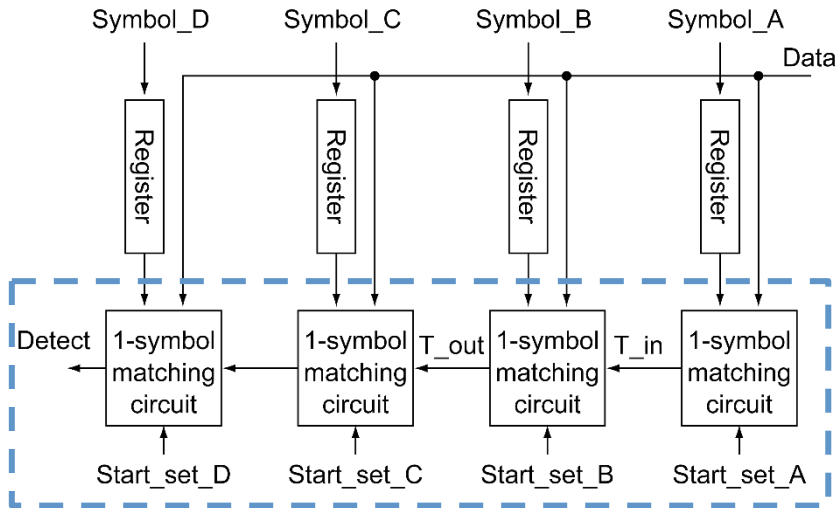| Expression	Meaning
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`[^A ]`	Matches the all data except data "A".

ex: `A.CD = ABCD, ACCD, ADCD, ・・・`
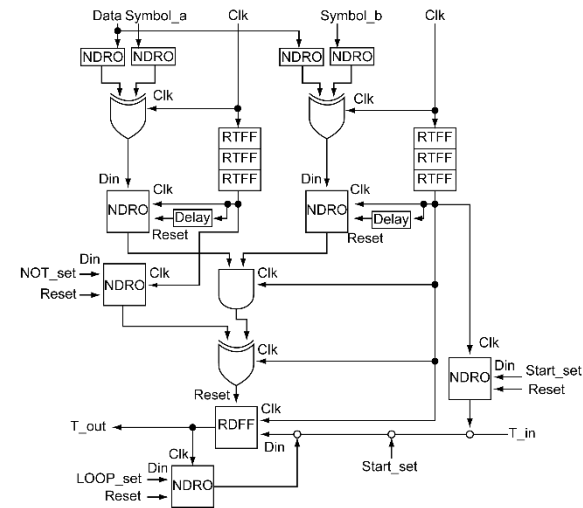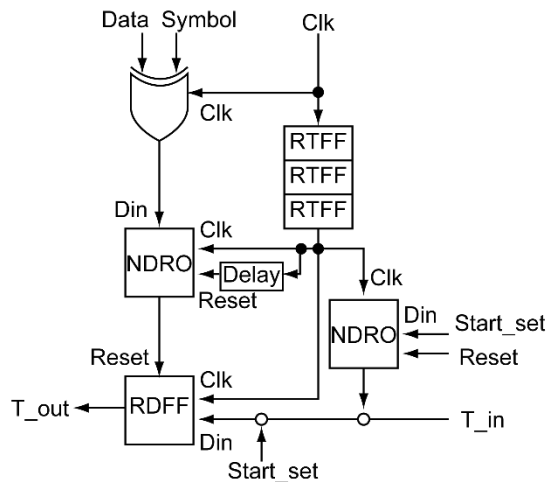
__Corresponding to regular expression by adding functions to 1SMC.__

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Scaling of SFQ CED circuit

- SFQ CED circuit has scalability.
- Operating speed is not reduced by scaling up.

	Exact matching	Regular expression
JJs (40 Symbol)	7448	22260

If we design CED circuit for enough Symbol, number of JJs will be 22260.

Summary

- CEP is one approach to process big data.
  - One of the applications of CEP system is NIDS.
  - Performs pattern matching in CED circuit

- Demonstrated 4-symbol SFQ CED circuit
  - Number of JJs is 4476.
  - Bias margin at 52.1 GHz is 68.8%～91.2%.

- Estimated CED circuit for regular expression
  - Added functions to 1SMC for regular expression
  - when we extended the scale of CED circuit, operating speed isn't reduced
  - Number of JJs will be 22260 for a 40-Symbol CED.

Thank you for your attention !