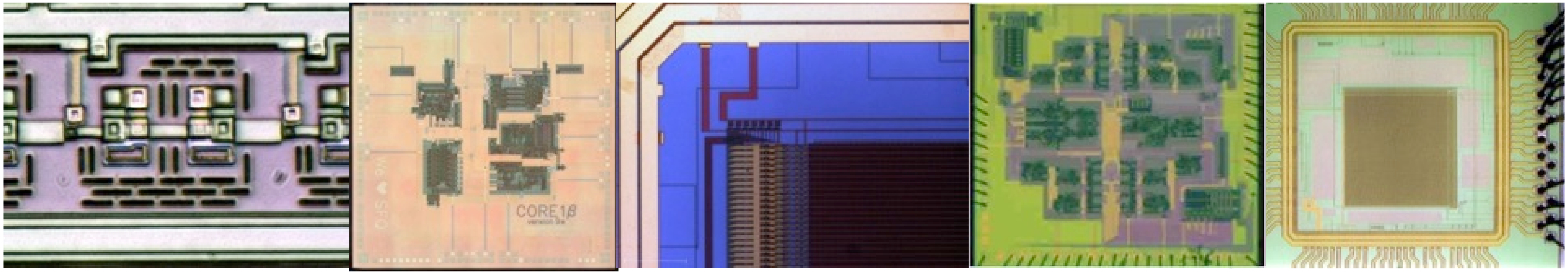
IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2017.
Invited presentation 4EO1-01 given at EUCAS, 17-21 September 2017, Geneva, Switzerland.

YNU Initiative for Global Arts & Sciences
YOKOHAMA National University

13th European Conference on Applied Superconductivity,
Geneva, 17-21 September 2017



Recent research developments of adiabatic quantum-flux-parametron circuits technology toward energy-efficient high-performance computing

N. Yoshikawa[1,2], N. Takeuchi[2], C.L. Ayala[2], Q. Xu[2], K. Fang[1], N. Tsuji[1], F. China[1], Y. Murai[1], T. Ortlepp[2,3], Y. Yamanashi[1,2]

[1]*Department of Electrical and Computer Engineering, Yokohama National University, Japan*

[2]*Institute of Advanced Sciences, Yokohama National University, Japan*

[3]*The CiS Research Institute for Microsensor Systems GmbH, Germany*

EUCAS 2017

The circuit was fabricated using ISTEC standard process (STP2). National Institute of Advanced Industrial Science and Technology partially contributed to the circuit fabrication.

Institute of Advanced Sciences
Yokohama National University

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Outline

- Background and motivation
- Operation principle of adiabatic quantum flux parametron (AQFP)
- AQFP as an energy-efficient logic circuit
  - Evaluation of AQFP as a logic circuit
- Design methodology of AQFP logic circuits
- EDA tools for Top-Down design
- Summary

Background

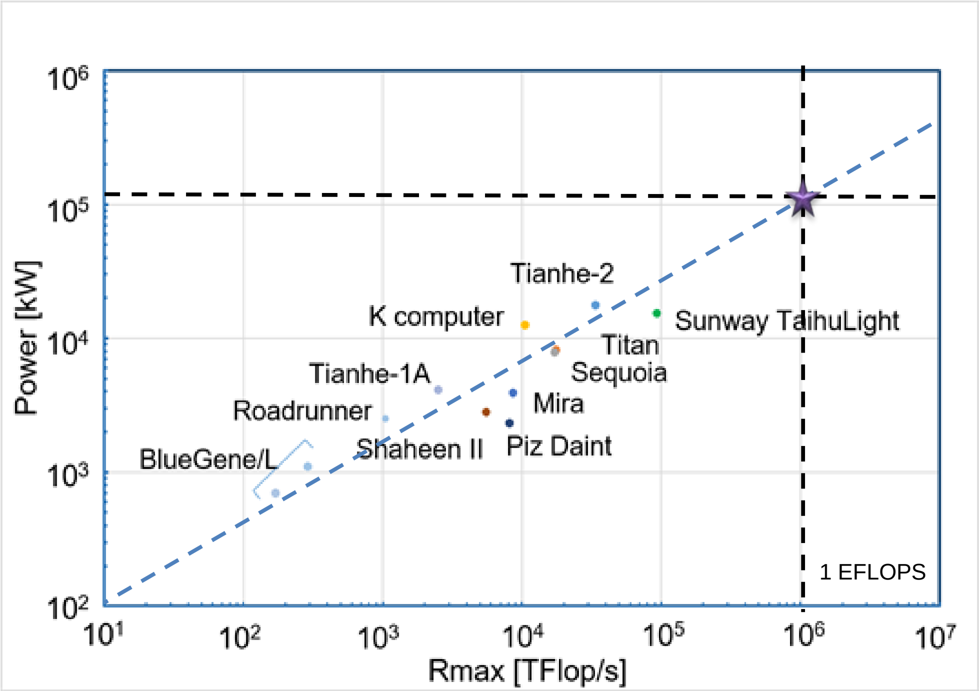
Estimated power consumption to realize an exa-scale computer

> 100 MW
~ $million/100 MW per year

K computer (Japan)

Peak performance: 10.5 PFLOPS
Power consumption: 12.6 MW

1st-ranked computers in recent TOP500



http://www.top500.org/

Low-Power Logic Devices is highly demanded.

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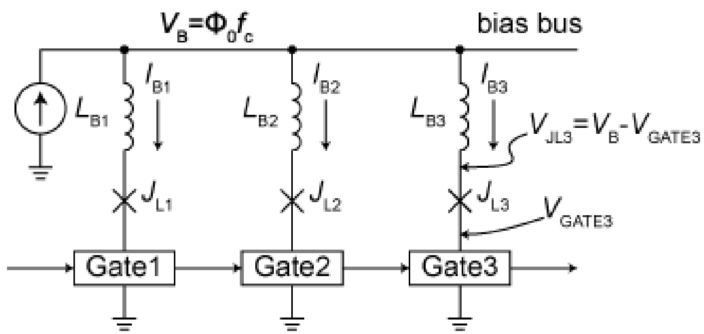
Energy-Efficient SFQ Circuits

DC Powered	AC Powered

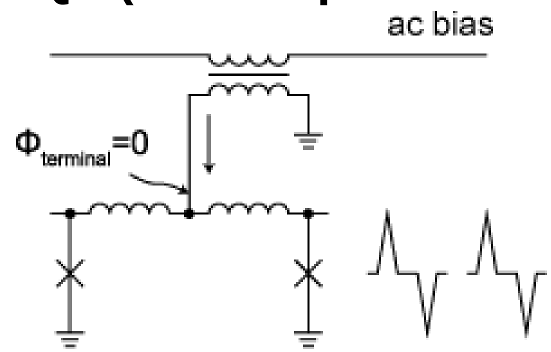
ERSFQ (Hypres)



$P_S \sim P_D \sim I_c\Phi_0 f$

O. A. Mukhanov, *IEEE Trans. Appl. Supercond.* **21**, 760 (2011).

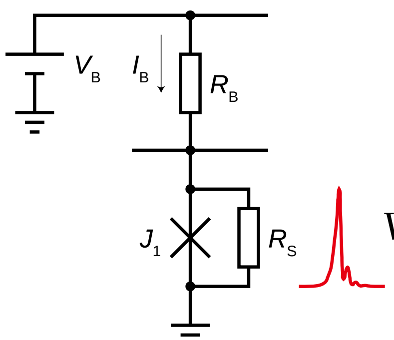
RQL (Northrop Grumman)



$P_S \sim 0,\ P_D \sim I_c\Phi_0 f$

Q. P. Herr *et al.*, *J. Appl. Phys.* **109**, 103903 (2011).

LV-SFQ (Nagoya Univ.)

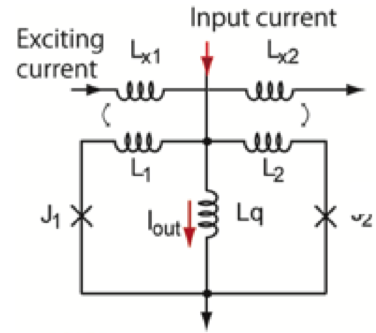


$P_S \sim 5P_D,\ P_D \sim I_c\Phi_0 f$

$$V=\frac{\Phi_0}{2\pi}\frac{d\varphi}{dt}$$

M. Tanaka *et al. JJAP* **5** 1053102 (2012)

AQFP (Yokohama National Univ.)



$P_S \sim 0,\ P_D < I_c\Phi_0 f$

N. Takeuchi, *et. al.*, *SUST*, 26, 035010 (2013).

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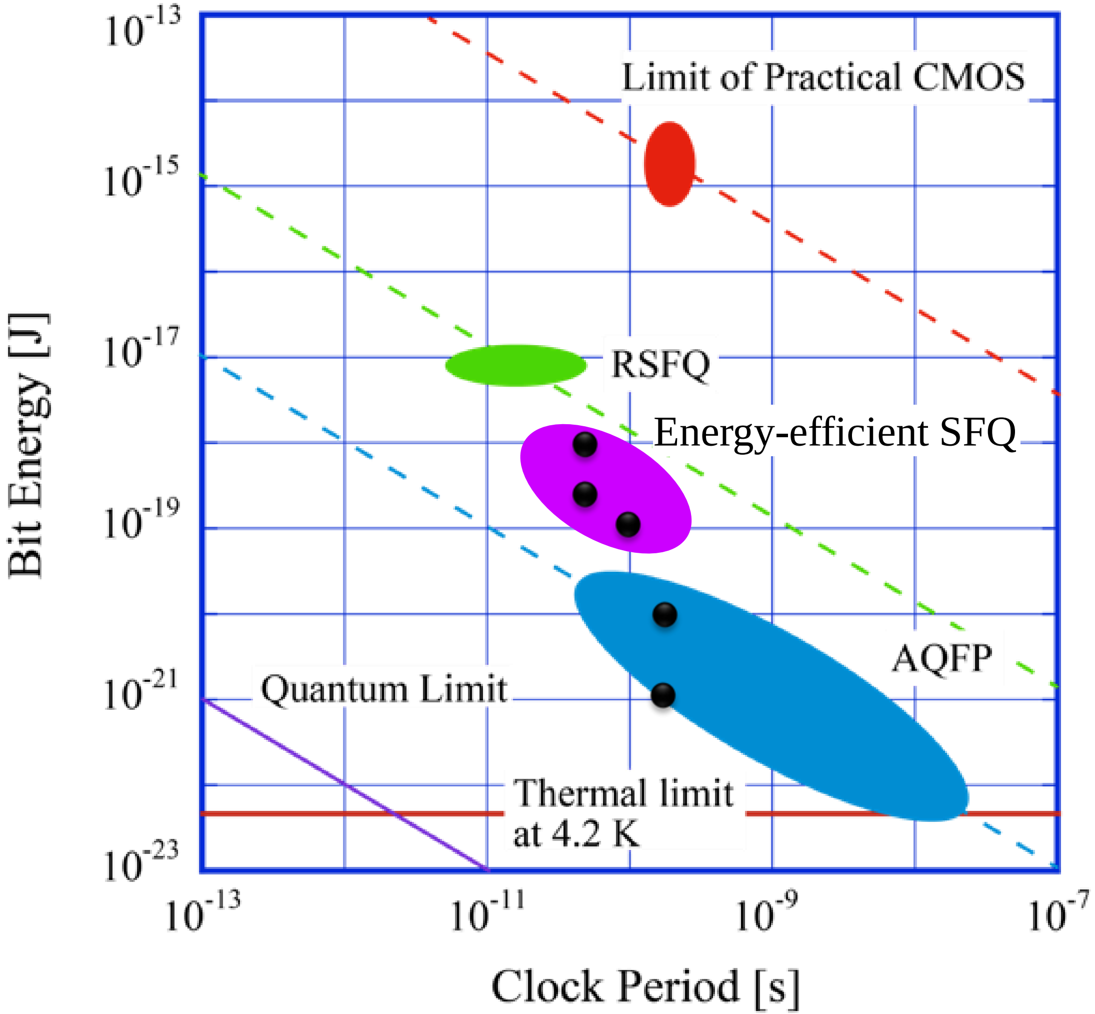
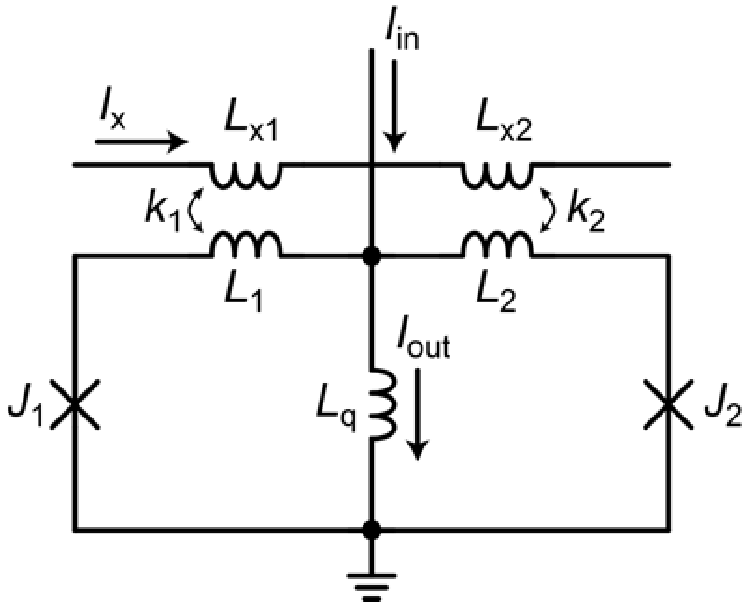
Comparison of Energy-Delay Product



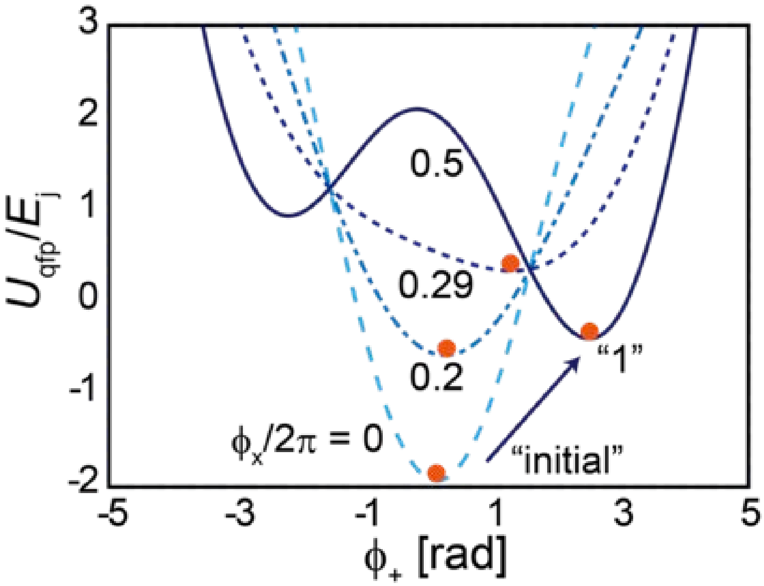
Adiabatic Quantum-Flux-Parametron (AQFP)

AQFP gate



An SFQ is stored in the right or left loop depending on I_{in}.

Potential energy of the gate



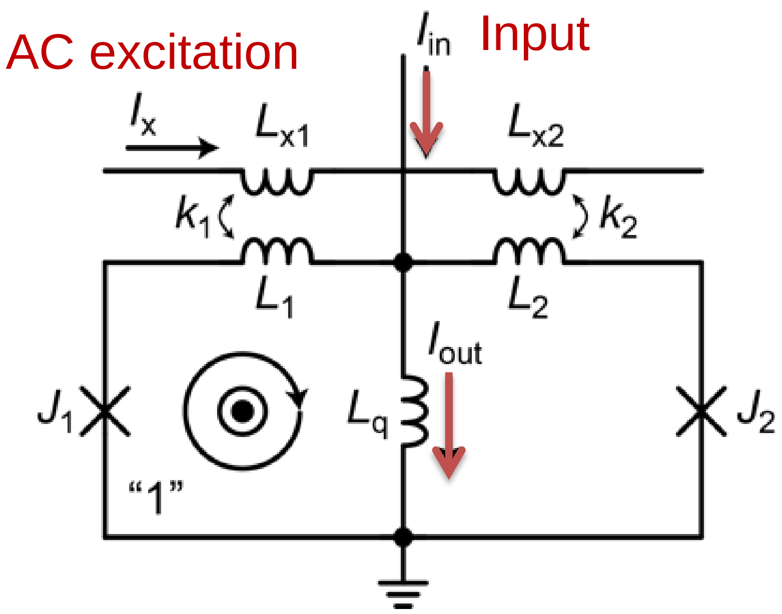
Potential energy changes adiabatically during switching.

Operation principle is based on QFP gates.

M. Hosoya et al., *IEEE Trans. Appl. Supercond.* 1, 77–89 (1991).

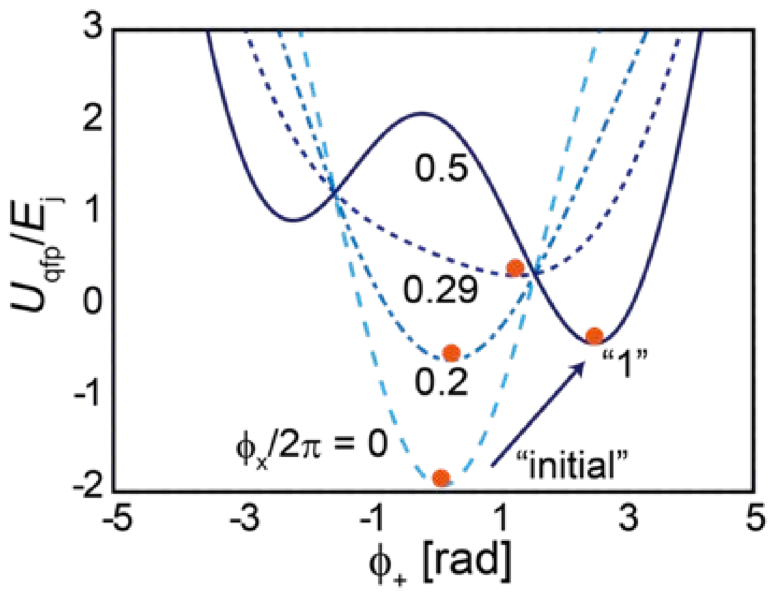
Adiabatic Quantum-Flux-Parametron (AQFP)

AQFP gate



I_{out} flows downward.

Potential energy of the gate



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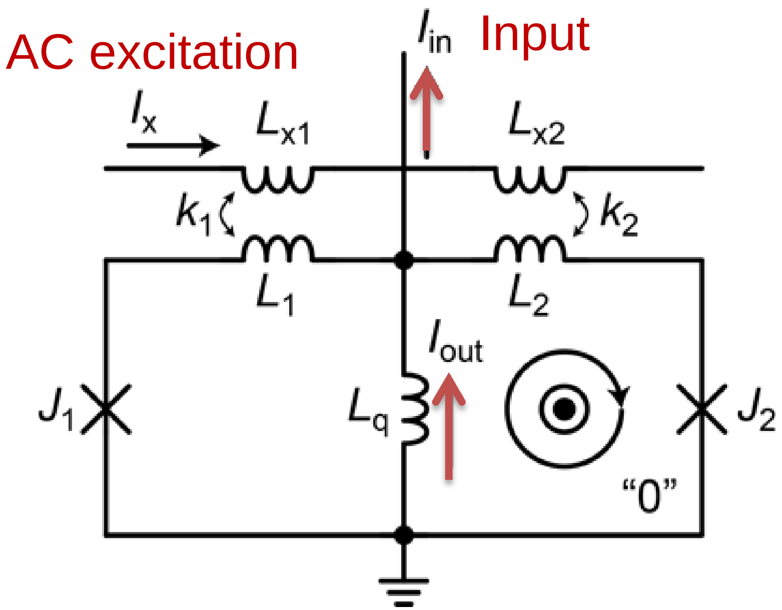
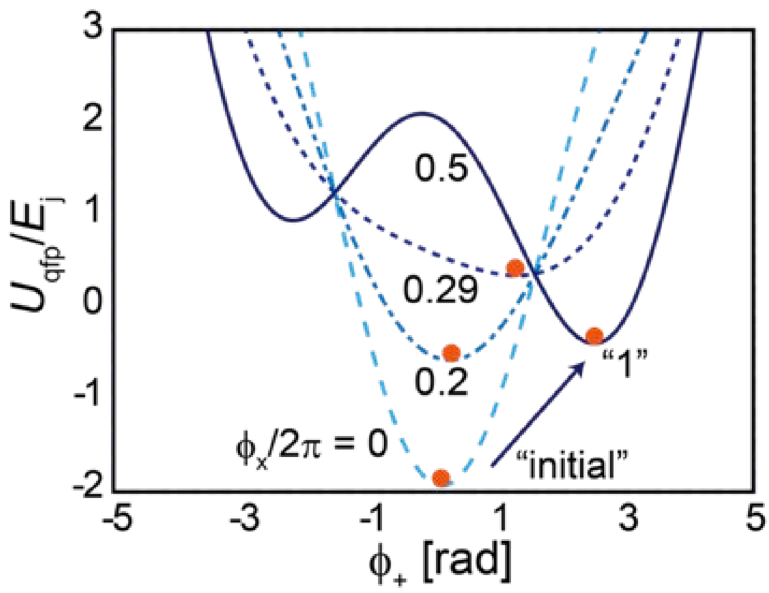
Adiabatic Quantum-Flux-Parametron (AQFP)

AQFP gate



I_{out} flows upward.

Potential energy of the gate

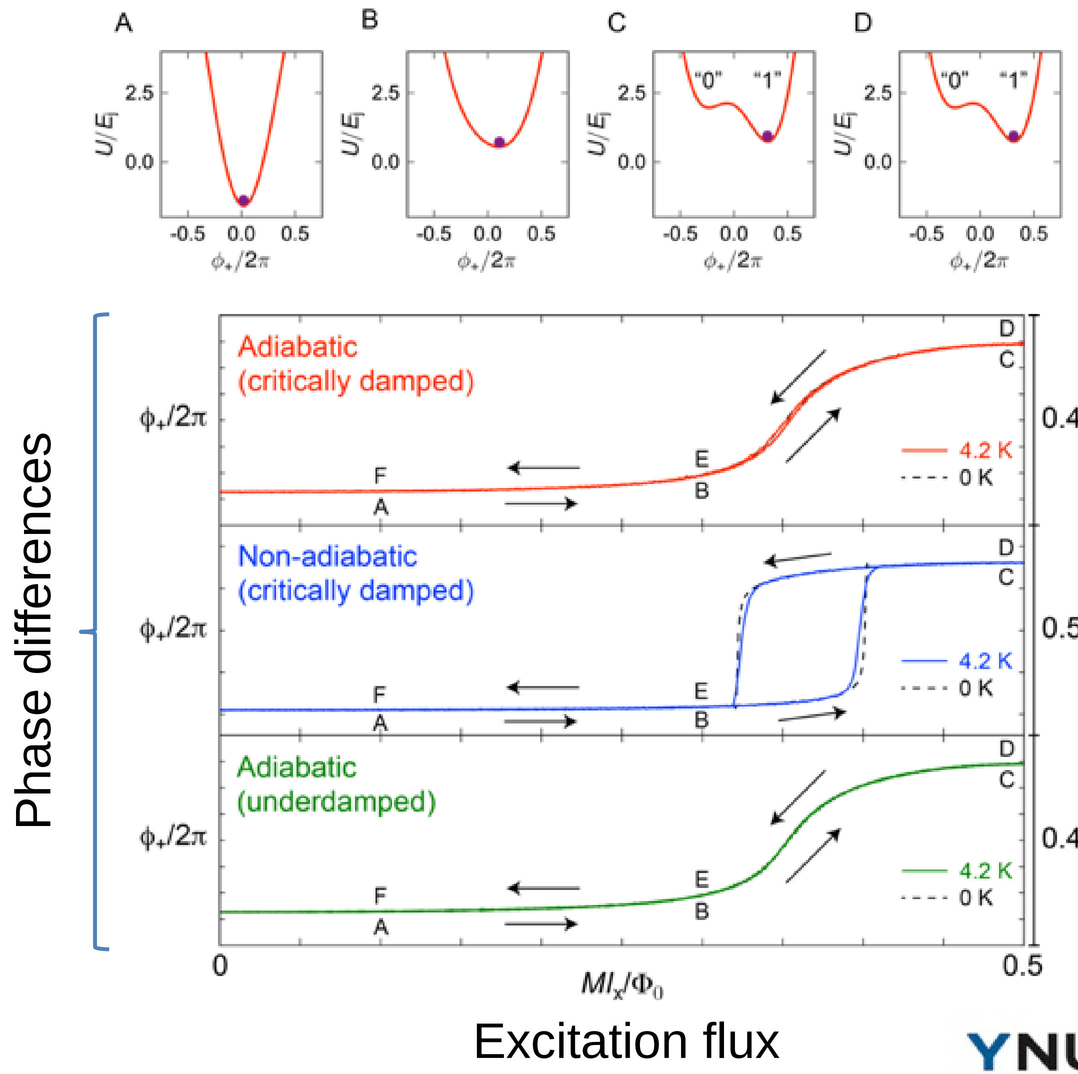


Potential energy changes adiabatically during switching.

Operation principle is based on QFP gates.

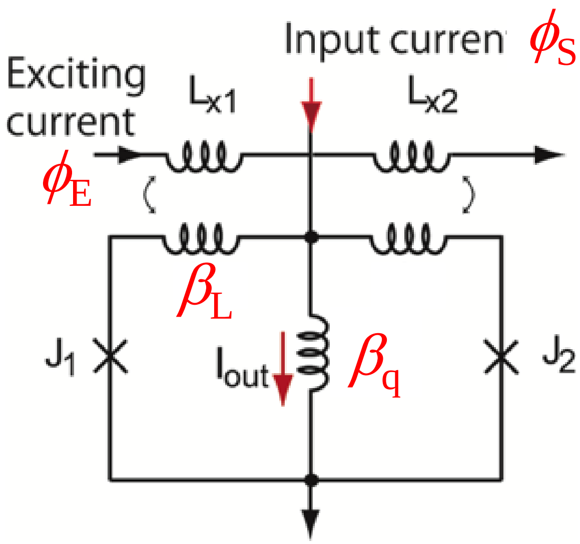
M. Hosoya et al., *IEEE Trans. Appl. Supercond.* 1, 77–89 (1991).

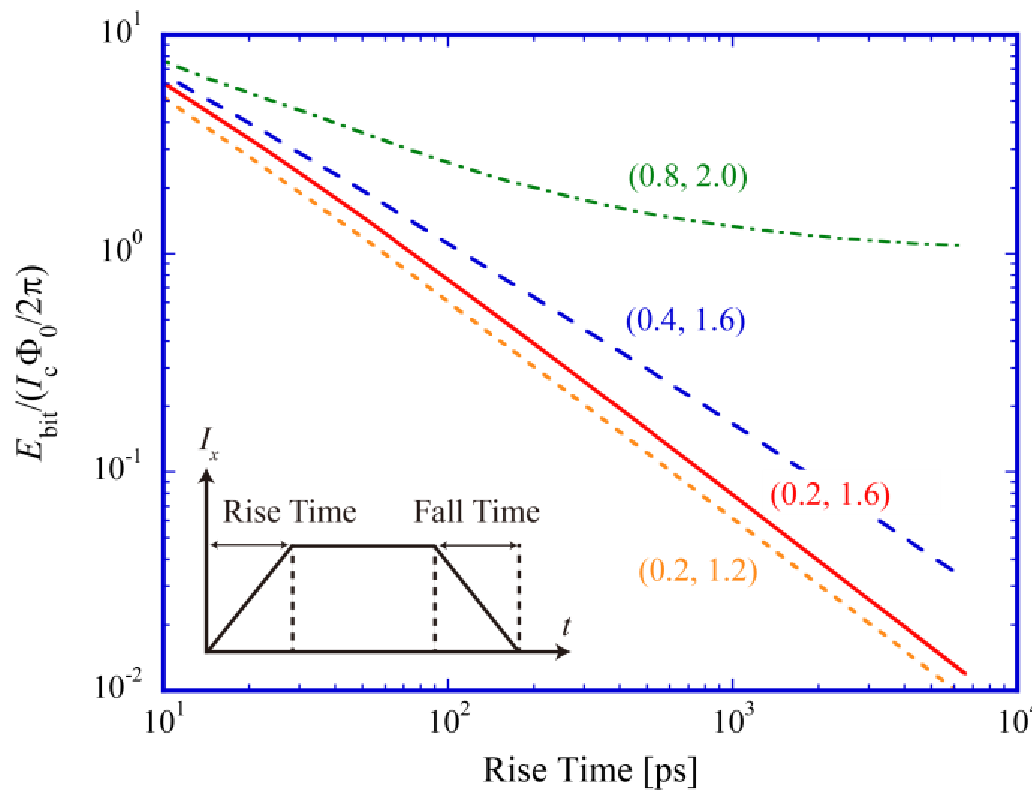
Evolution of Junction Phase at 4.2 K



The phase of junctions in AQFP gates change adiabatically even at a finite temperature.

Bit Energy vs. Clock Period of AQFP





Energy dissipation $\propto f$

When rise time is 1000 ps, $E_{bit} = 0.023\ I_c\Phi_0$ (~ $20k_BT$).

→ 1/1000 of RSFQ

N. Takeuchi, *et.* al., *SUST*, 26, 035010 (2013).

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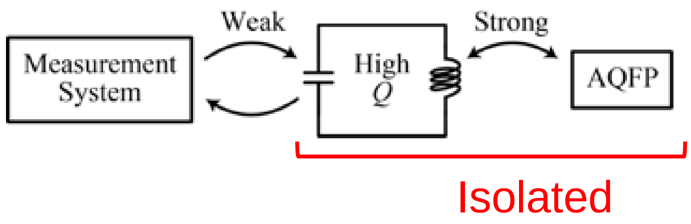
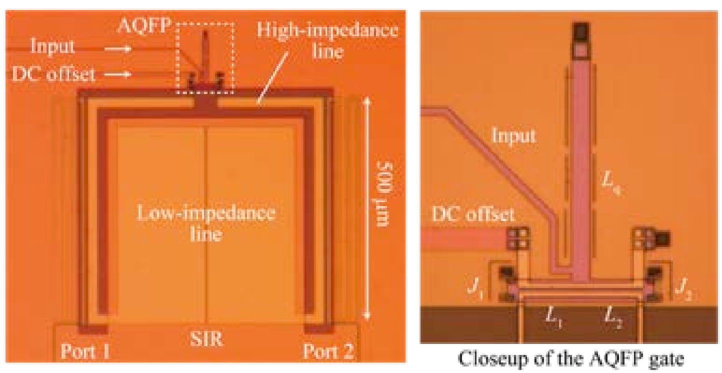
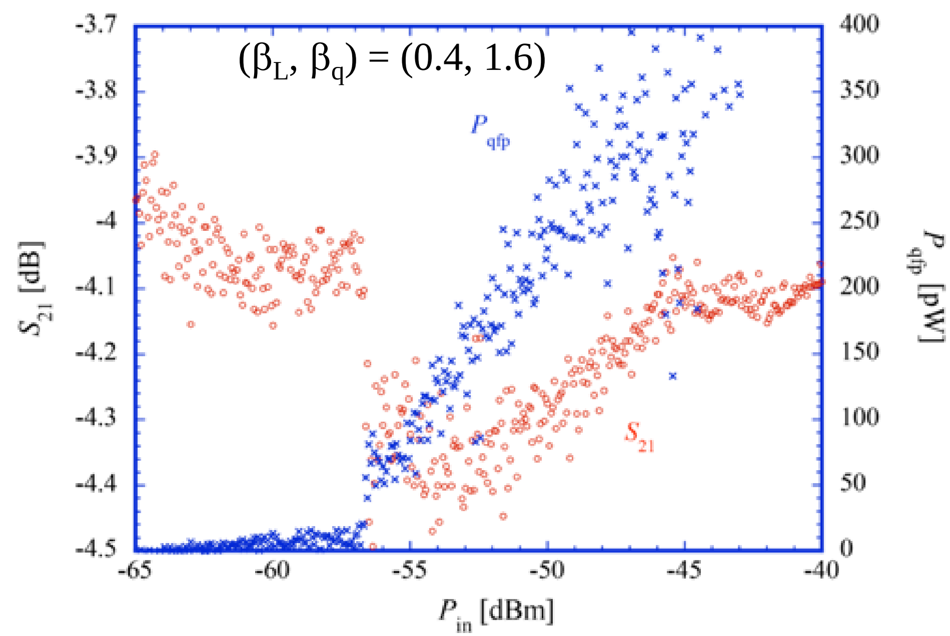
Bit Energy Measurement of AQFP using a Superconducting Resonator





Measured power consumption of AQFP



Clock frequency: 4.998 GHz
Q of resonator : 357

P_{qfp} ~ 50 pW

E_{bit} ~ 10 zJ ~ $170 k_B T$

CRAVITY AIST

AIST Nb Josephson standard process (STP2) was used.

N. Takeuchi, *et. al.*, *Appl. Phys. Lett.*, 102, 052602 (2013).

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Comparison of Superconducting Logics

Logic	Clock Freq. [GHz]	$E_{bit} / I_c\Phi_0$	Typical I_c [μA]	EDP [aJ·ps]
CMOS	4	-	-	~10^5
RSFQ [1]	50	19	150	120
eSFQ [2]	20	0.8	150	12
RQL [3]	10	0.33	150	10
LV-RSFQ [4]	20	3.5	150	54
AQFP [5]	5	0.0042	50	0.086
Quantum limit	-	-	-	5.3×10^{-5}

[1] X. Peng et al., IEICE Trans. Electron. **E97.C**, 188 (2014).
[2] M. H. Volkmann et al., Supercond. Sci. Technol. **26**, 015002 (2013).
[3] Q. P. Herr et al., J. Appl. Phys. **109**, 103903 (2011).
[4] M. Tanaka et al., IEEE Trans. Appl. Supercond. **23**, 1701104 (2013).
[5] N. Takeuchi et al., Supercond. Sci. Technol. 28, 015003 (2015).

Evaluation of AQFP as a Logic Circuit

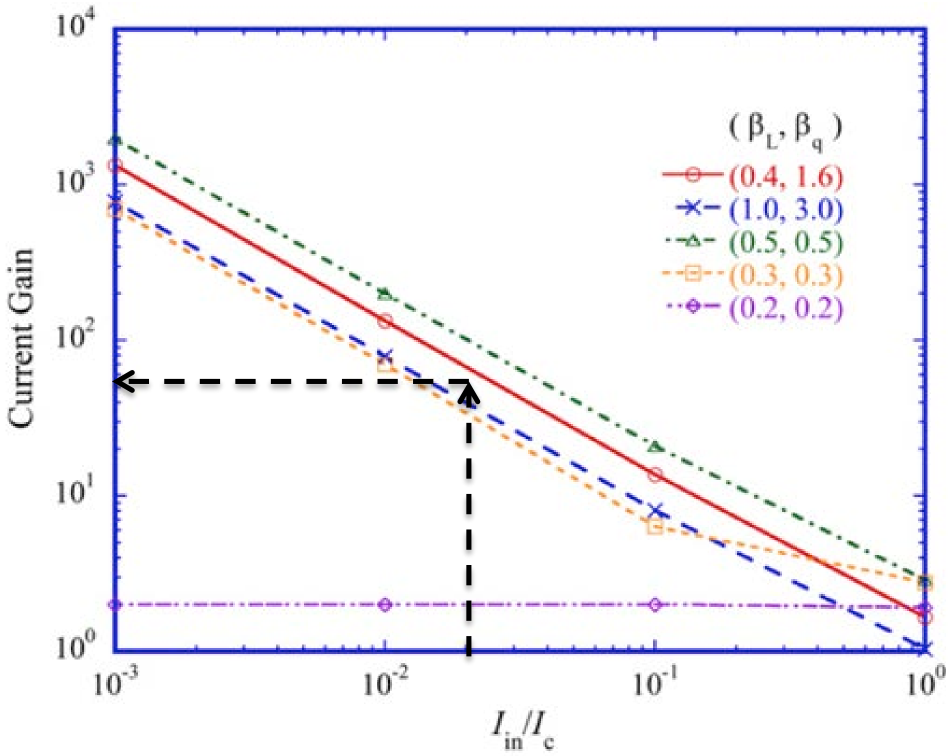
Important metrics as a logic circuit

- Gain
- Functionality
- Speed
- Energy consumption
- Driving ability
- Connectability
- Error rates
- Robustness
- Density

Gain

- Current gain of AQFP is considerably large.

Current gain vs. input current at T = 0K



If we assume

δI_{in} ~ 1 μA, and I_c = 50 μA,

the current gain is given by

$I_c / \delta I_{in}$ ~ 50.

δI_{in}: input thermal noise

cf. In RSFQ circuits with

I_{in} ~ 20 μA, I_c = 100 μA,

the current gain is ~ 5.

N. Takeuchi, *et. al*., *SUST*, 26, 035010 (2013).

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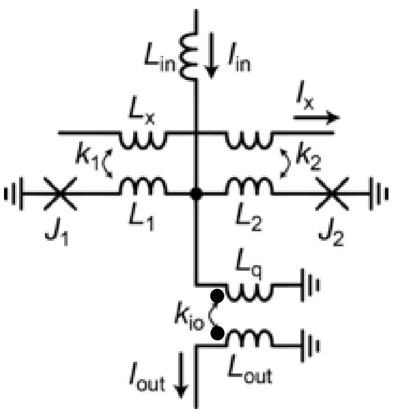
Functionality

- NOT gate is cost free.
- Majority gate is a basic logic gate.

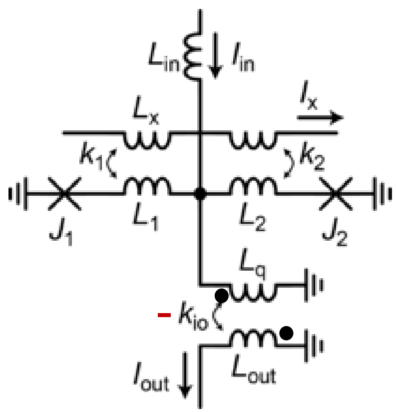
NOT gate is made by using a transformer with negative coupling.

Majority gate is made by connecting three buffers in parallel.

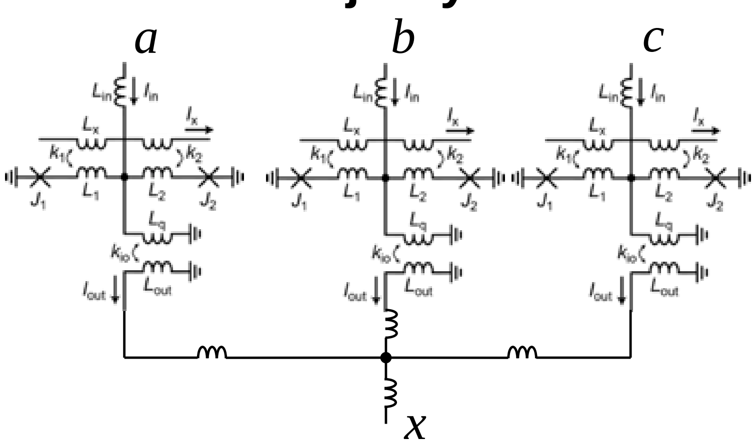
Buffer



NOT



Majority



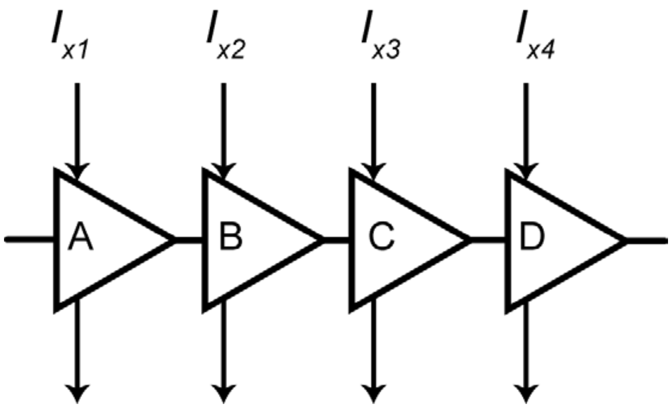
$$x = \mathrm{MAJ}(a, b, c) = ab + bc + ac$$

K. Inoue, *et al*. IEEE Trans. Appl. Supercond., **23**, 1301105 (2013).

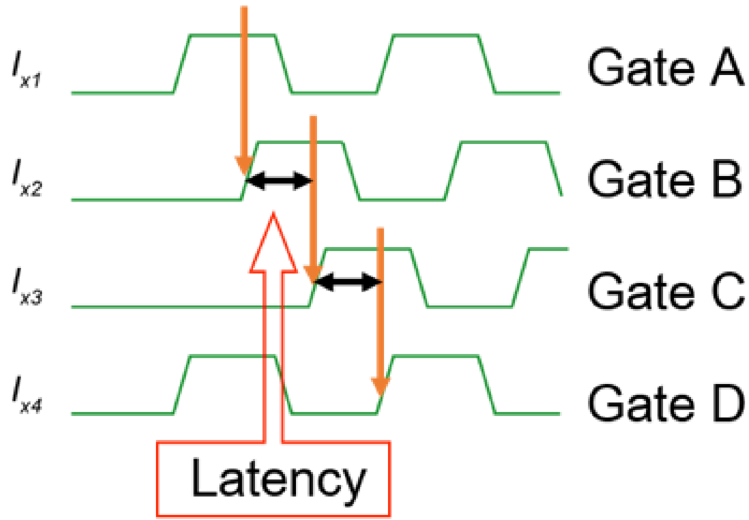
Speed

- AQFP is driven by multi-phase clocks. (4-phase is typically used.)
- Target clock frequency is 5 GHz.
- Double excitation method can increases the clock frequency [1].
- Latency is improved by increasing the number of phase.

Clocking of AQFP gates



$$Latency = \frac{clock\ period}{number\ of\ phase}$$

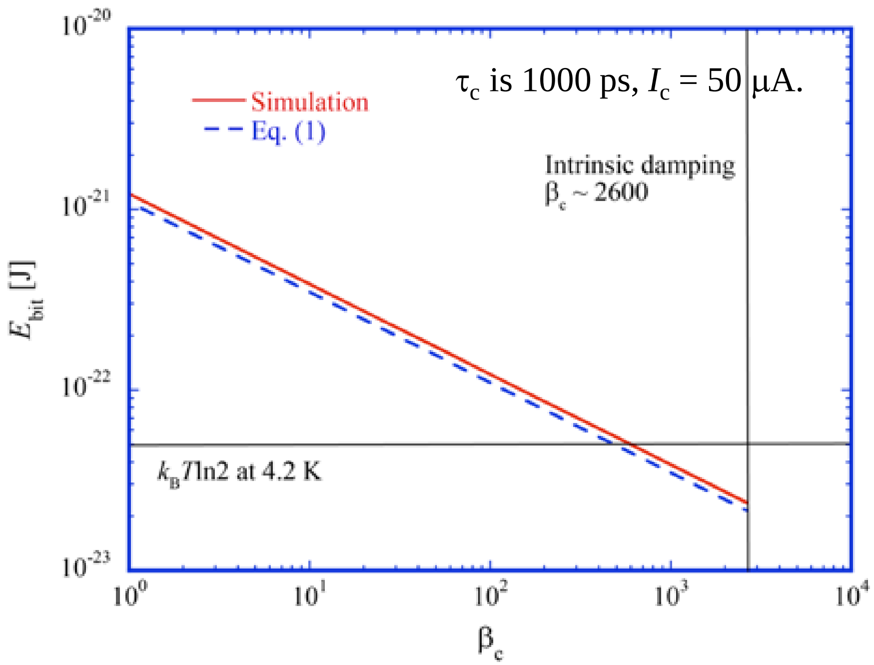


[1] K. Fang, J. Appl. Phys., **121**, 143901 (2017).

Energy Consumption

- The static energy consumption is zero, the dynamic energy consumption is proportional to the clock frequency.
- The energy consumption is decreased by using high-J_c and high-β_c junctions.

β_c Dependence of Bit-Energy of AQFP



Bit energy:

$$E_{bit} = 2 I_c \Phi_0 \frac{\tau_{sw}}{\tau_{rf}}$$

Intrinsic switching time:

$$\tau_{sw} \approx \frac{\Phi_0}{I_c R} = \sqrt{\frac{2\pi \Phi_0 c}{\beta_c j_c}}$$

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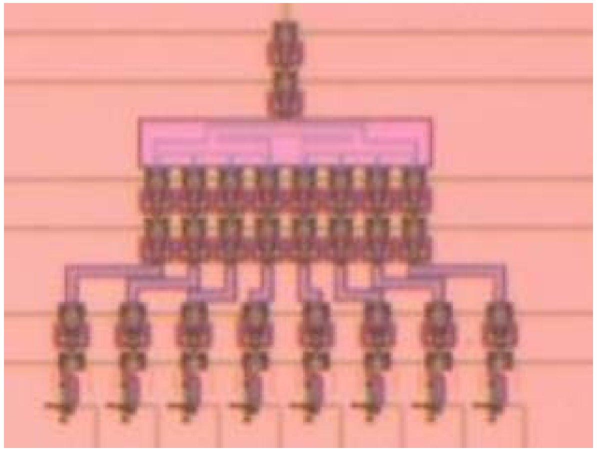
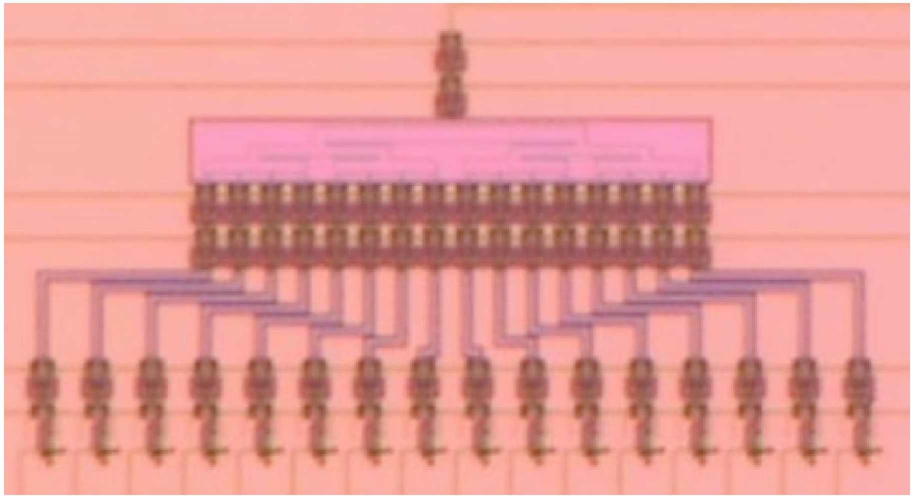
Driving Ability

- Fan-out of AQFP gate is large (4 ~ 16).

1:8 splitter



1:16 splitter



(cf. Fan-out of RSFQ circuits: 2 ~ 3.)

CRAVITY AIST

AIST Nb Josephson standard process (STP2) was used.

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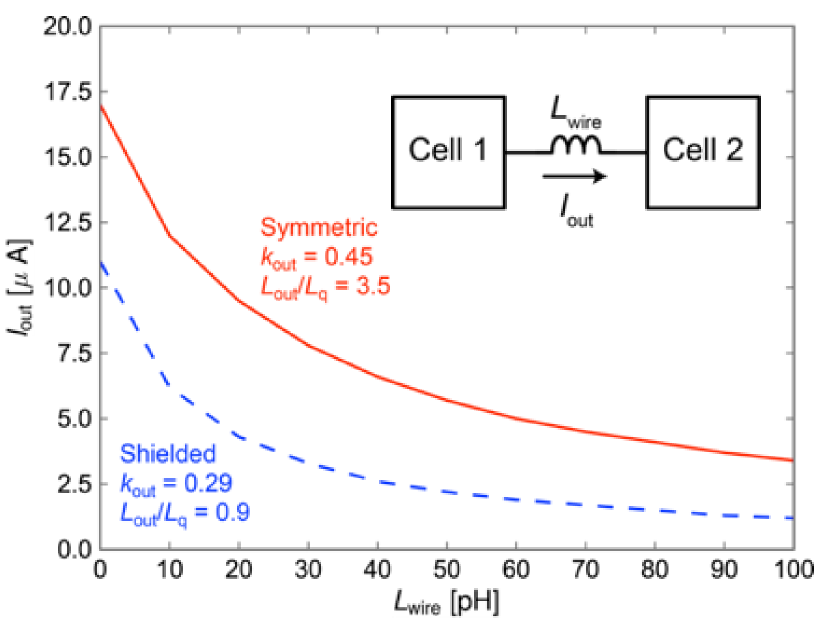
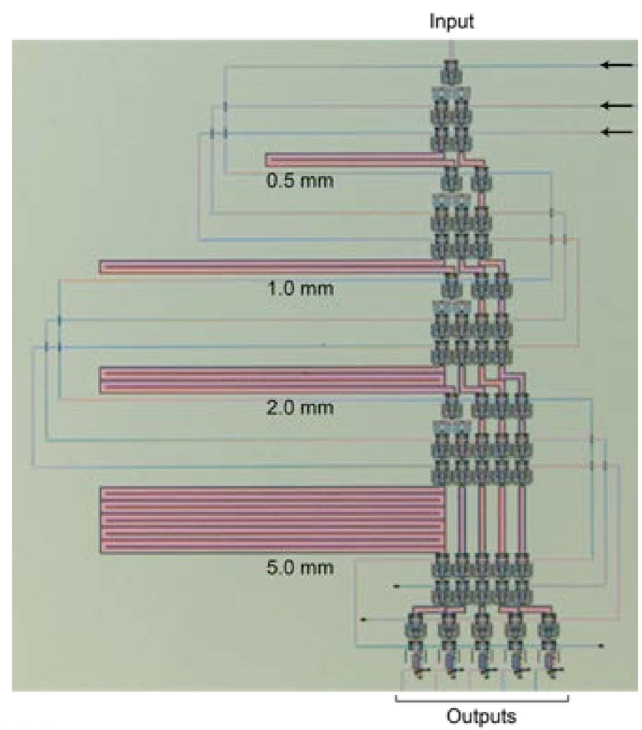
Connectability

- The output current of AQFP gate decreases with increase of interconnect inductance, which limits the wire length.
- L_{max} ~ 1 mm.

I_{out} vs. L_{wire}



Testing of maximum wiring length



N. Takeuchi et al., J. Appl. Phys. **117**, 173912 (2015).

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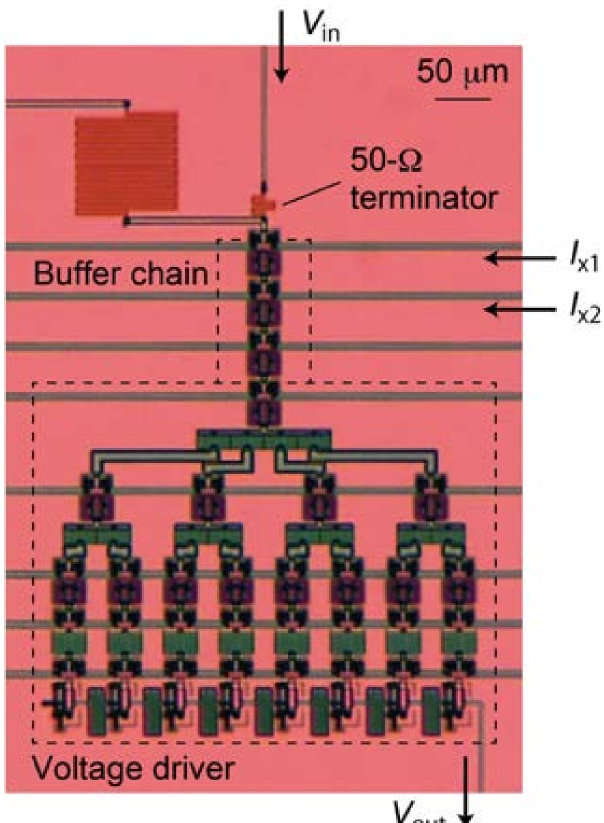
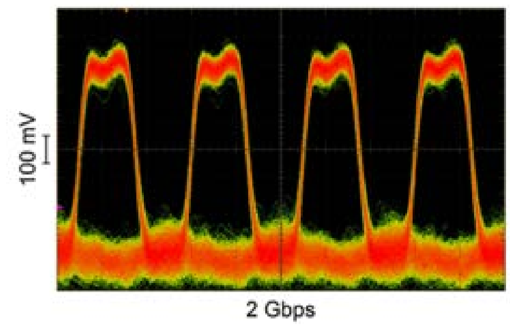
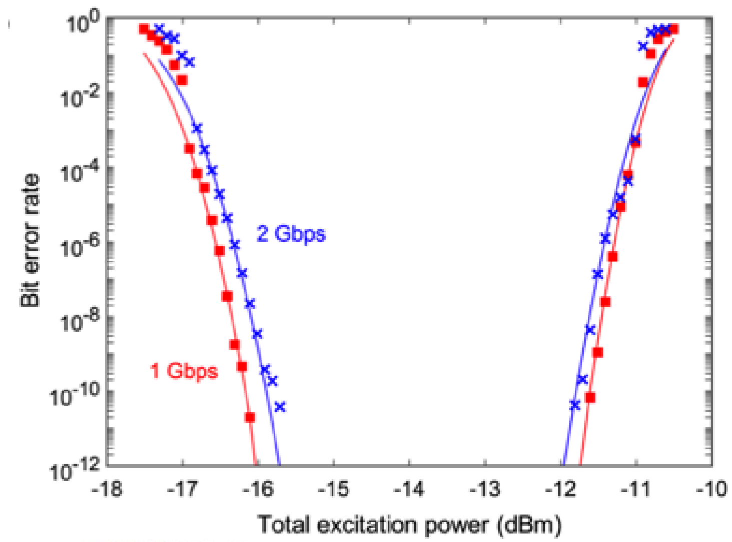
Error Rates

- Bit-error-rate of AQFP gate is quite small when $E_J >> k_B T$.

2 GHz bit-error-rate test results







N. Takeuchi, *et al.*, Appl. Phys. Lett., **110**, 202601 (2017).

CRAVITY AIST

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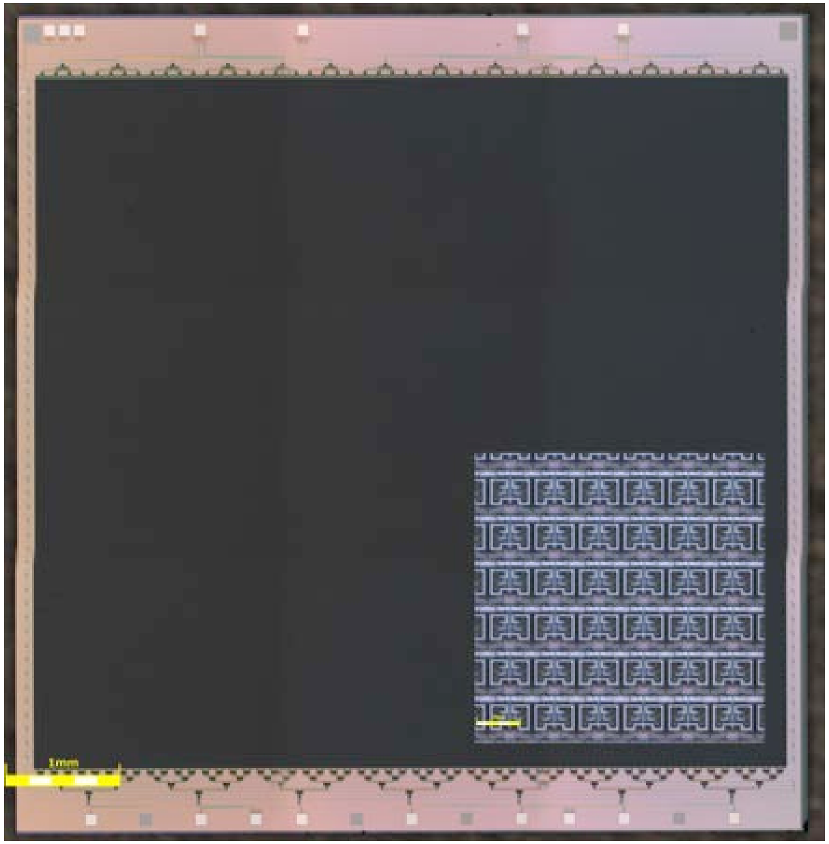
Robustness

Demonstrated 84k-Junction AQFP buffer array



- AQFP is robust because
  - The operation is based on differential pairs of junctions and inductances.
  - The critical current of all junctions is the same.

Area	6.68 × 6.23 mm^2
Bias Current	3.60 mA
JJ number	83736

AIST 10 kA/cm^2 high-speed standard process (HSTP) was used.

CRAVITY AIST

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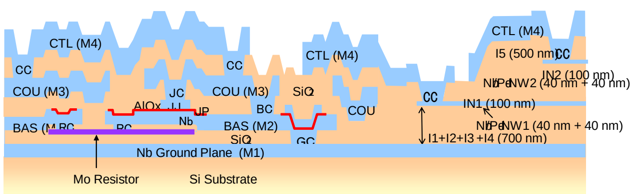
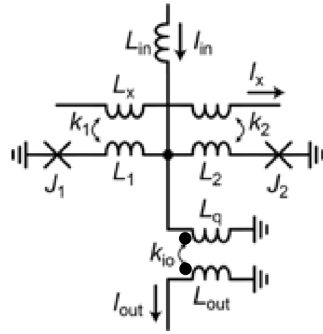
Density

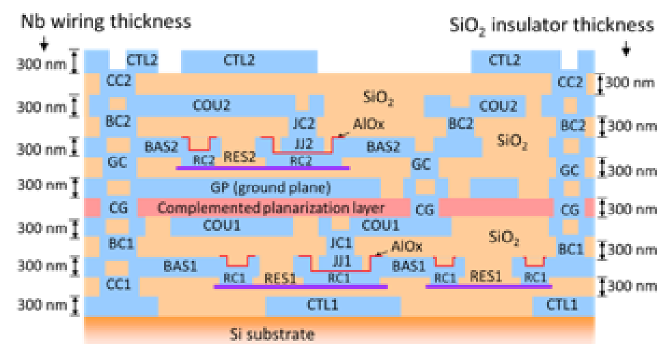
- Multi-layer processes improve the circuit density.

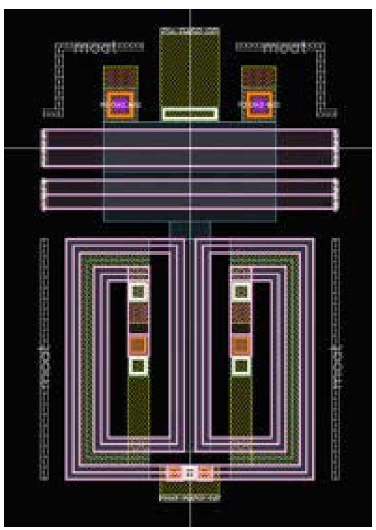
4-metal layer process



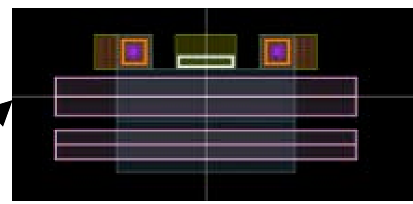


7-metal layer process

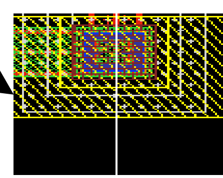




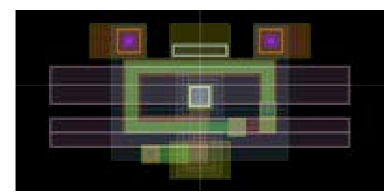
$40 \times 25\ \mu m^2$



Excitation line
(upper layers)



Transformer
(lower layers)



$13 \times 25\ \mu m^2$
(-67.5% area reduction)

~ 0.3M gate/cm^2

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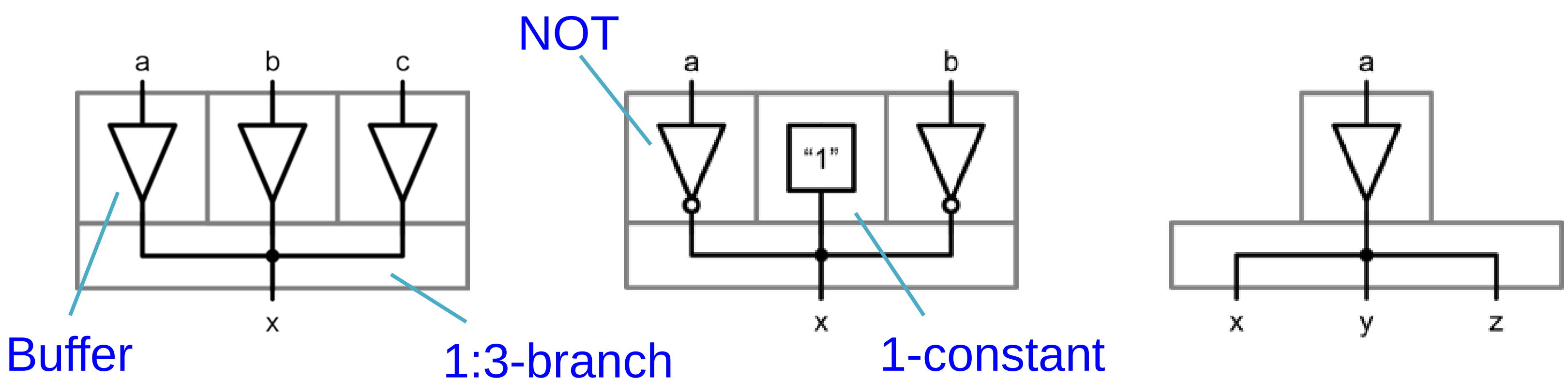
Design Methodology

- Logic cells can be designed by placing four building blocks: Buffer, NOT, Constant, Branch

Majority **NAND** **Splitter**



$$x = \mathrm{MAJ}(a,b,c) = a \cdot b + b \cdot c + c \cdot a$$

$$x = \mathrm{MAJ}(\bar{a},1,\bar{b}) = \bar{a} + \bar{b} = \overline{ab}$$

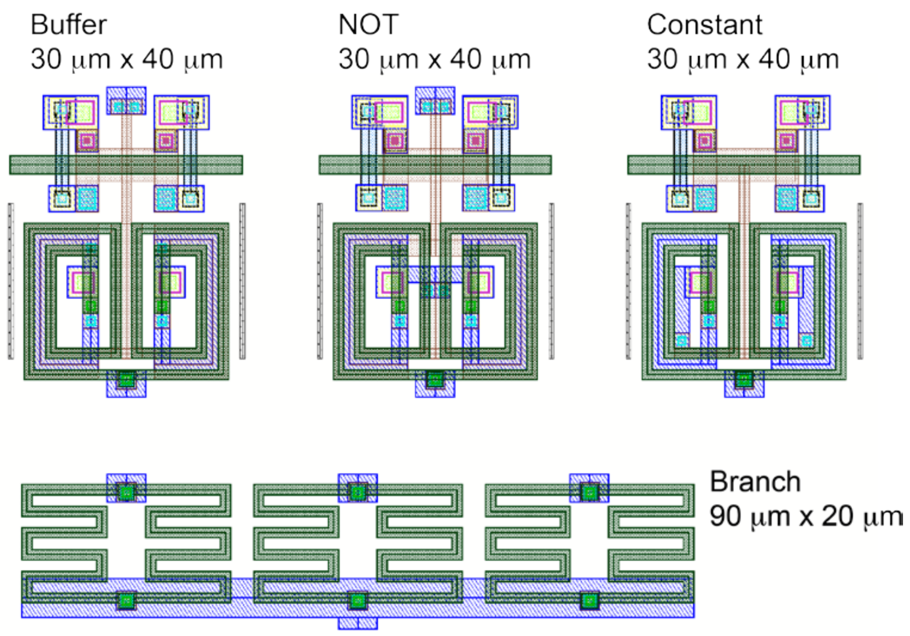
$$x = y = z = a$$

N. Takeuchi *et al.*, J. Appl. Phys. **117**, 173912 (2015).

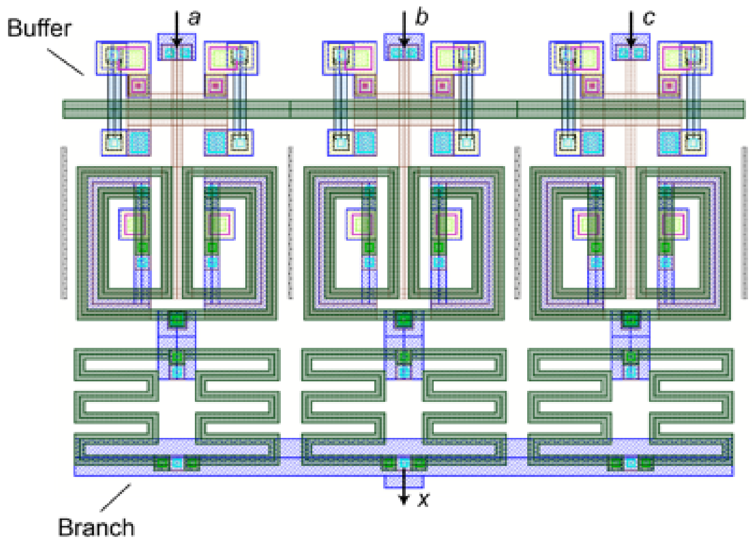
Layout of Basic Cells

- Symmetric design prevents the parasitic coupling between the excitation and output inductance.

Building block cells

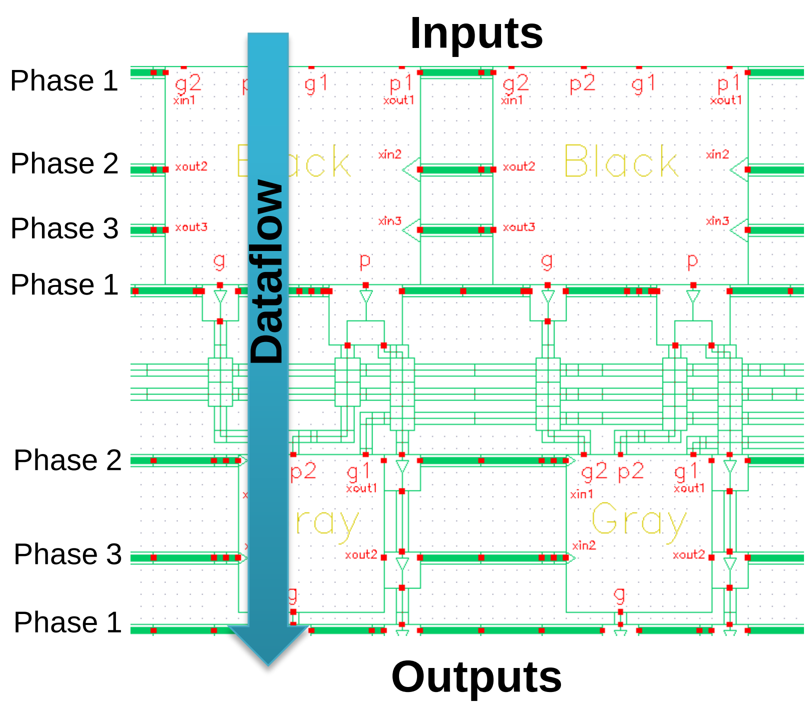


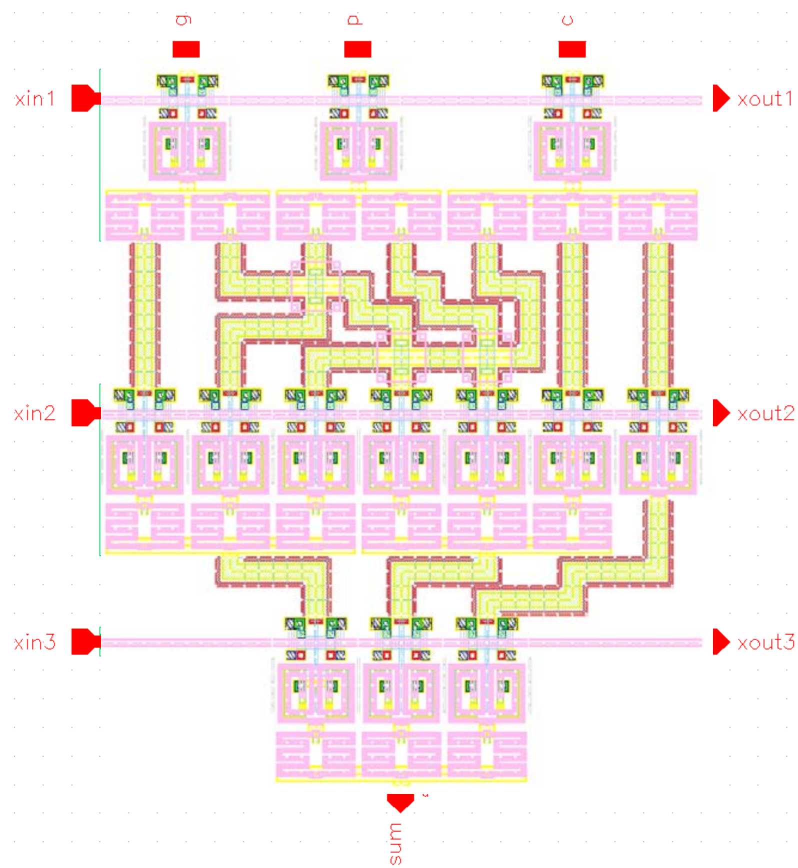
Majority cell



N. Takeuchi *et al*., J. Appl. Phys. **117**, 173912 (2015).

AQFP Logic Design





- Logic cells are placed together like Lego blocks
- Logic gates grouped by phase & data flow

AQFP design flow

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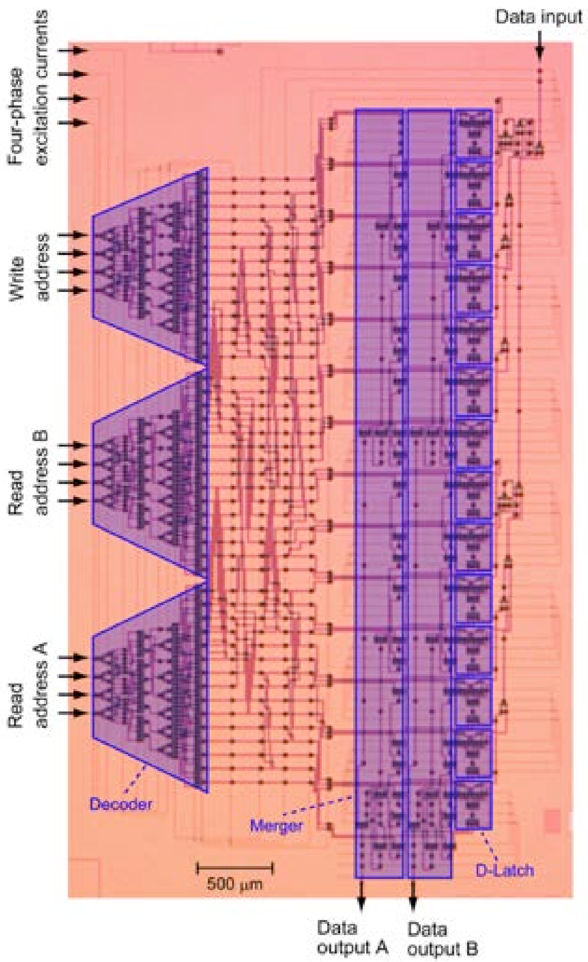
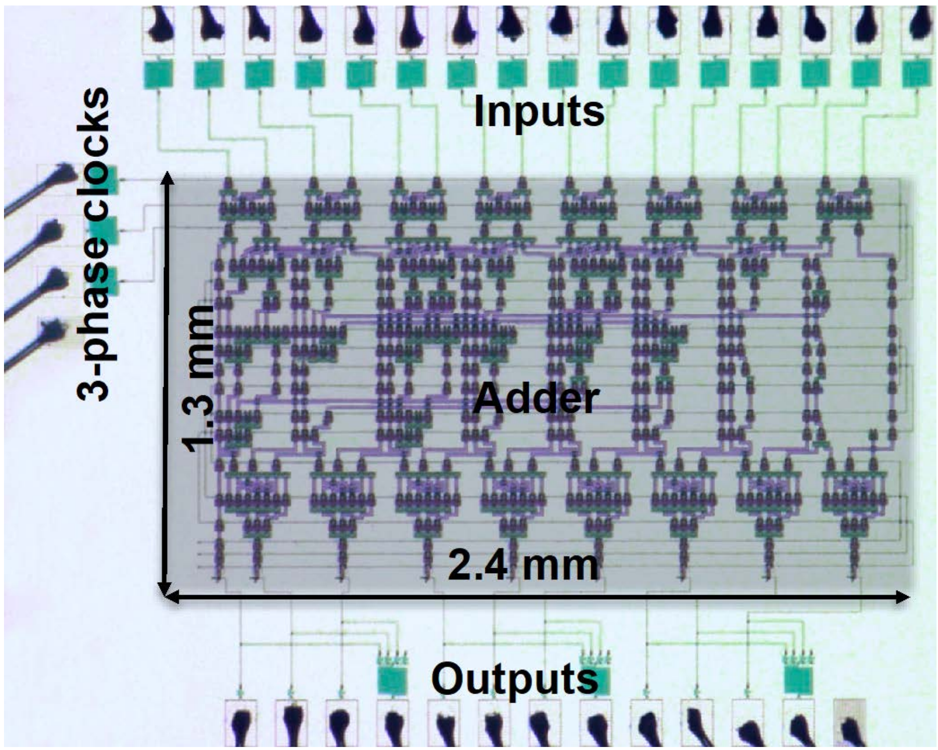
Demonstrated AQFP Circuits

16-word by 1-bit register file



N. Tsuji et al., IEEE Trans. Appl. Supercond., **27** (2017).

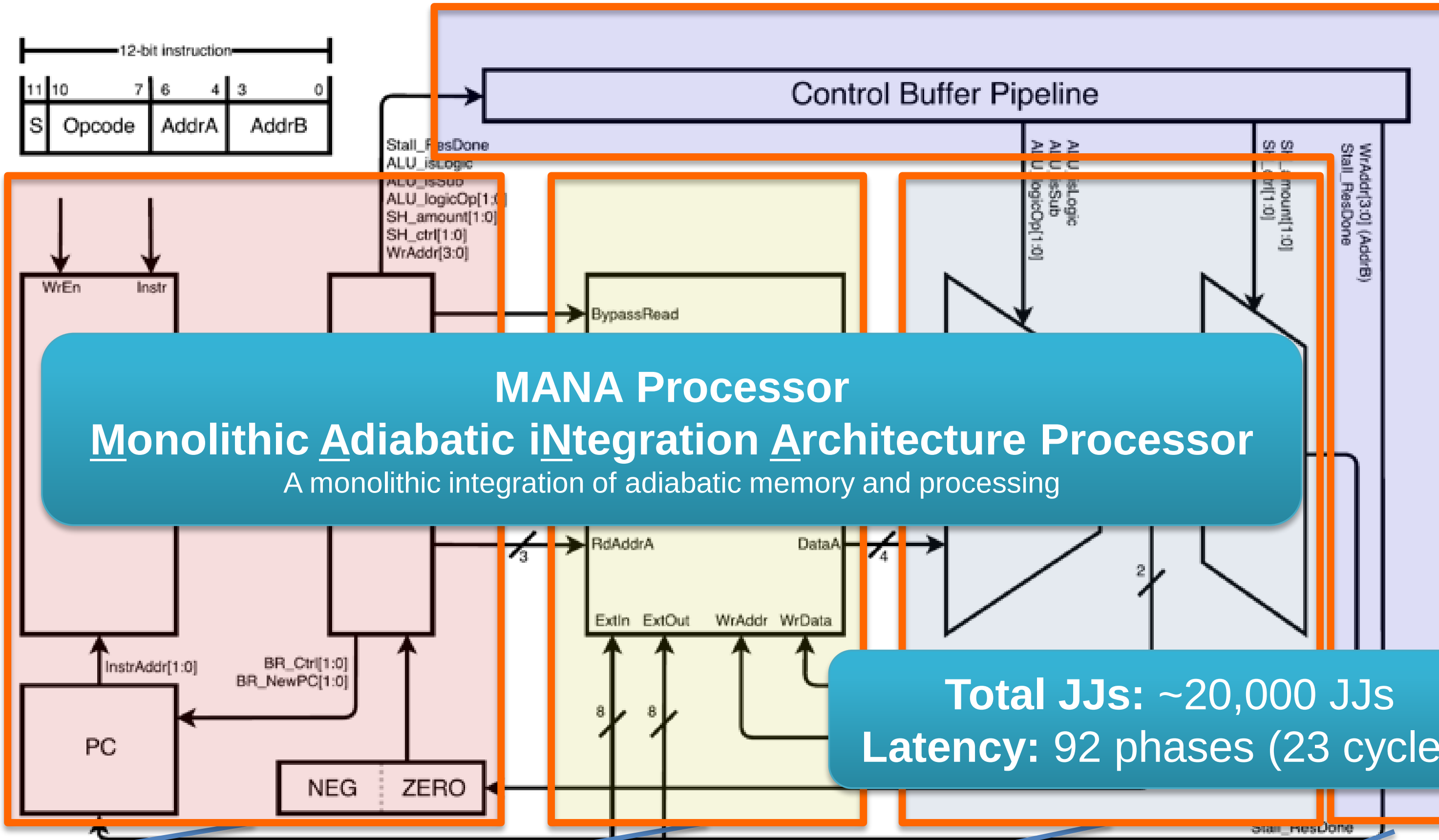
8-bit carry look-ahead adder



C. L. Ayala et al., IEEE Trans. Appl. Supercond., **27** (2017).

IEEE/CSC & ESAS SUPERCONDUCTIVITY NEWS FORUM (global edition), October 2017.
Invited presentation 4EO1-01 given at EUCAS, 17-21 September 2017, Geneva, Switzerland.

4-bit AQFP RISC Microarchitecture



MANA Processor

Monolithic Adiabatic iNtegration Architecture Processor

A monolithic integration of adiabatic memory and processing

Total JJs: ~20,000 JJs
Latency: 92 phases (23 cycles)

Instruction Buffer, Decode, and Issue	Register File with bypass Ext. I/O	ALU, Shifter	Control Pipeline, Routing
4988 JJs, 22 phases	**7892 JJs, 20 phases**	**1556 JJs, 20 phases**	**5148 JJs, 66 phases***

EUCAS2017, 1EP1-6, 1EP1-12

*overlapped with pipeline

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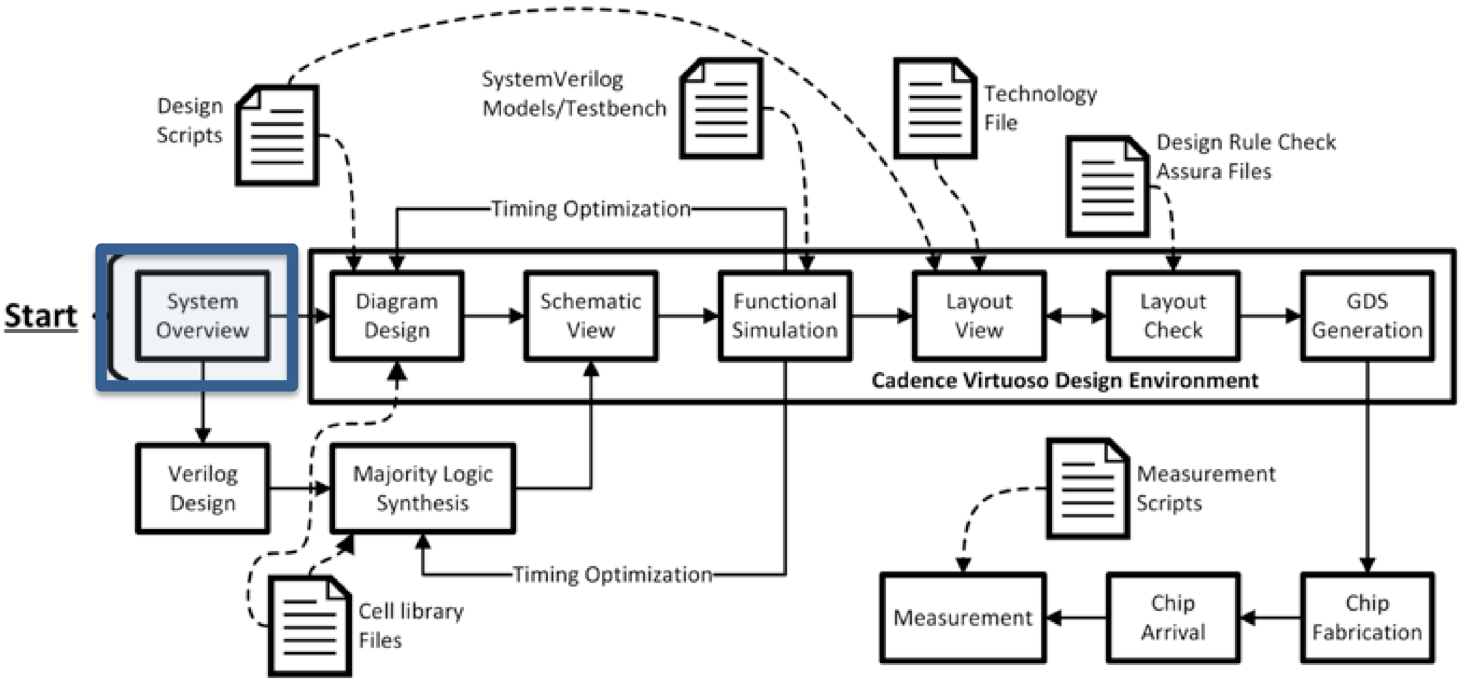
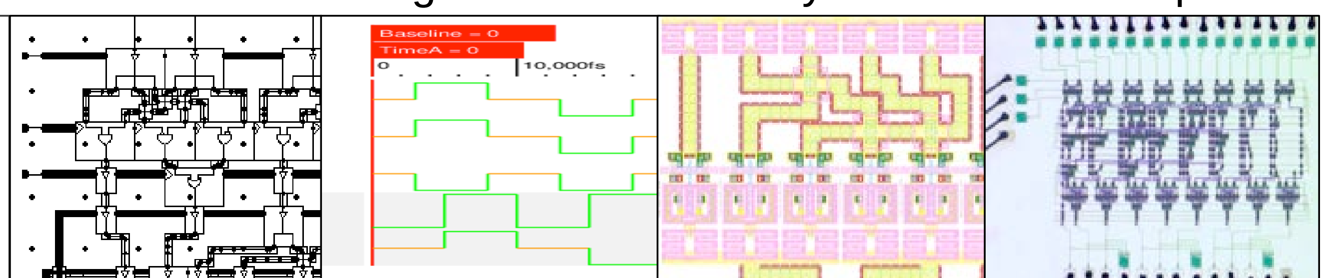
EDA Tools for Top-Down Design



Verilog/VHDL | Schematic | Digital Sim. | Layout | Chip

```
Function: 1-bit full-adder
Pin: input (a,b,carry_in)
     output (carry_out, sum)
Lib: AQFP standard library
Behaviour description:
    sum = a + b + carry_in,
    carry_out = a*b + (a+b)*c;
```



Qiuyun Xu, *et al.*, IEEE Trans. Appl. Supercond., **27**, 1301905, (2017).

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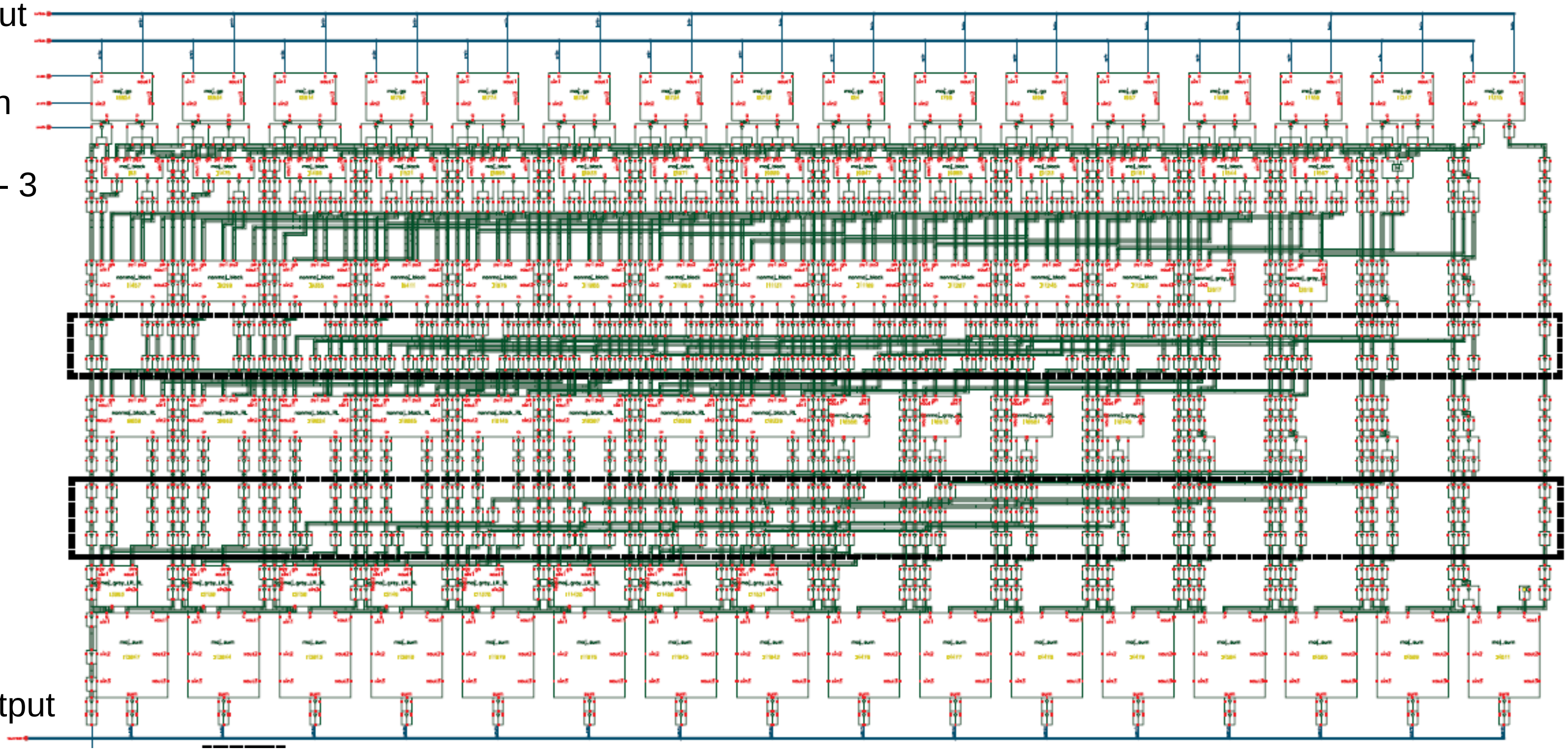
AQFP Circuit Design using EDA Tools

Layout of 16-b AQFP carry-look-ahead adder

Data input

Excitation current: Phase 1 - 3



Data output

Y. Murai, et al., IEEE Trans. Appl. Supercond., **27**, 1302209 (2017).

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Future Directions

- Investigation of design methodology and EDA tools for large-scale AQFP integrated circuits
  - Wire-length limitation
  - Multi-phase clock distribution
  - Majority-based logic synthesis
  - Microprocessor architecture
- More energy efficient logic
  - Use reversible QFP (RQFP) [1].
- New applications
  - Control and readout circuits for Quantum computers
  - Read out circuits for superconducting sensor arrays

[1] N. Takeuchi, *et al*. Scientific Reports, **4**, 6354 (2014).

Summary

- Adiabatic quantum flux parametron (AQFP) is extremely energy efficient logic.
  - ~1 zJ/bit @5 GHz
  - Three orders of magnitude smaller than energy-efficient SFQ logic
  - Six orders of magnitude smaller than CMOS logic
- AQFP has excellent properties as a logic circuit in terms of gain, functionality, speed, energy consumption, driving ability, error rates, robustness, and density.
- AQFP microprocessors are under development based on CMOS-like design methodology and top-down EDA tools.